Wideband Sampling by Decimation in Frequency

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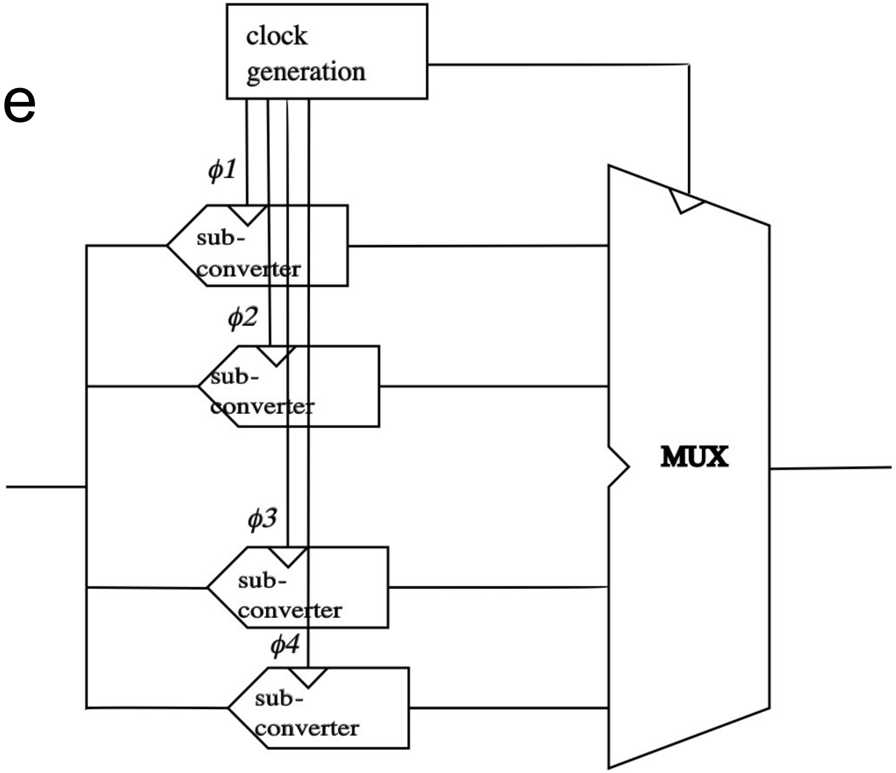
Old-fangled high-speed

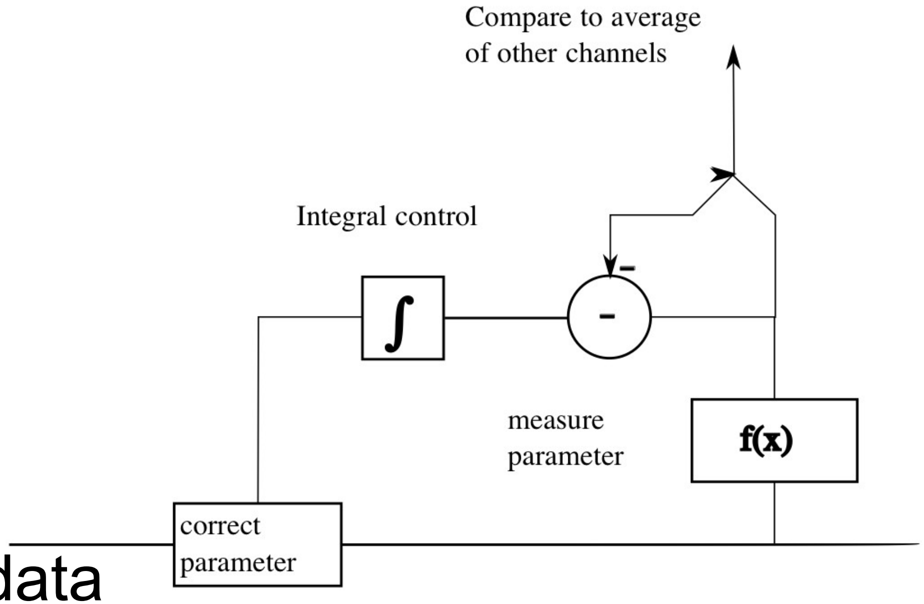
- "round robin"
  - aka "ping-pong" (N=2)
  - aka N-path
- rotate sampling, reassemble
- each sampler full BW
  - and full load on input
- Need good matching
  - gain, offset, BW, …
  - or correction

multipath.svg



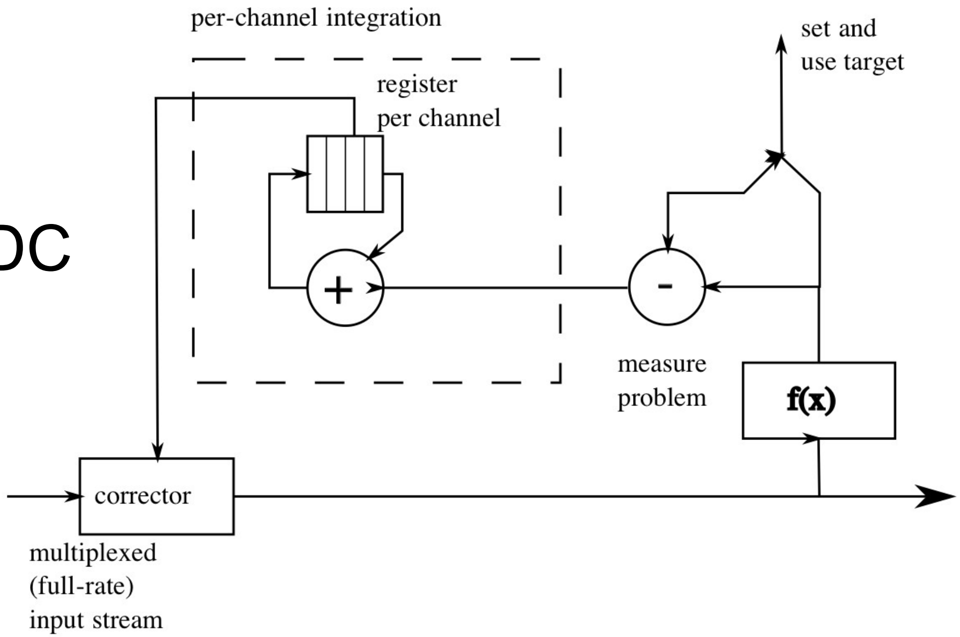
Fixing round-robin: feedback

- Measure and correct parameter
  - e.g. offset
    - measure DC
    - add same
  - e.g. gain
    - measure rms
    - multiply
- Assumes (ako) stationarity
  - e.g. clock not locked to data
- Correction can be A or D



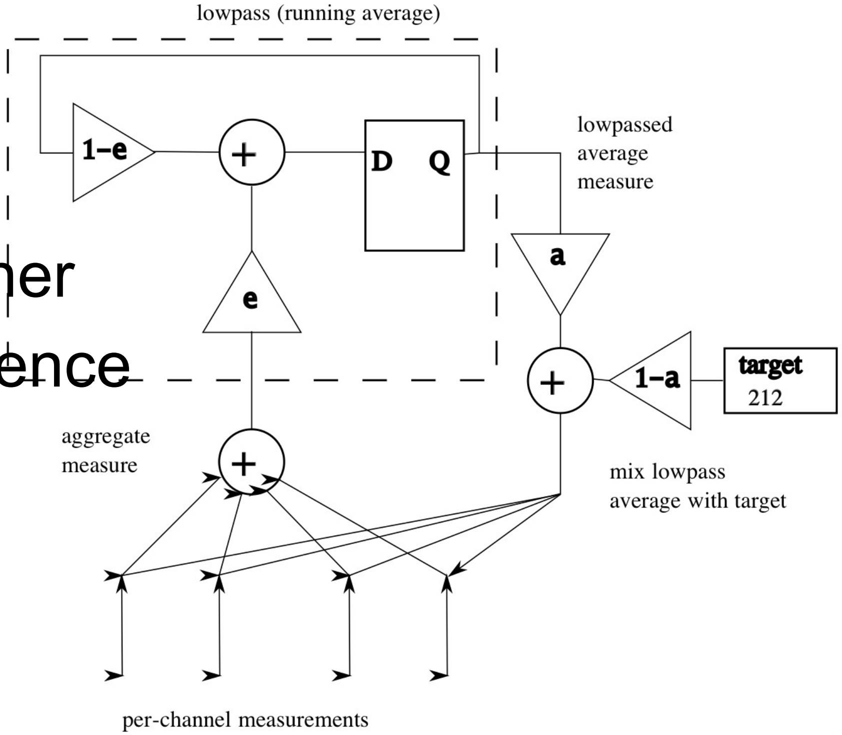
Fixing multiplexed stream

- Easily modified to work on the full-rate stream
  - (digitally)
- efficient implementation
- e.g.: f(x) = x
  - integrate per-channel DC
    - relative to target
  - subtract
  - just a high-pass filter
    - per-channel
    - convergence easy to verify



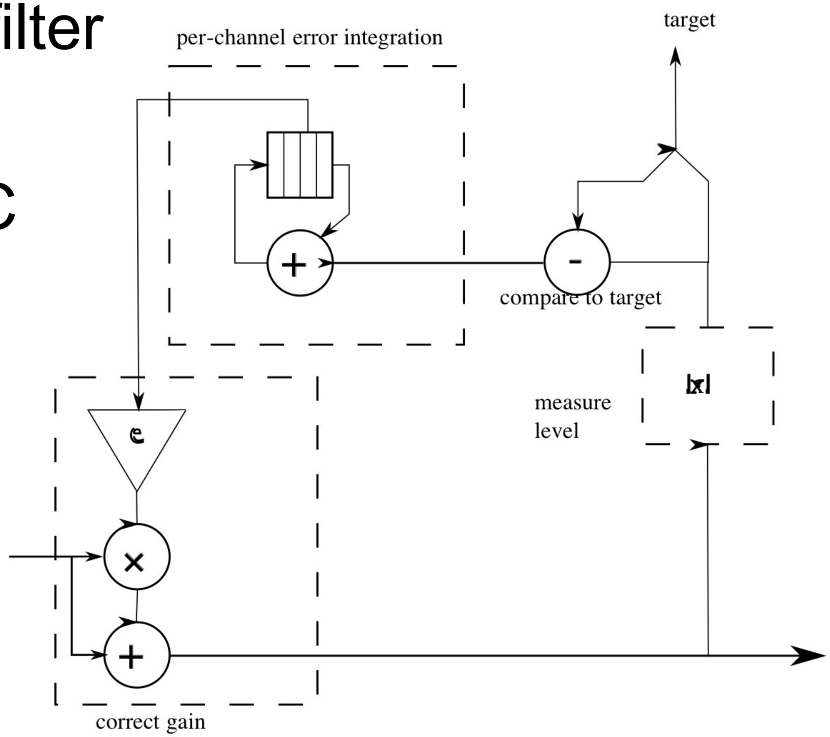
Setting the target

- average the measurement
  - over channels and time
- mix with a target
  - otherwise they all drift together
  - or pick one channel as reference
- feed back to correctors



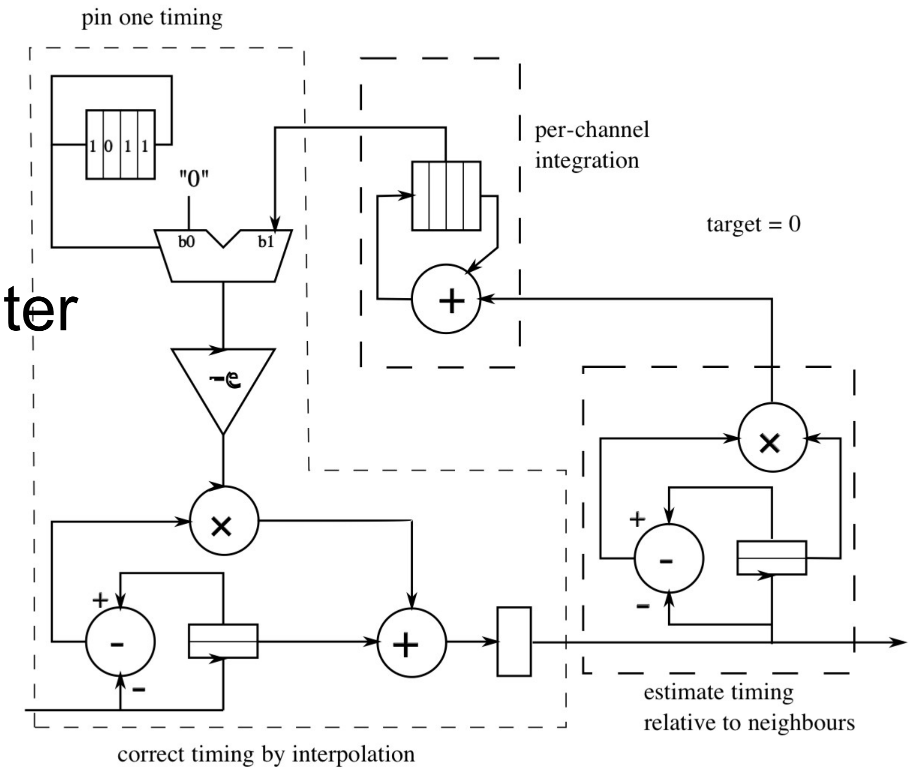
Correcting gain variation

- force average magnitudes to match
  - set small epsilon to avoid distortion
  - convergence same as for filter
- Gains can be set A or D
  - analogue combines w AGC



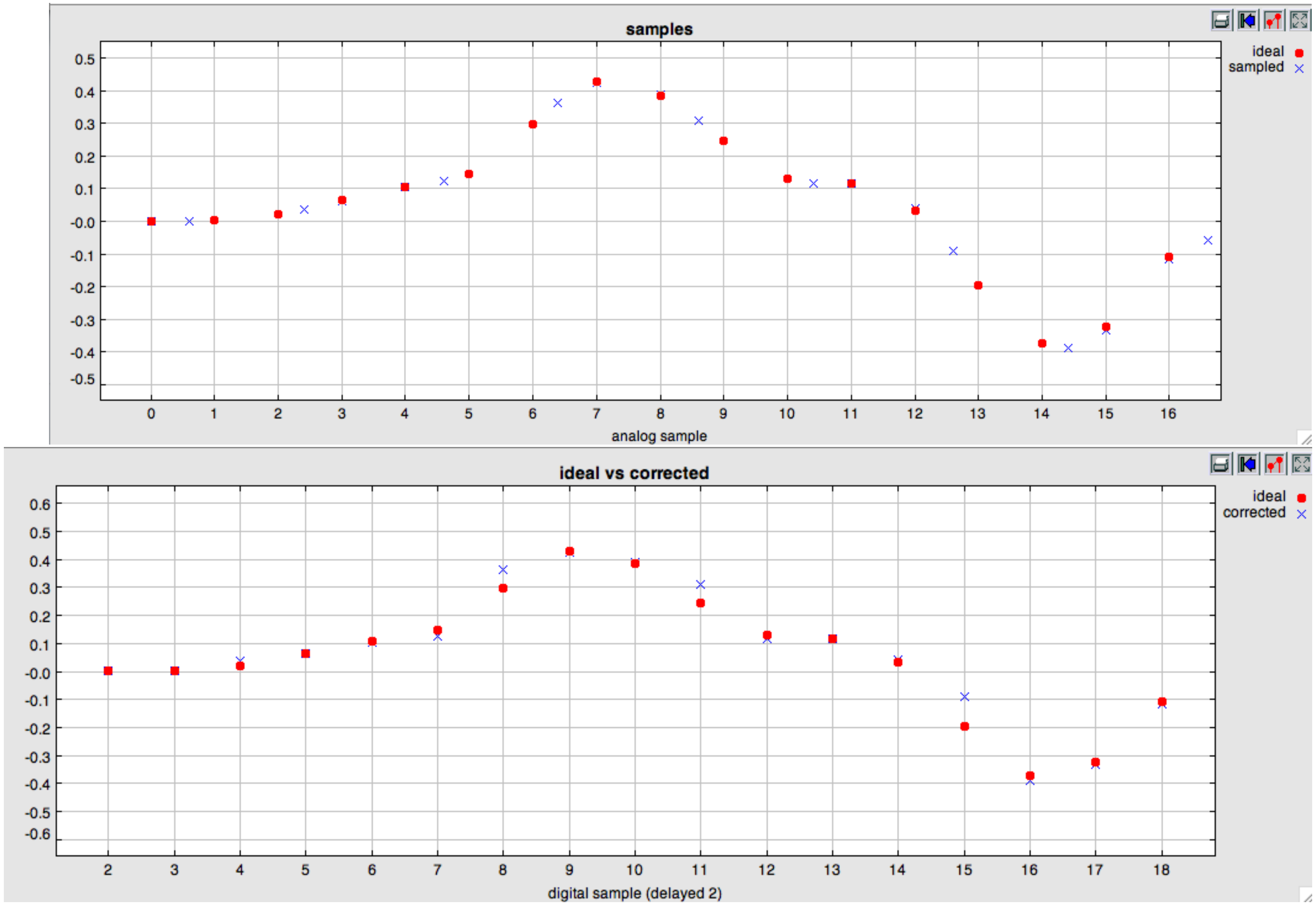
Correcting timing

- Measure correlation with (previous - next_
  - ideally 0
- do interpolation to correct
  - or adjust in analogue
- Same convergence as for filter



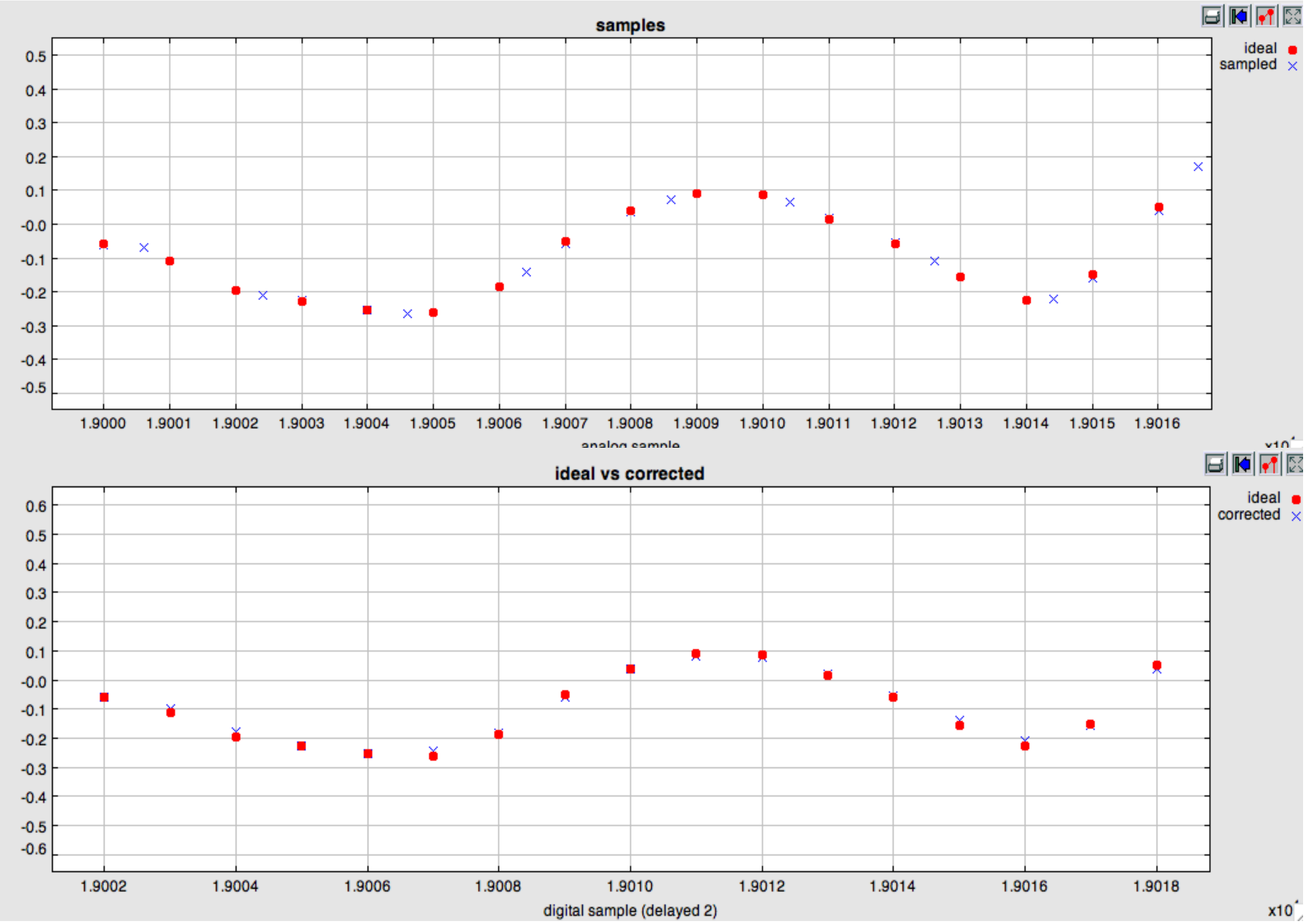
Correcting timing: before

As sampled vs. as interpreted by digital system



Correcting timing: after

As sampled vs. as interpreted by digital system



Old-fangled high-speed

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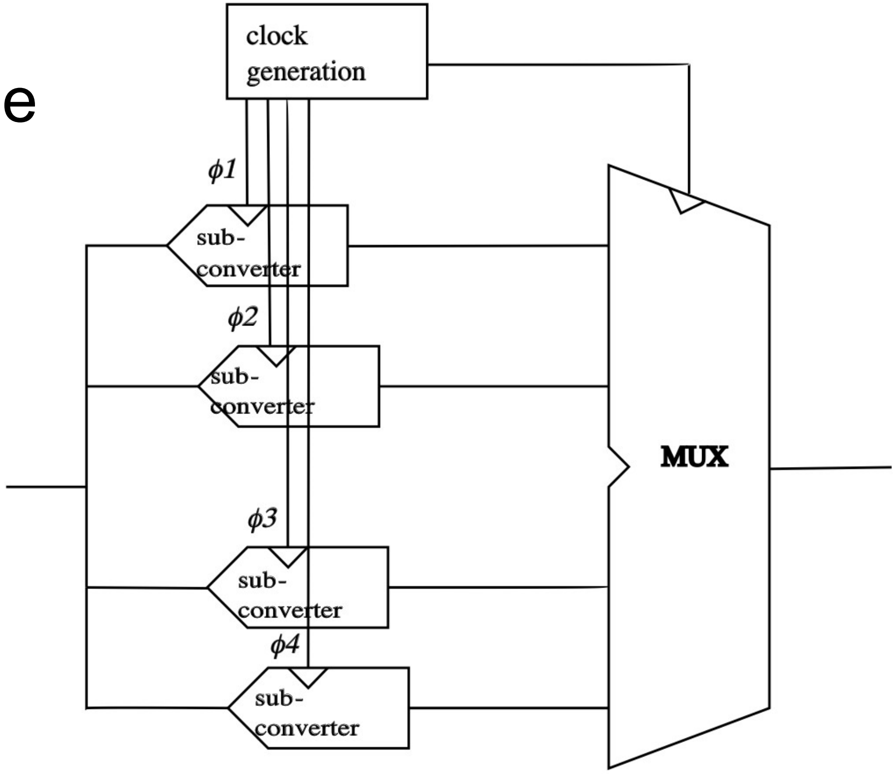
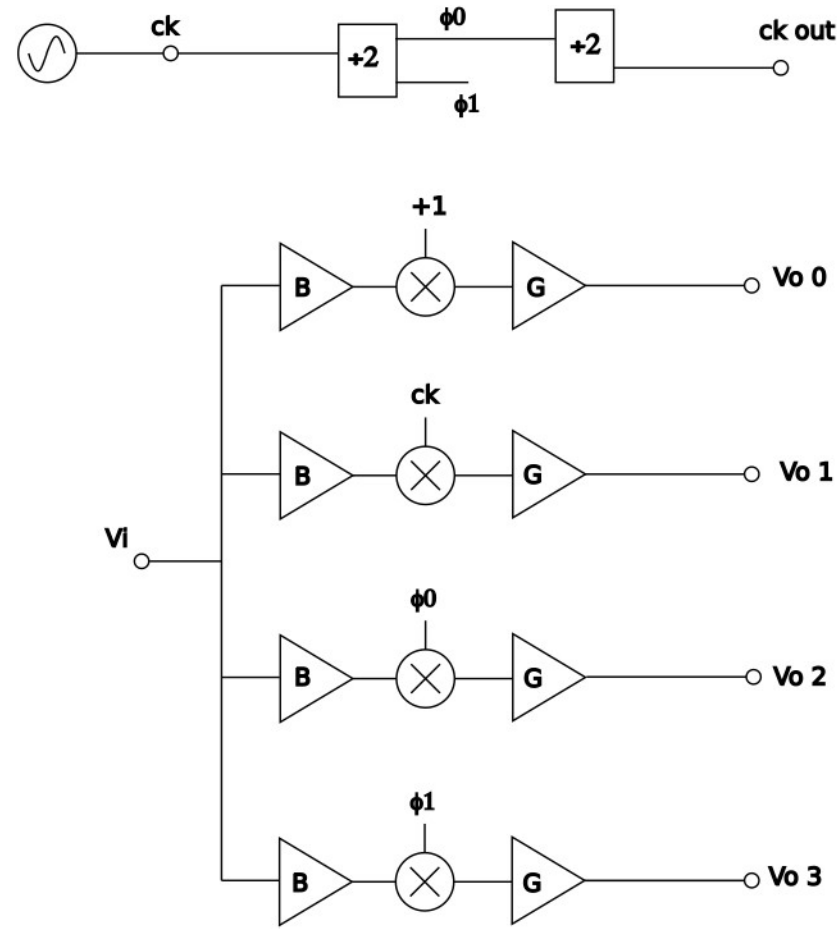


High-speed challenge

- New ADC architecture
- Stretch goal:
  - 100GHz
  - 7b
- Modular plan
  - decimation in frequency front end
  - plus low-power “passive” pipeline
  - DSP correction

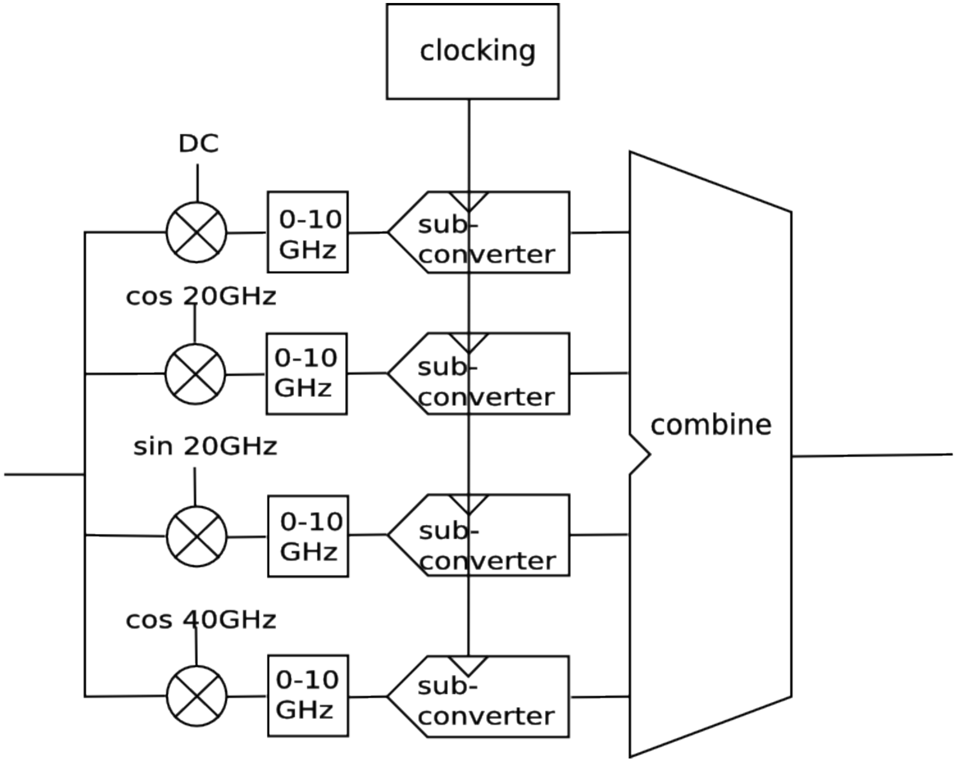
New Front End

- Decimation in frequency
  - as opposed to “-in time”, which is round-robin
- Big win: low-BW sampling
  - smaller switches
  - less injection
    - better linearity
    - less offset
    - lower sampler power
  - lower jitter sensitivity
  - easier clock distribution



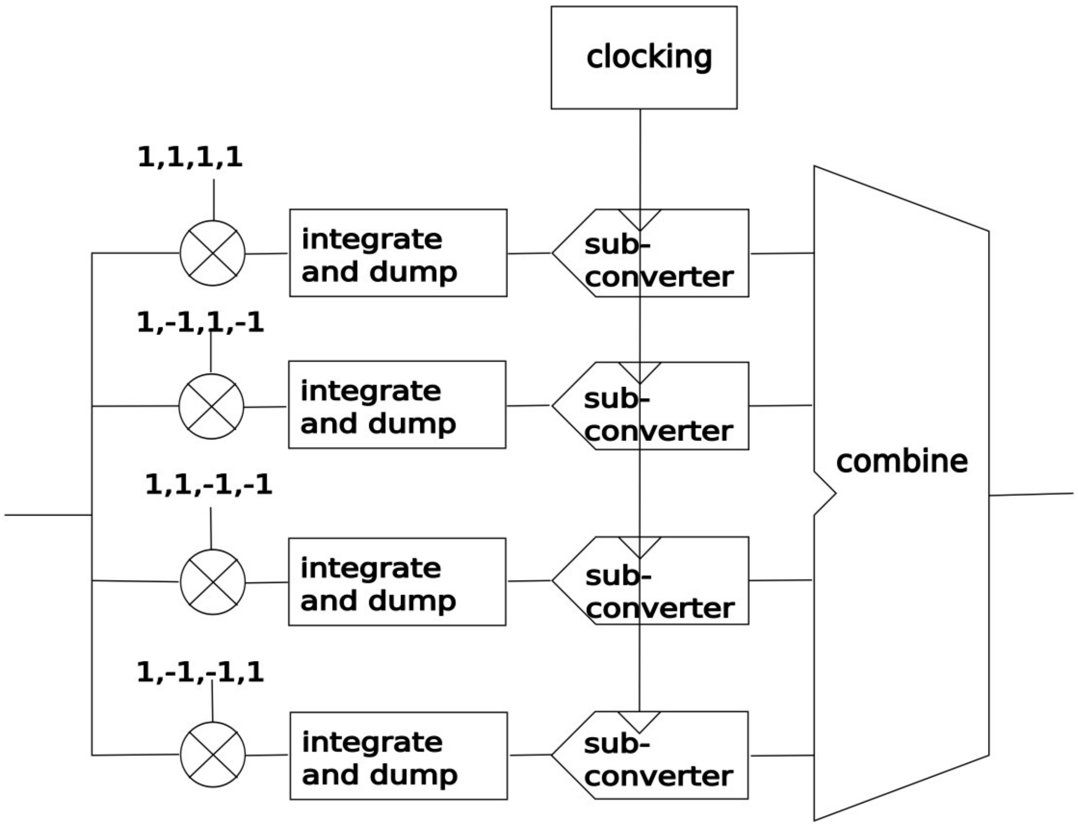
Mixer-based front end?

- basic idea: split into bands
- why: lower bandwidth into samplers
  - smaller switches
  - easier jitter requirements
- but: need anti-alias filters



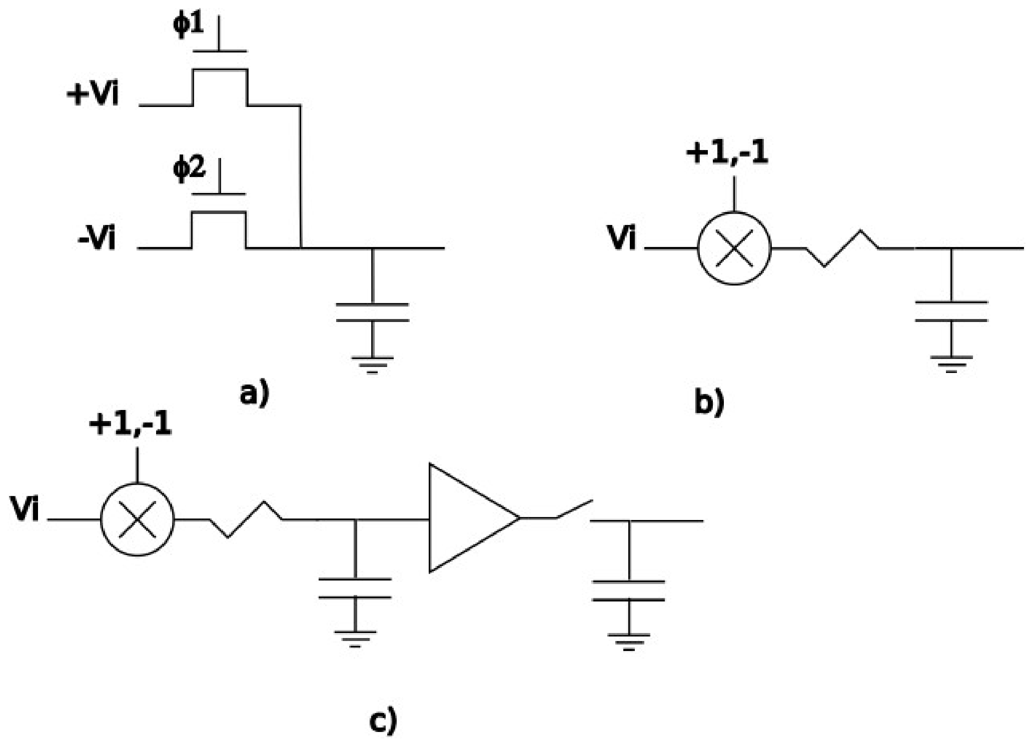
Walsh front end?

- replace brickwall filters with integrate-and-dump
  - & prefilter by sinc
- remove alias with post-processing
- but: integration needs infinite DC gain
- but: "dump" needs infinite-speed switch



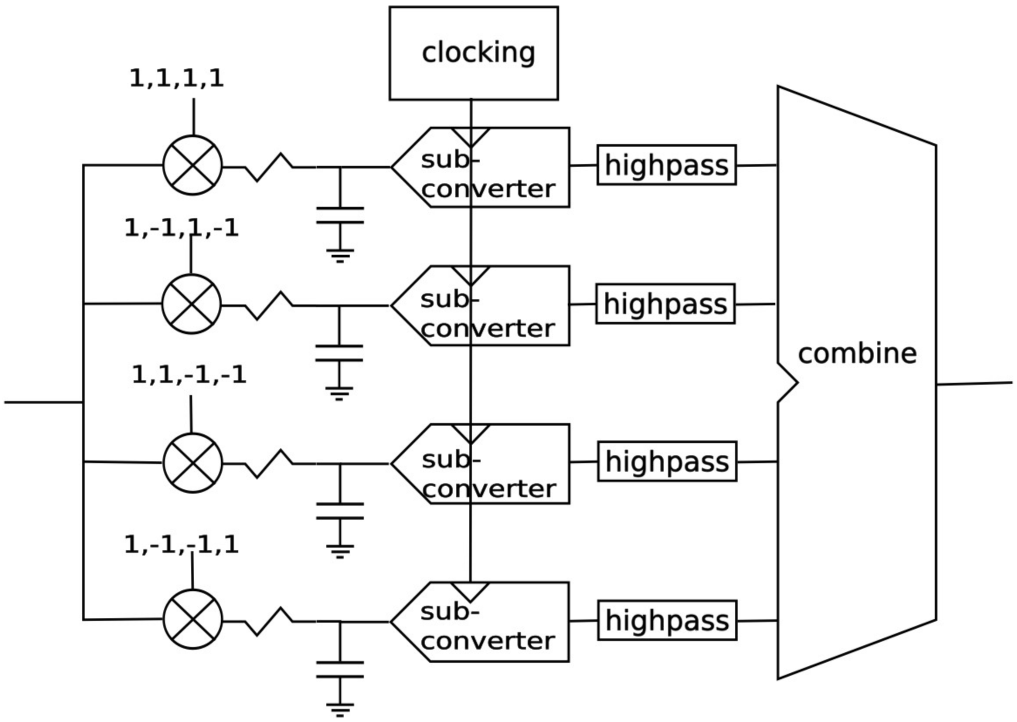
Practical components

- filtering:
  - low Q
  - low gain
  - order ~ # of stages
- mixing
  - overdriven LO
- sampling
  - low BW
  - simple clocking
- fanout
  - 2-4x at speed
  - tree structure



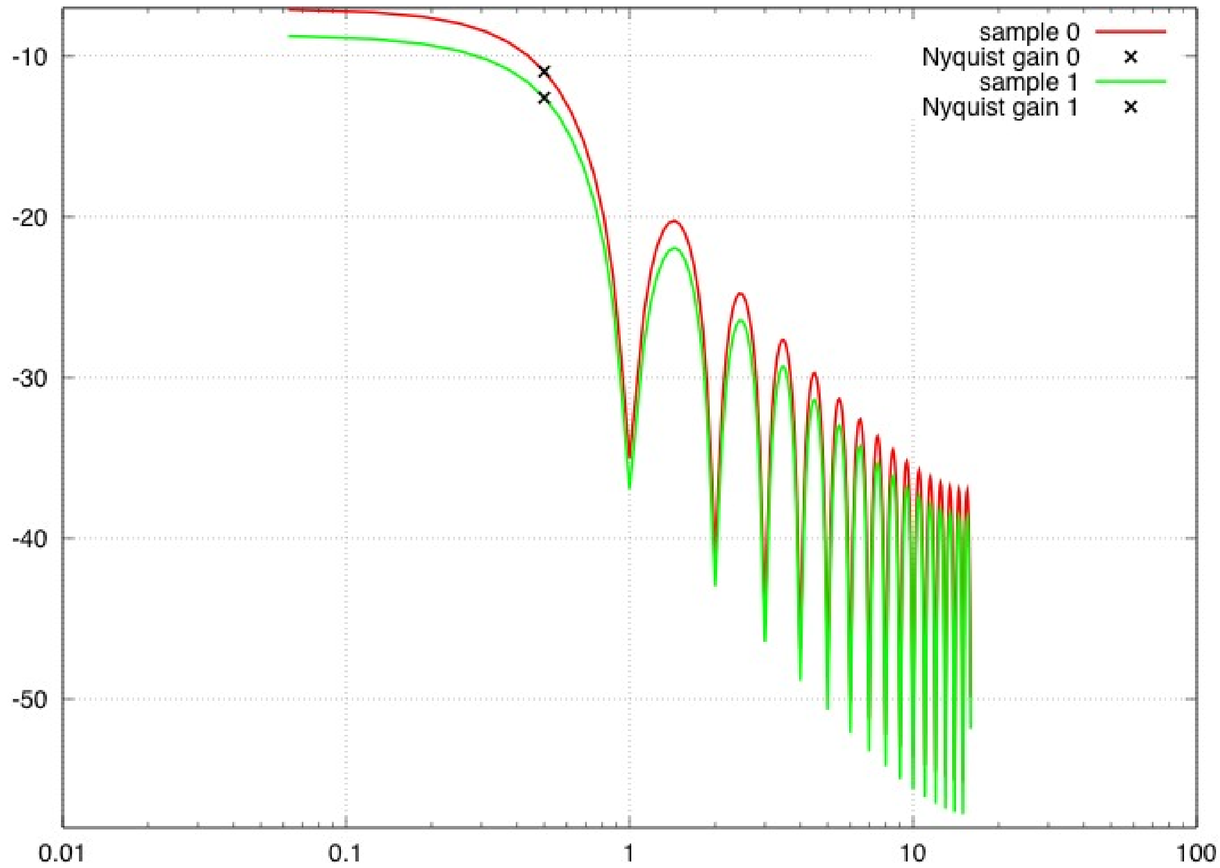
Walsh-RC

- replace integrate-and-dump with:
  - RC
  - N=1 highpass
  - derived from CIC architecture
- Mathematically exact
  - for RC



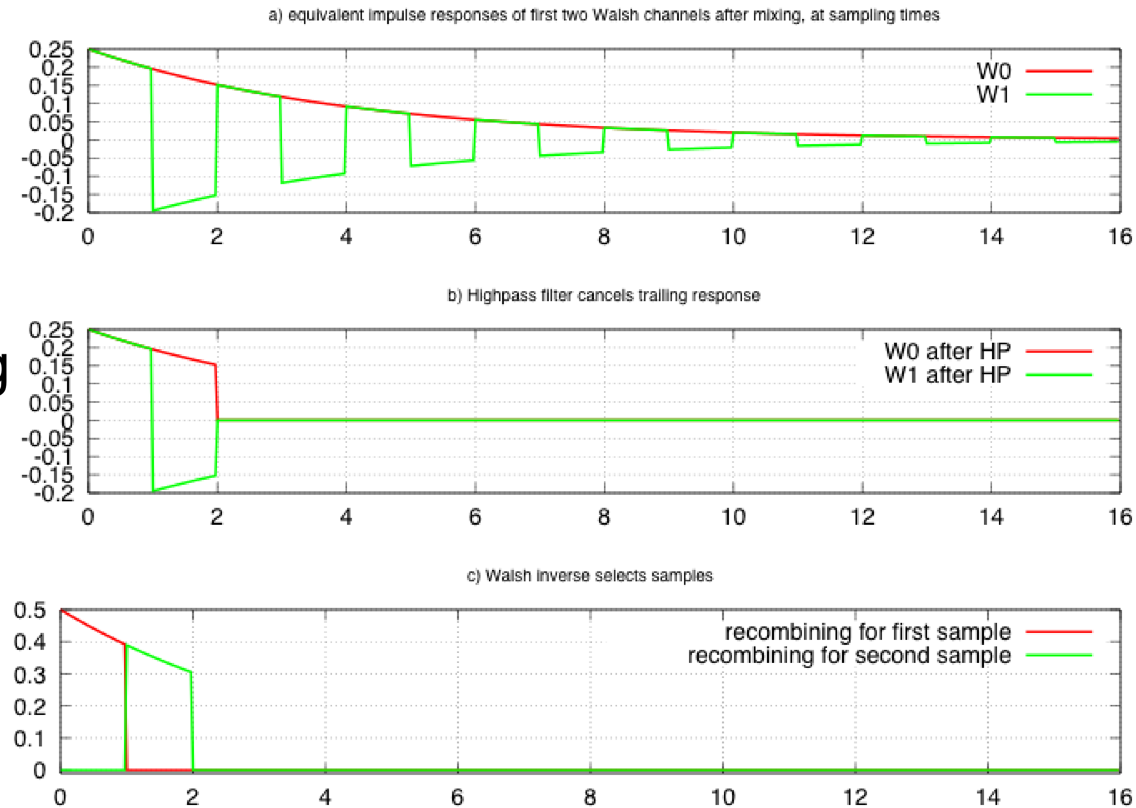
Walsh-RC DSP

- Walsh corrects with [1 1;1 -1]
- RC with [1 1; 1.4 -1.4]
- Walsh has sinc(0.5) = 3.9dB droop
- RC similar
  - 3.9dB at 4T
- free anti-aliasing



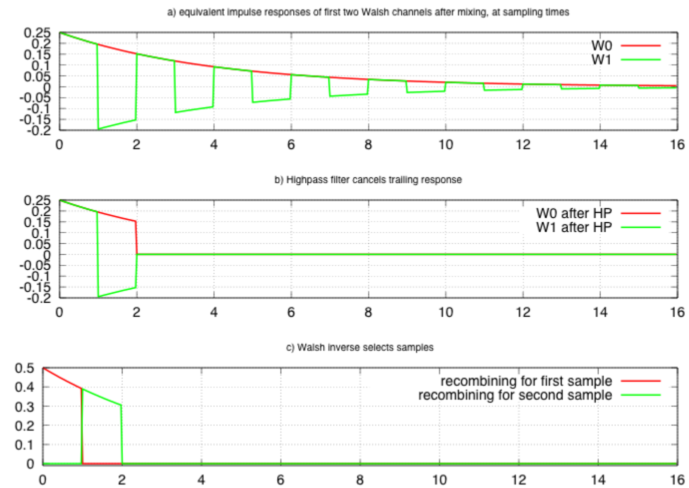
Walsh-RC DSP – time domain

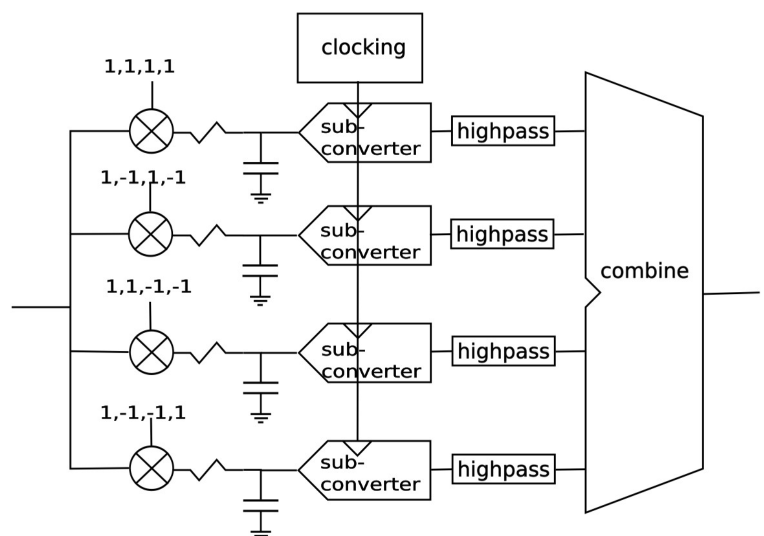
- front end: slow RC
  - vs. Walsh integrator
- mixer modulates impulse response
  - measured at sampling instant
- highpass cancels tail
  - per CIC
- [+ +; + -] selects samples
  - and gain fix
- could stay in FFT...



Impulse Response in Time-Varying Systems?

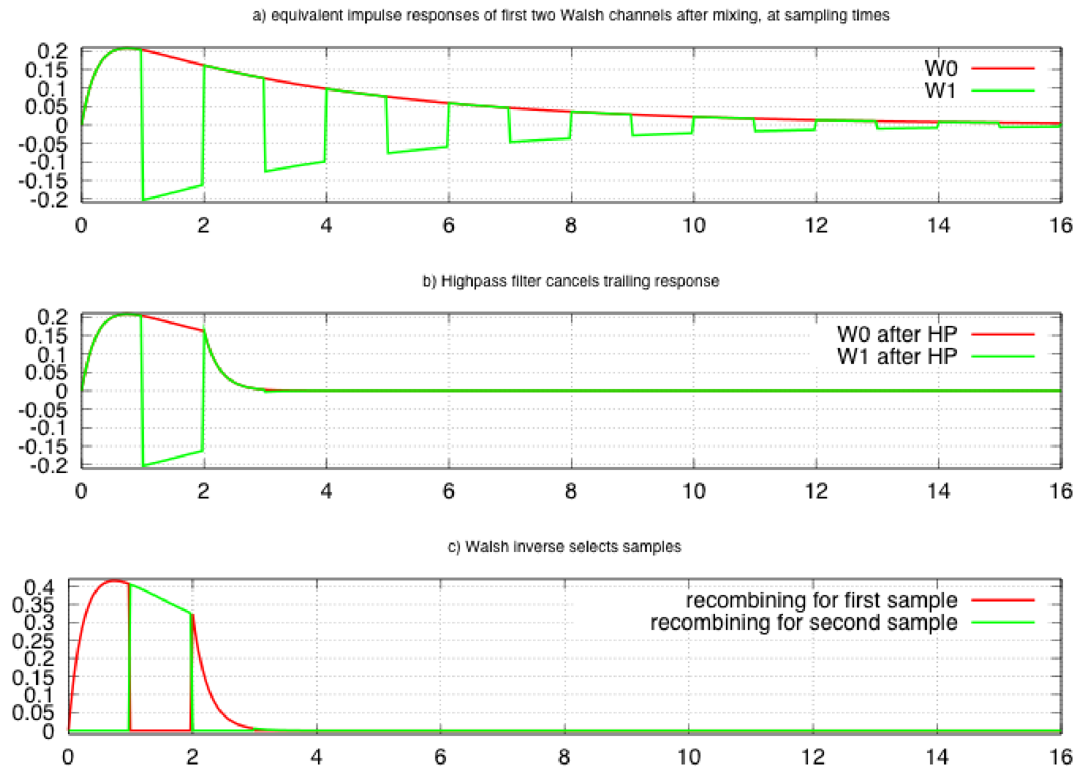
- For time-invariant:
  - apply impulse at time 0
  - record response forwards
  - same for all (t-tau)
- For time-varying
  - measure at time t
  - for impulse at every preceding tau
    - messy for simulation!





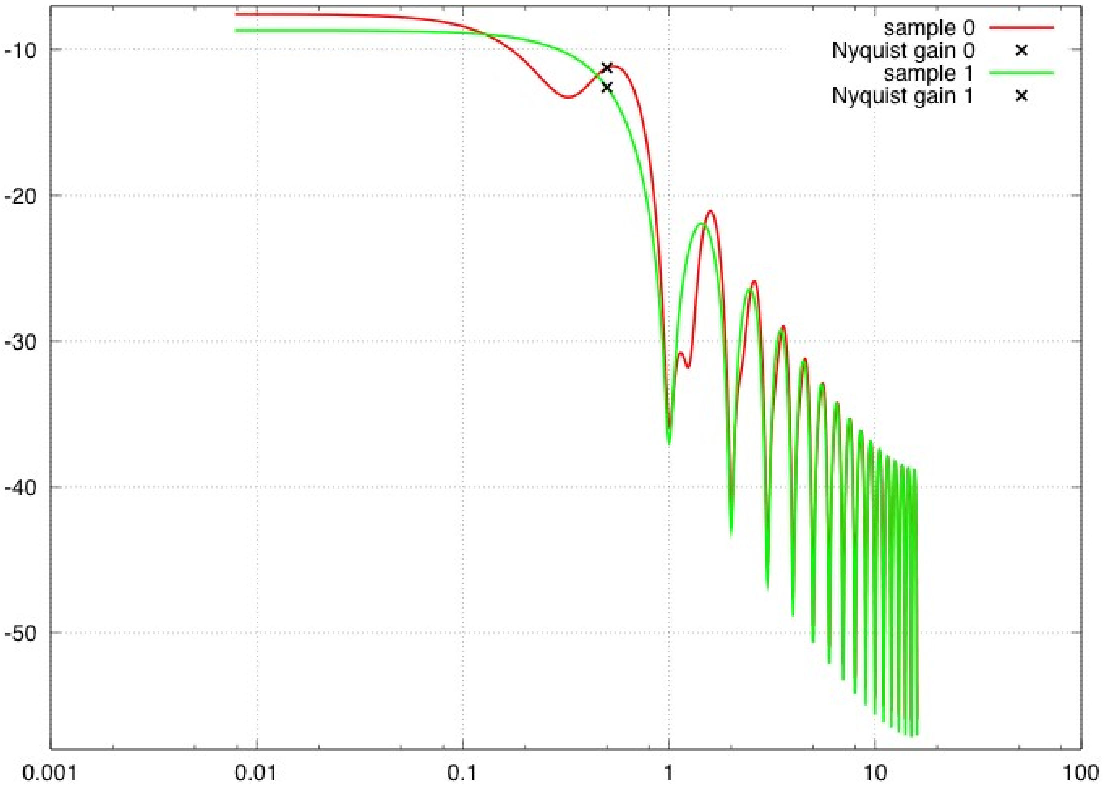
Walsh, higher order, time domain

- Same basic principles
- even/odd samples have different BW
  - needs digital filter to correct
  - timing can be optimized
- “Dominant pole” design approximates ideal RC behaviour



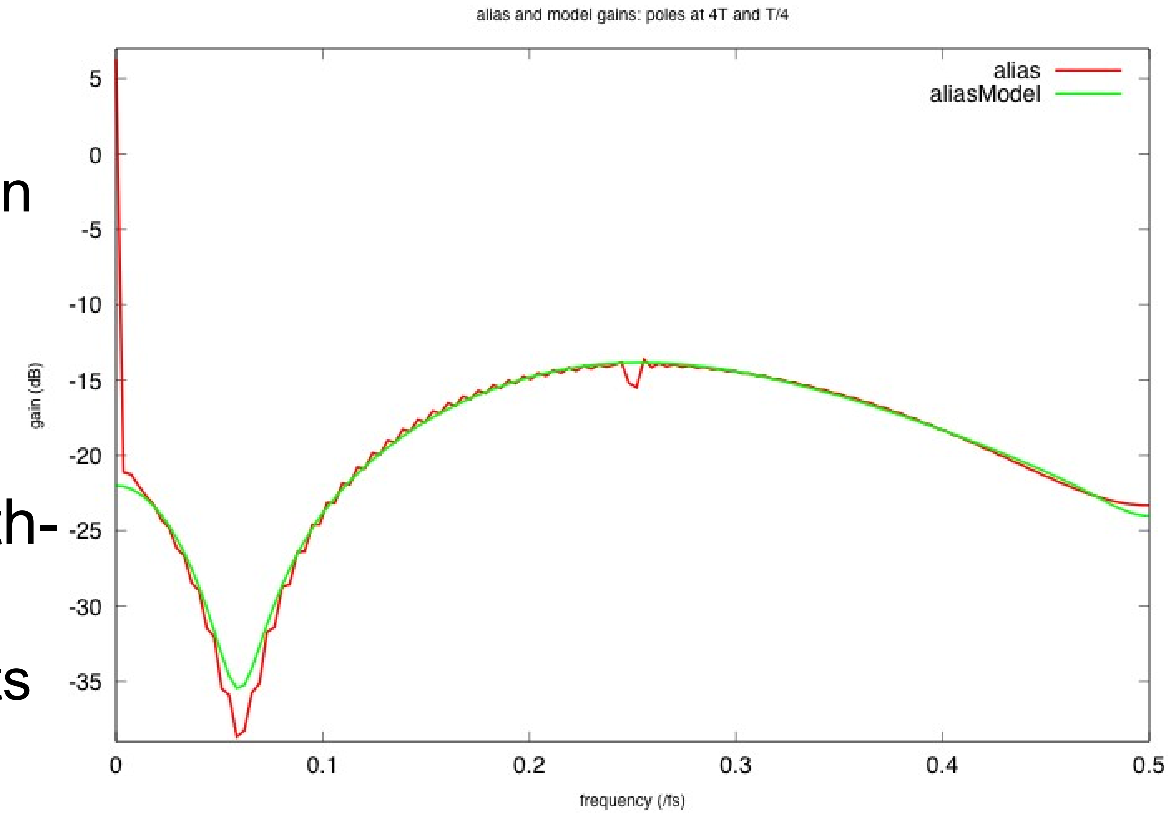
Walsh, higher order; spectra

- Still have ~ sinc()
- needs ~4th-order filter per channel to match
- timing optimization controls dip.
- Works for any transfer function
  - numerically fine if dominant-pole



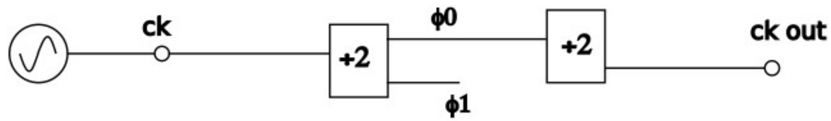
Walsh, higher order; alias view

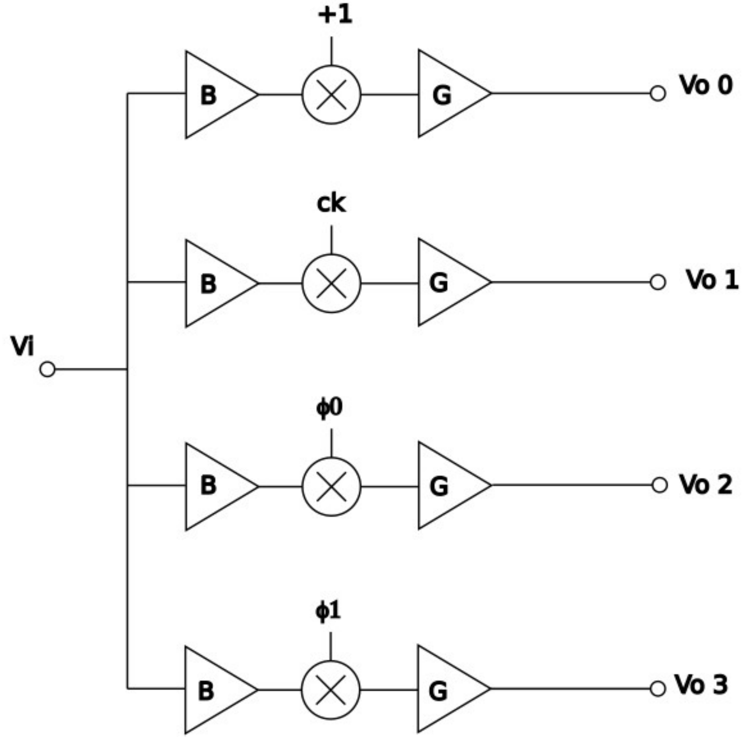
- Example: poles at 4T and T/4
  - no timing optimization
- aliases 15dB down without correction
  - even of gain
- match shown is for 6th-order FIR per output.
  - coefficients of 3-4 bits



Decimation in Frequency

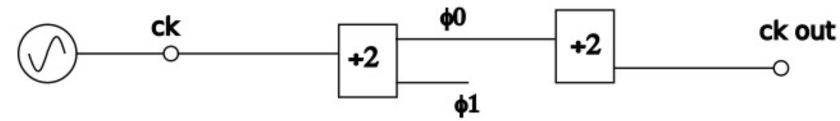
- Big win: low-BW sampling
- Use recursively
  - 2x or 4x cells
  - 2-4-4-4 for 128x, e.g
  - but BW scales per stage
- Takes place of fanout network for signal distribution

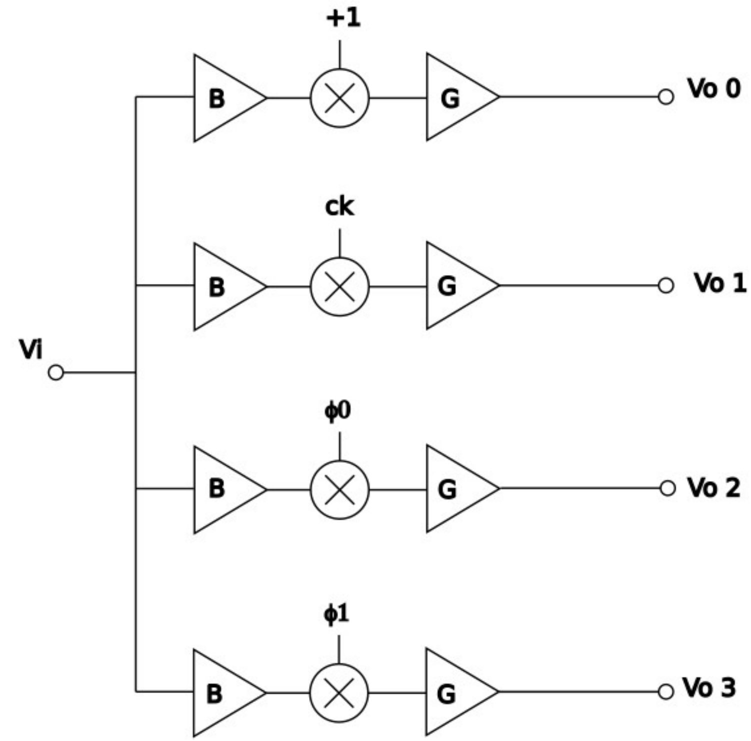




Design example: 100GHz

- clock: 50GHz in
  - 12.5GHz out to next stage
- Buffer: non-dominant
  - 50GHz = T/4
  - 4x fanout ~ current gain
- Mixers: 50G and 2*25G
  - dominates jitter
- Gain: 4T dominant pole
  - 12dB, 3GHz
  - ~ unity gain at next Nyquist
- Next stage: 4x wider
  - ¼ BW, same total power

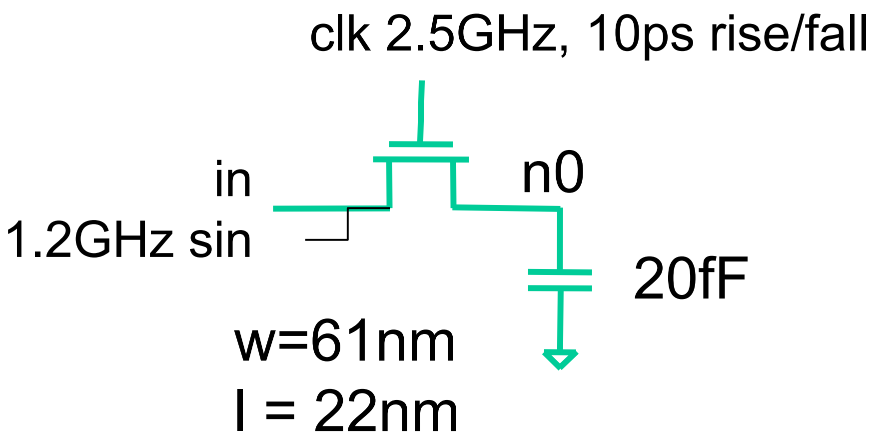


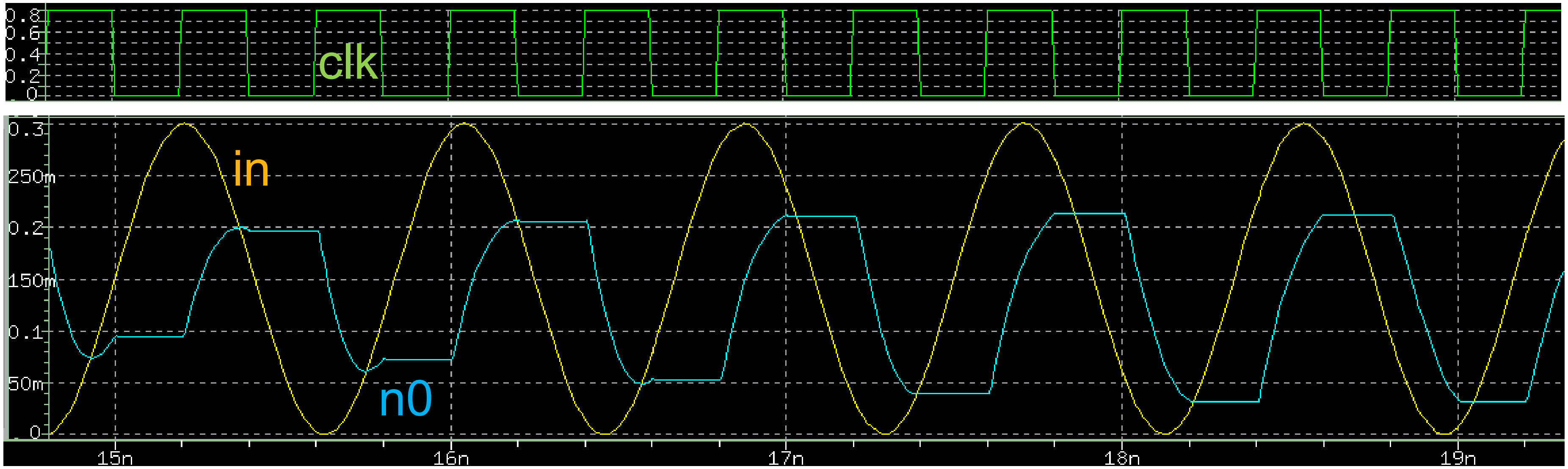


22nm open-source model

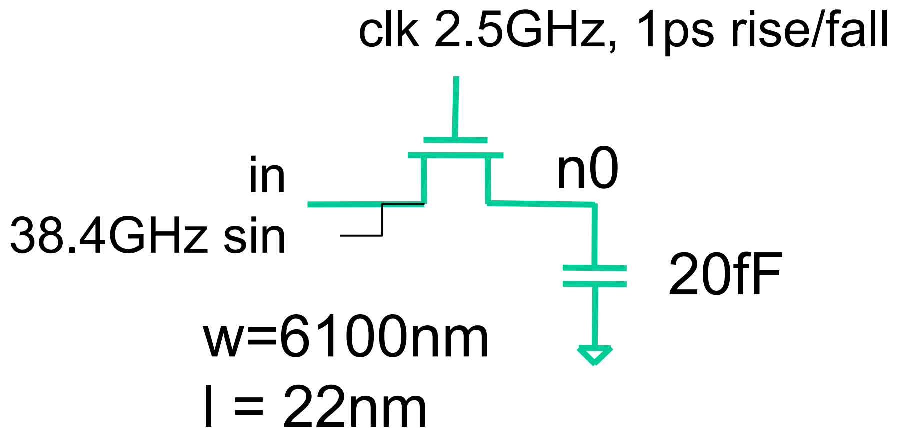
- stay clear of NDA
- http://ptm.asu.edu/modelcard/HP/22nm_HP.pm
  - * PTM High Performance 22nm Metal Gate / High-K / Strained-Si
  - * nominal Vdd = 0.8V
  - .model nmos nmos level = 54
  - ...
- LP variant available
- 16nm, 32nm, 45nm available

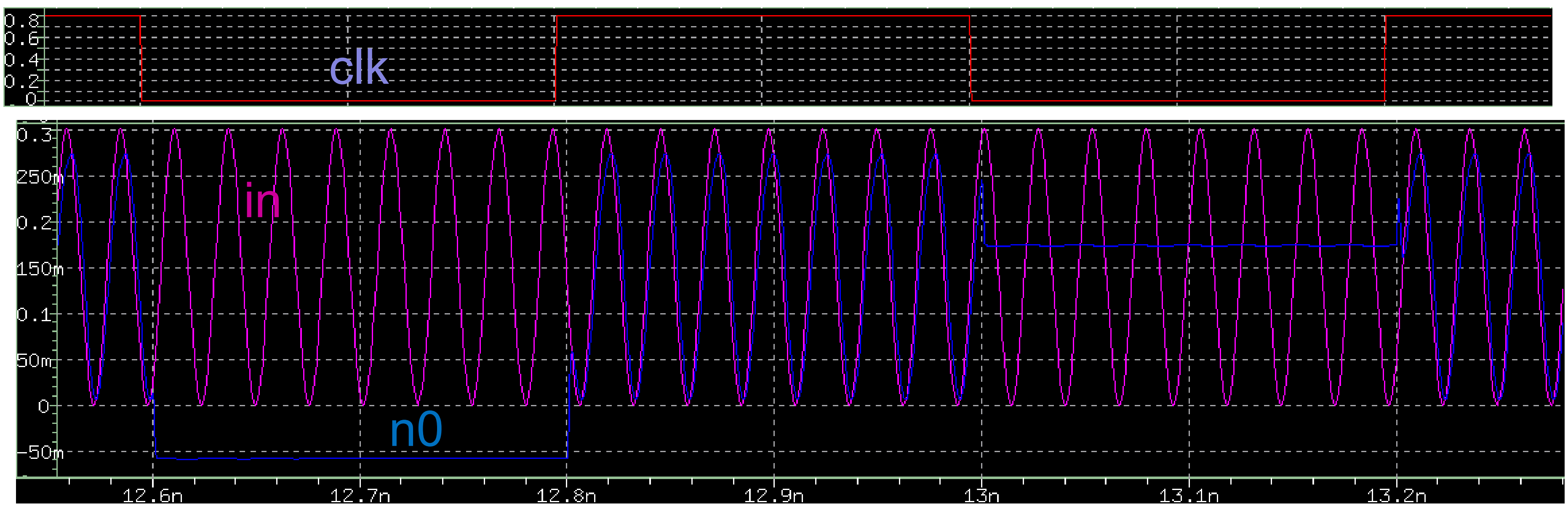
Sampling 1.2GHz sin at 2.5GHz





Sampling 38.4GHz sin at 2.5GHz

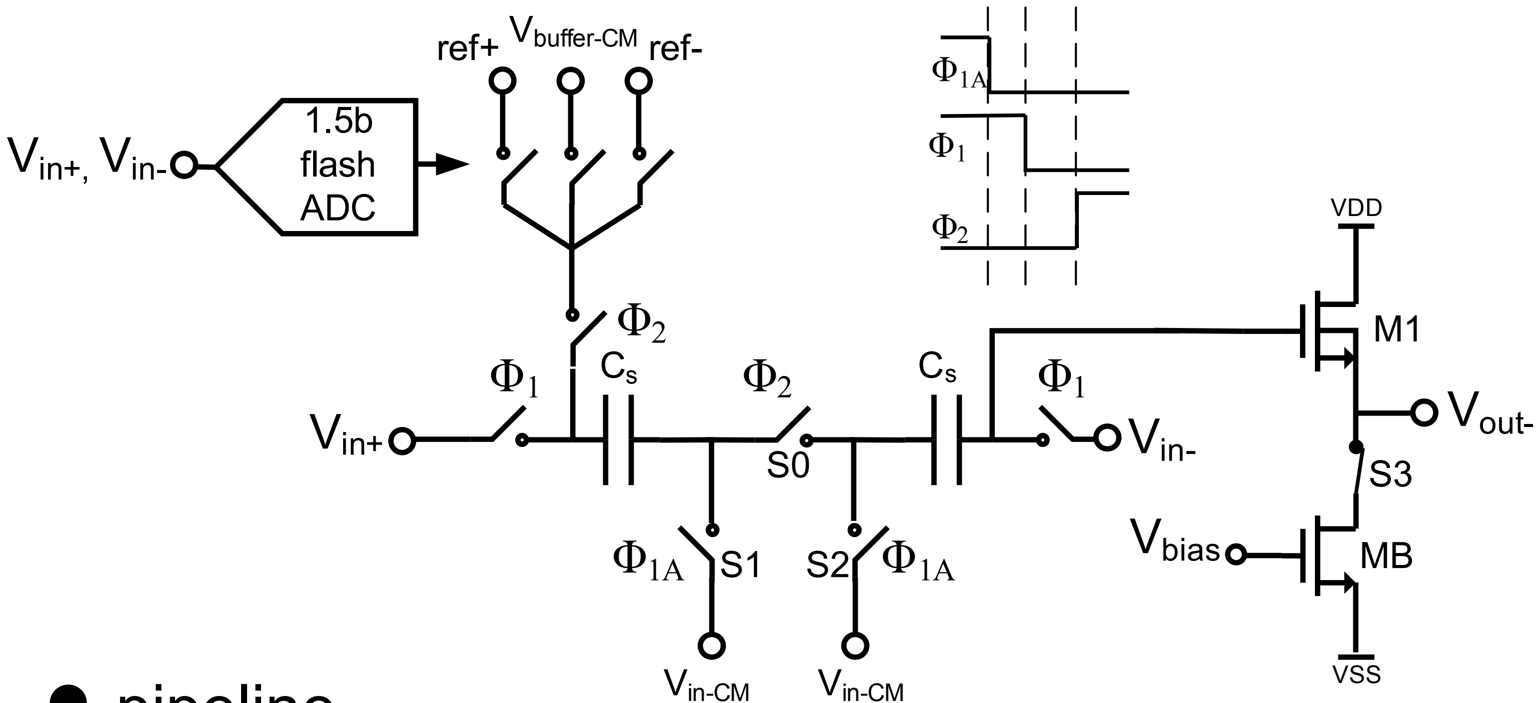




Reduced-BW sampling win:

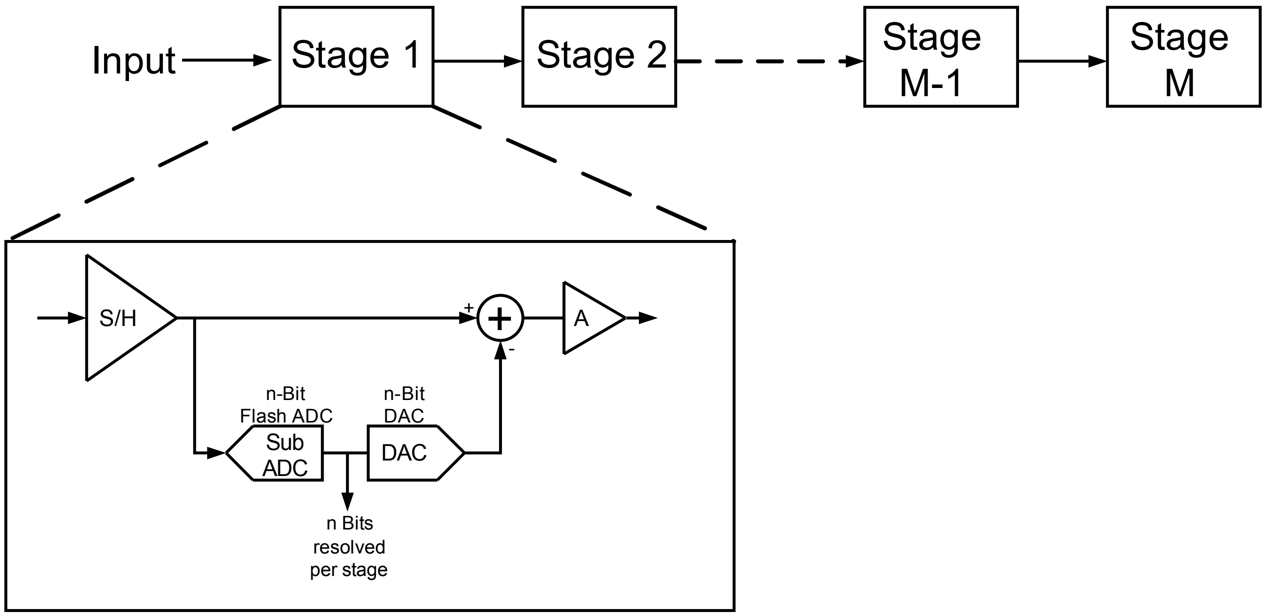
- 100x smaller sampling device (61/22nm)
  - 100x less clock drive requirement
    - 100x easier to manage jitter
  - 100x less load on input driver
  - 100x less pedestal
    - 100x better PSRR
    - 100x better linearity
- in exchange for front-end mixers
  - 1 50GHz mixer vs N 100GHz (effective) samplers

Subconverters?



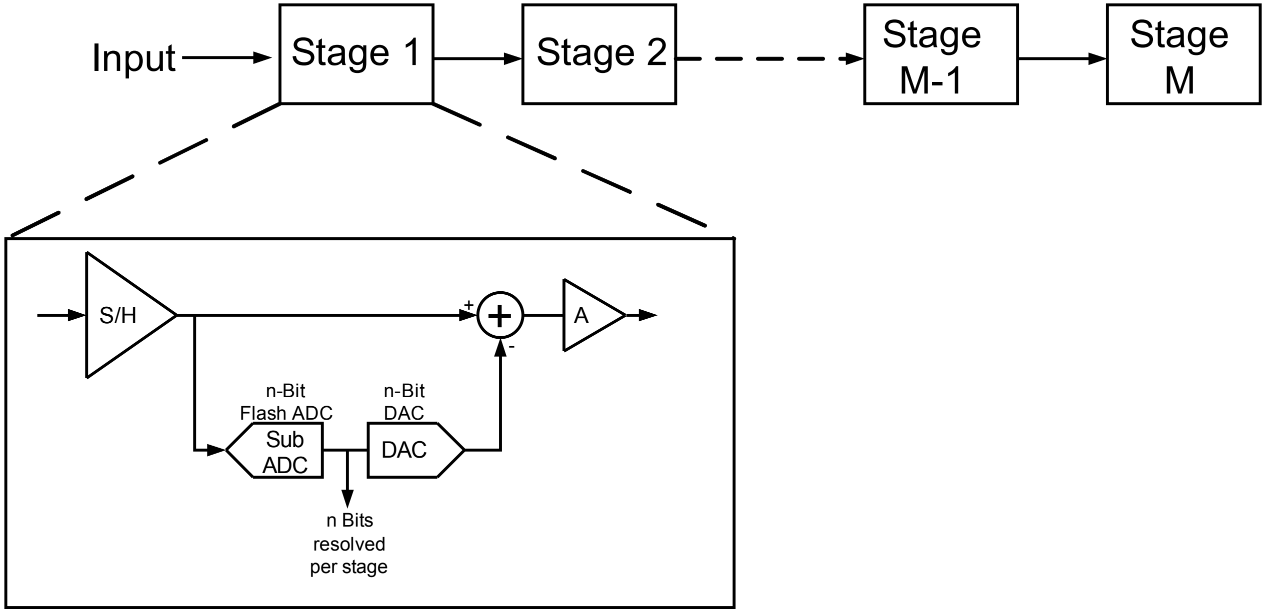
- pipeline
  - fewer distinct subconverters => easier DSP (less state)
- low-power version
  - no op-amps

Pipelined ADC



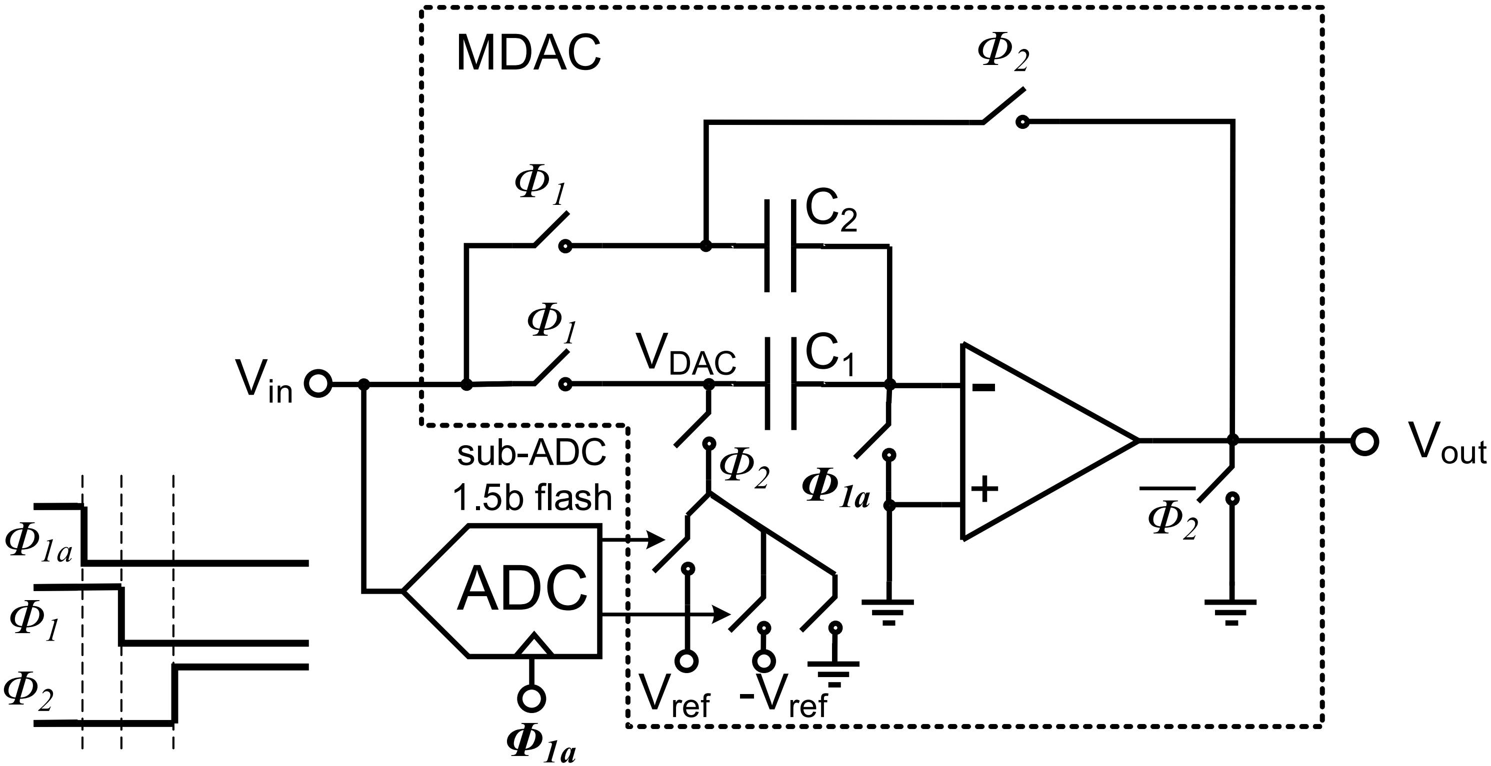
- ✓ **Nyquist-rate ADC (thus fewer ADCs required to interleave to achieve a high sampling rate)**
- ✓ Comparator redundancy allows for large mismatch in comparators
- ✓ Can generally push most calibration to the digital domain (i.e. no analog calibration required)
- ✓ **Can easily increase resolution by adding more front-end stages**
- ✗ Some passive devices required → area can be larger than SAR (but not necessarily)

A low-power pipelined ADC approach



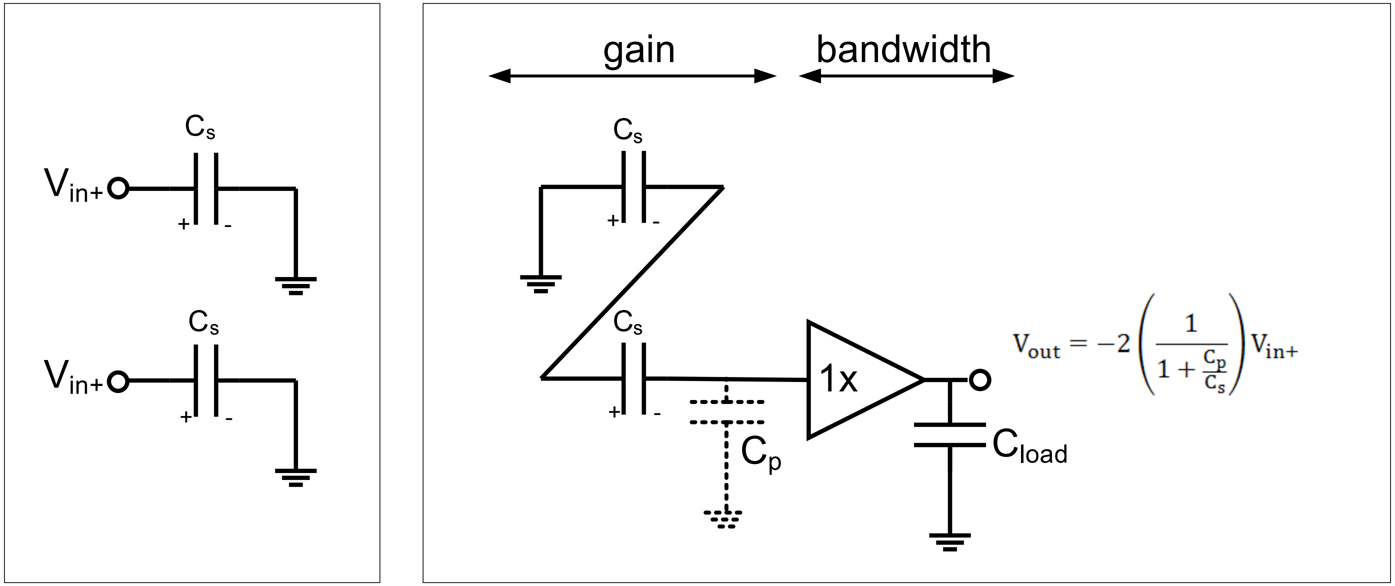
- Traditionally pipelined ADC implemented with opamps, resulting in slow, more power consumption (which is why it hasn't been used much in very high speed ADCs)
- Recent advances allow for opamp-less designs, enabling low-power and high-speeds

Classic 1.5b pipelined stage



- Speed, power limited by opamp
- Attenuation around loop results in closed loop speed being a fraction of open loop speed

Gain using capacitive charge pump

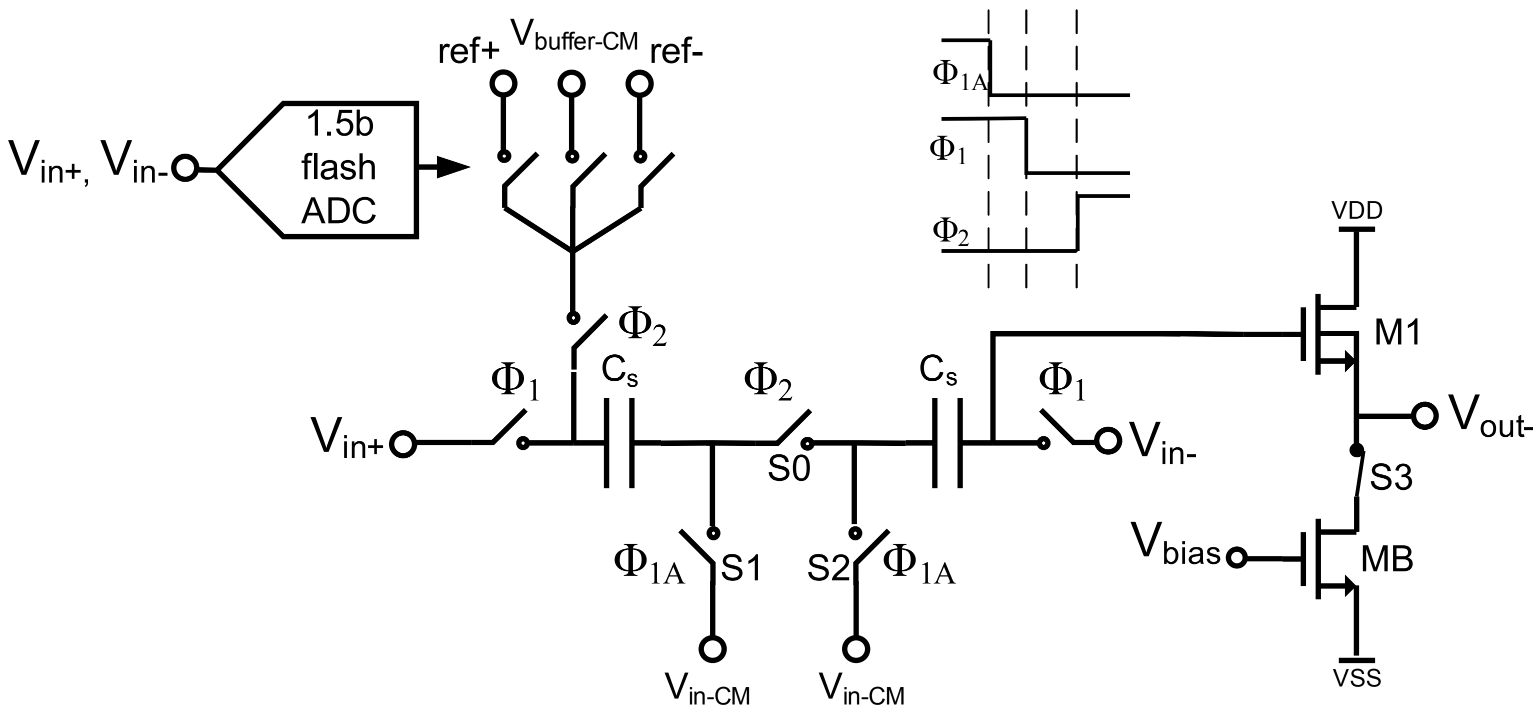


During Φ_1

During Φ_2

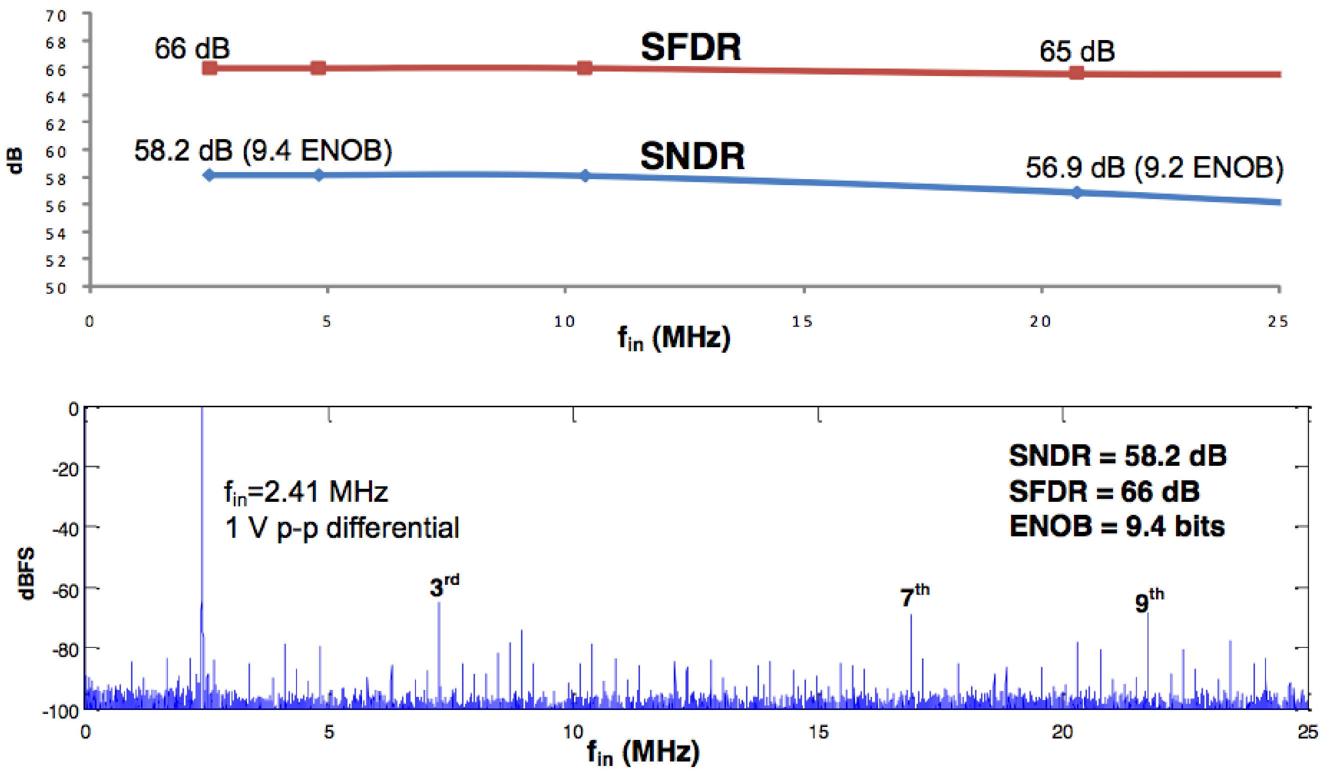
- Charge pump inspired gain stage
- Gain, bandwidth operation decoupled
- No opamps, open loop operation → very low power →fast
- Requires simple digital gain calibration

ISSCC '09/JSSC '10 – Ahmed et al



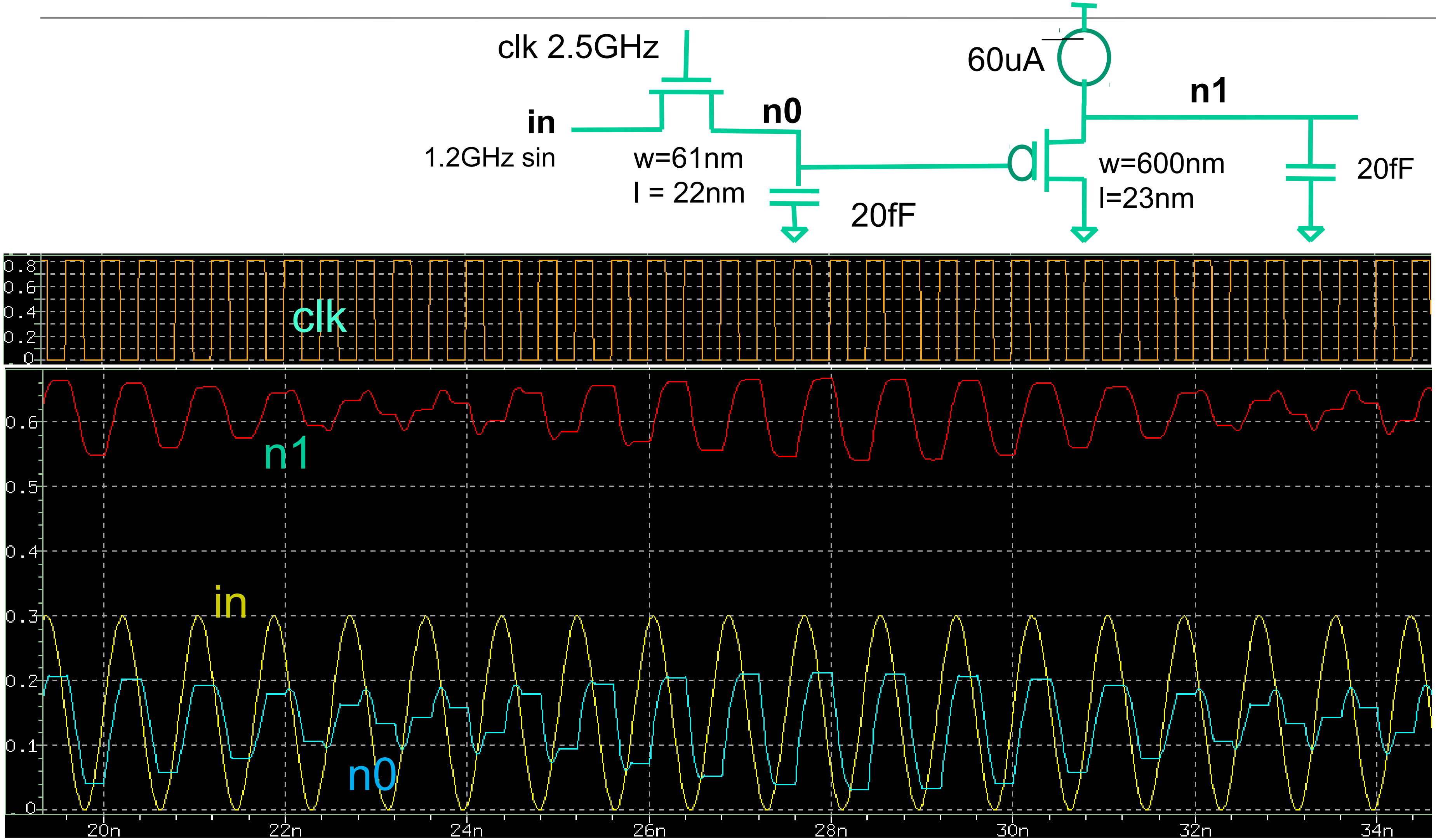
- MDAC stage can achieve high speed for very low power
- For 6-bit: not kT/C limited hence can use very small C_s → very small input cap
- Has compact area
- **Source follower can be efficiently made very fast**

SNDR, FFT plots



- 10-bit ADC, 50MS/s, 3.9mW analog, 6mW digital in 1.8V 0.18um CMOS → 0.3 pJ/step
- Can adapt topology for higher speeds, lower resolution → should have much better FOM in newer technologies
- Successful simulations of 6-bit ADC in 0.18um with 1V supply (w/some modifications)

Source follower in 22nm



Fast ADC

- i.e. too fast for efficient single-path
  - e.g. 40*2.5GHz
- round-robin
  - needs correction for mismatches
  - has difficult front-end requirements
- Walsh/frequency-domain
  - also needs correction
  - easier front end
  - weirder

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