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A 4GHz Fourth-Order SiGe HBT Band Pass ΔΣ Modulator

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Abstract

Test results for a fourth-order band pass (BP) ΔΣ modulator (ΔΣM) are presented. The 0.5-μm SiGe HBT design uses active LC resonators with Q enhancement and return-to-zero latches to drive the feedback DACs. The packaged circuit consumes 350mW from a single 5V supply when clocking at 4GHz. Measured results indicate a maximum SNR of 53dB, SFDR of 69dB, and a dynamic range of 62dB, all in a 4MHz bandwidth.

Introduction

Band pass ΔΣ modulators (BPΔΣMs) are attractive for converting IF [1] and RF [2] analog radio signals to digital. Such conversion is useful because it allows mixing, channel selection, and signal processing to be done in the digital domain, greatly alleviating the tolerance problems associated with analog circuitry.

The design presented here is a higher-order, reengineered version of the second-order design in [2], with a new resonator and return-to-zero (RZ) latch and greater attention paid to circuit nonidealities. As well, the new design is in a different process (advanced SiGe HBT [3]).

Modulator Architecture and Circuit Design

A block diagram of our fourth-order LC bandpass ΔΣM is shown in Fig. 1. The input voltage goes through a transconductor G_m, producing a current which drives an LC resonator. A second transconductor G_q provides positive feedback to enhance the Q of the on-chip resonator inductor. Because this is a fourth-order modulator, there are two such stages, followed by a latched comparator which both samples the signal and provides one-bit quantization. Feedback is provided through various latching stages: first, a master D flip flop (DFF) provides half a delay, then two separate paths with slave and slave/master RZ D flip flops provide additional half and full delays. The feedback is achieved via current summing (KCL) at the resonator outputs, and the values of each feedback DAC current can be tuned. This allows for the modification of the noise-shaping transfer function as well as the compensation of time-domain nonidealities such as excess loop delay [4].

Fig. 2 shows a detailed view of the resonator, which is an improved version of the one published in [5]. The tank circuit is designed for 1GHz resonance and uses top metal spiral inductors of 3.5nH with nominal Q of 6 at 1GHz and 1.525pF MIM capacitors. It is driven by two multi-tanh doublets (shown in the Figure), one for each of resonator gain and Q. The cross-coupled asymmetric differential pairs with emitter degeneration provide wide linear input range which could be varied by altering the 4:1 transistor ratio and number of series diodes.

The one-bit quantizer is a conventional ECL-style master slave differential comparator with preamplification [6]. The return-to-zero D flip flop architecture is new, and the slave/master DFF is depicted in Fig. 3. Each desired half delay in Fig. 1 is provided by a circuit which looks the same as the left half of the DFF in Fig. 3, while the RZ function is accomplished with the circuit on the right half of that same DFF. The cross-coupled latch transistors are replaced with diode-connected transistors as shown. During one half of the clock cycle, these diodes are inactive and the output is free to switch, but in the next half cycle the diodes force the output to zero differential voltage. These outputs drive simple current-steering differential-pair DACs.

Experimental Results

The modulator was implemented in a 0.5μm HBT SiGe process with typical maximum f_t of 40GHz. Including pads, the chip measures 1.64×2.40mm^2; without pads, 0.85×1.46mm^2. Due to the large number of pads (40) and dc biases (15), wafer-level testing was not performed. The chip was bonded inside a CQFP44 package and mounted on a four-layer test board. DC biases were set manually using 10kΩ potentiometers. An on-chip output buffer was designed to drive a 50Ω load. A die photograph is shown in Fig. 4.

The modulator itself operates off a single 5V supply. Input and clock signals were applied differentially through discrete power splitters, and their common mode levels were set with one additional power supply each and bias tees. While running, the modulator consumes 350mW of power. A wide-

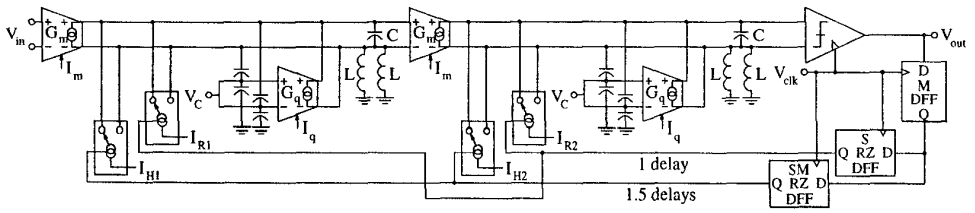

Fig. 1: Block diagram of a fourth-order LC BPΔΣM.

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band spectrum analyzer plot clearly showing a notch at 1GHz (which is one quarter of the clock frequency) appears in Fig. 5. The input tone was -22dBm at 1.001GHz. The tone near 1.25GHz seemed to be caused by coupling of interfering signals through the dc biasing wires that set the input common-mode level.

In a 4MHz bandwidth, the modulator achieved a maximum SNR of 53dB and SFDR of 69dB (11 bits). Fig. 6 plots SNR vs. input amplitude; the graph does not extend to SNR=0 because very small inputs caused noise shaping to cease. This was found to be due to resonators having lower Q tuning range and worse comparator sensitivity than predicted by simulation. Extrapolating to zero SNR yields a modulator DR of 62dB. Time-domain nonidealities were more difficult to compensate for than anticipated, leading to performance only marginally better than the second-order design reported previously. A future design will include more on-chip dc biasing to prevent some of the testing problems experienced here, and work is in progress to determine methods to automatically tune the feedback coefficients to obtain optimal performance in the presence of circuit nonidealities.

Conclusions

We have demonstrated a fourth-order LC band pass $\Delta\Sigma$ modulator in 0.5μm technology for the digitization of 1GHz RF signals. The modulator dissipates 350mW from a 5V supply and achieves eleven-bit resolution in a 4MHz bandwidth.

Acknowledgments

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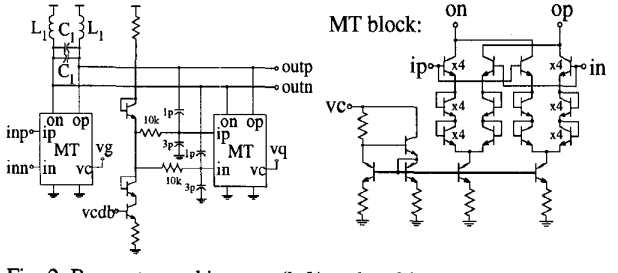

Fig. 2: Resonator architecture (left) and multi-tanh doublet (right).

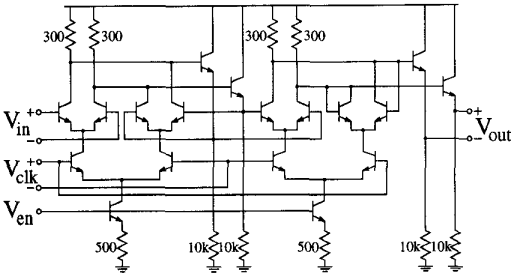

Fig. 3: Slave and master stages of a return-to-zero DFF.

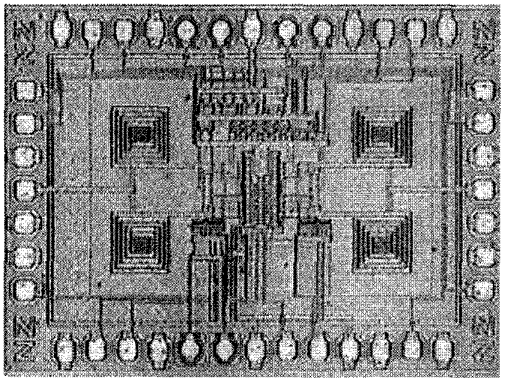

Fig. 4: Die photomicrograph.

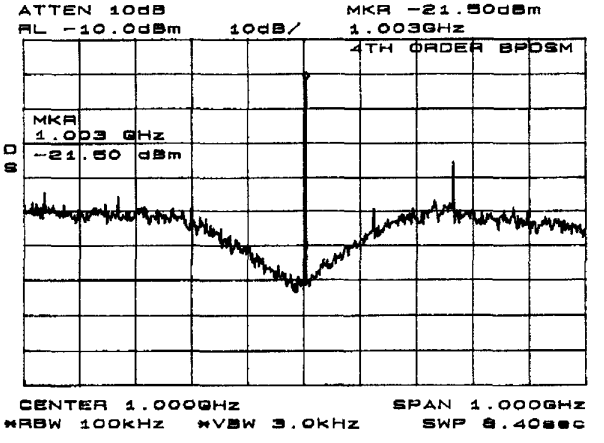

Fig. 5: Plot of output spectrum centered at 1GHz.

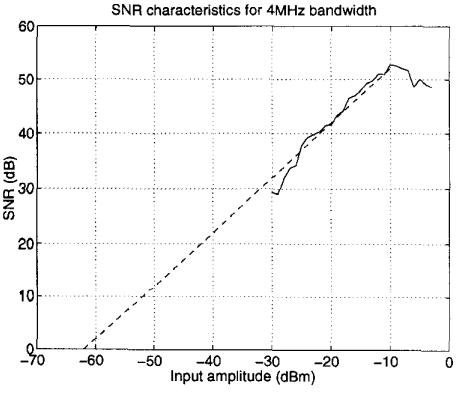

Fig. 6: Measured SNR vs. input signal amplitude.