Loop Delay and Jitter in Continuous-Time Delta Sigma Modulators

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Abstract

The effect of certain fundamental nonidealities on the resolution of a continuous-time (CT) delta sigma modulator are examined in this paper. We start by talking about the equivalence between an ideal CT delta sigma modulator and its discrete-time (DT) counterpart, then consider the effect of quantizer/DAC propagation delay, clock jitter, and the recently-identified phenomenon of signal-dependent jitter on the ideal performance.

I. Introduction

Delta sigma modulators ($\Delta\Sigma$Ms) are commonly used in data conversion applications [1]. The majority of designs are discrete-time (DT) in nature, often switched-capacitor (SC) [2], sometimes switched-current (SI) [3]. Of particular importance for high-speed applications are continuous-time (CT) designs [4], [5], [6]. Fig. 1 shows a typical example of such a design [5]; it is a second-order low pass CT$\Delta\Sigma$M that can be clocked at speeds of a few GHz. Each stage consists of a transconductor (which performs voltage-to-current conversion) and an integrator (which does the opposite). The quantizer produces a voltage output which drives differential pair DACs; feedback summation is achieved via KCL.

A modulator's most important performance measure is the resolution in bits. While many kinds of nonidealities (such as nonlinearities in the input transconductor or finite op-amp gain) can degrade performance, CT designs are particularly sensitive to certain nonidealities involving the quantizer and feedback DACs. Their effects become more noticeable still as clock speeds are pushed ever higher. This paper examines three fundamental nonidealities that affect CT designs and discusses what can be done to compensate for them.

II. Ideal $\Delta\Sigma$M CT $\Leftrightarrow$ DT Equivalence

The presence of a clocked quantizer inside the loop in a CT$\Delta\Sigma$M means that the overall loop can be regarded as DT. To see why this is so, we can "open the loop" around the quantizer as depicted in Fig. 2. The output bit $y(n)$ changes only at sampling instants, and so is a DT quantity. The feedback DAC transforms the output impulse into a CT signal $\hat{y}(t)$, perhaps a full-period non-return-to-zero (NRZ) rectangular pulse as shown. This pulse is filtered by the CT loop filter $\hat{H}(s)$, whose output we call $\hat{x}(t)$, and then sampled at the quantizer, whereupon it becomes the DT signal $x(n)$. This implies the ideal CT loop with loop filter $\hat{H}(s) = \hat{X}(s)/\hat{Y}(s)$ has an equivalent DT loop filter $H(z) = X(z)/Y(z)$ such that the system states (x, y) are equal *at sampling instants*, i.e.,

$$(\hat{x}(t), \hat{y}(t))|_{t = nT_s} = (x(n), y(n)) \tag{1}$$

This equivalence is depicted in Fig. 3. The exact transformation between the two domains is determined by the DAC pulse shape. The circuit in Fig. 1, for example, can be shown to have a CT loop transfer function of

$$\hat{H}(s) = \frac{\frac{k_2}{C_2}s + \frac{k_1 g_{m2}}{C_1 C_2}}{s^2} \tag{2}$$

As shown there, the DACs do indeed produce NRZ pulses (that is, rectangular pulses of duration T_s), and using [4], it is possible to show that the equivalent DT representation for the circuit is

$$H(z) = \frac{\left(\frac{k_1 g_{m2}}{2C_1}T_s + k_2\right)z + \left(\frac{k_1 g_{m2}}{2C_1}T_s - k_2\right)}{\frac{C_2}{T_s}(z-1)^2} \tag{3}$$

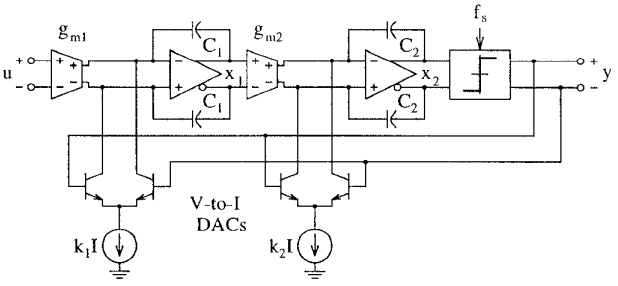

Figure 1: Example of second-order continuous-time $\Delta\Sigma$ modulator.

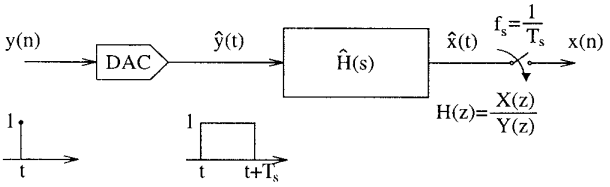

Figure 2: Open-loop equivalent of continuous-time modulator.

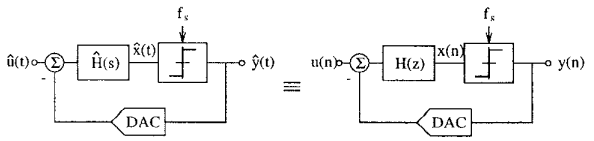

Figure 3: Equivalence between continuous- and discrete-time $\Delta\Sigma$Ms.

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To build the standard double integration ΔΣM [7] which has the $H(z)$ given below on the left of (4), it can be shown that the equivalent $\hat{H}(s)$ for an NRZ DAC is

$$H(z) = \frac{2z-1}{(z-1)^2} \Leftrightarrow \hat{H}(s) = \frac{1.5sT_s+1}{s^2T_s^2} \tag{4}$$

Different DAC pulse shapes (another common one is the RZ DAC whose output lasts $0.5T_s$ and then goes to zero) lead to a different equivalent $\hat{H}(s)$ for a given $H(z)$ [4].

III. Loop Delay

A real quantizer doesn't make a decision instantaneously: there is a nonzero delay before its output switches. Furthermore, there might also be some delay in the DAC, e.g., the differential pair in Fig. 1 takes a few picoseconds to switch. The important quantity in a CTΔΣM is the "loop delay", which we define as the total delay between the sampling clock edge and the edge of the DAC output.

As shown in Fig. 4, loop delay has the effect of shifting the

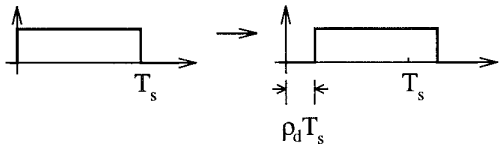

Figure 4: NRZ DAC pulse and delayed NRZ DAC pulse.

DAC pulse in time such that an NRZ pulse becomes an NRZ pulse delayed by some amount $\rho_d T_s$. This changes the mapping between continuous and discrete domains — in a detrimental way, we shall now see.

As an example, consider the modulator in Fig. 1 with a sampling clock of 1GHz (T_s=1ns), $g_{m1}=g_{m2}$=1mA/V, and $C_1=C_2$=2pF. It can be shown that the equivalent DT loop filter for the modulator is given by

$$H(z) = \frac{y_2z^2+y_1z+y_0}{8z(z-1)^2} \tag{5}$$

where

$$\begin{aligned} y_2 &= (k_1+4k_2)-(2k_1+4k_2)\rho_d+k_1\rho_d^2 \\ y_1 &= (k_1-4k_2)+(2k_1+8k_2)\rho_d-2k_1\rho_d^2 \\ y_0 &= -4k_2\rho_d+k_1\rho_d^2 \end{aligned} \tag{6}$$

For an ideal modulator, there is no loop delay, and so ρ_d=0. Using this and k_1/k_2=4/3 in (6), and substituting the results in (5), gives

$$H(z) = \frac{2z^2-z}{z(z-1)^2} = \frac{2z-1}{(z-1)^2}, \tag{7}$$

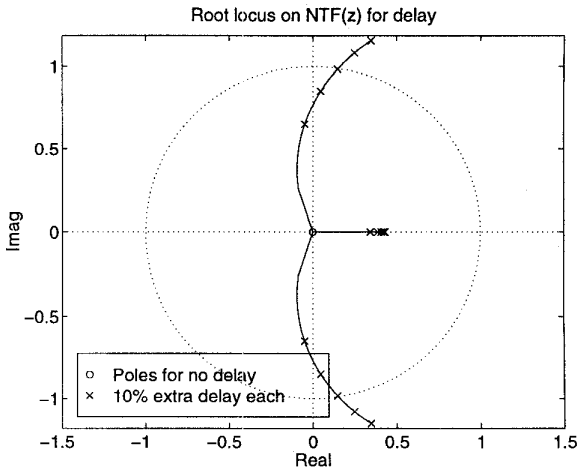

Figure 5: Root locus plot showing how loop delay affects stability.

which is the usual double integration ΔΣM from (4). In an actual modulator, $\rho_d \neq 0$, in which case $y_0 \neq 0$ in (6), and the pole-zero cancellation at $z = 0$ in (7) doesn't occur. The modulator then becomes *third* order. In general, if the loop delay causes the DAC pulse to extend beyond T_s, then the modulator order increases by one [4].

A double-integration modulator is known to be unconditionally stable [8], while for third-order modulators, the stability is conditional [9]. In fact, the stability of (5) can be shown qualitatively to worsen with ρ_d using a root locus plot. The circuit is "linearized" by replacing the quantizer as a summer with an independent input e, and the poles of the so-called "noise transfer function"

$$\mathrm{NTF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \tag{8}$$

are plotted as a function of ρ_d [4]. The root locus is shown in Fig. 5; with no delay, the poles of NTF(z) are all at the origin, but as delay increases, they move towards the unit circle. Two of them exit the unit circle at ρ_d=0.31, implying the modulator becomes unstable for 31% delay, though this number isn't accurate because linearizing the circuit is an approximation only. The quantitative effect on performance must be determined through simulation. Fig. 6 is for OSR=32 and a –4 dB input tone, and we see that as loop delay increases, SNR falls. A loop delay of about 100% is found to be needed to make the circuit unstable.

Loop delay is one manifestation of something that makes a CTΔΣM, and specifically the DAC pulse shape, nonideal. Other DAC pulse nonidealities such as finite rise/fall time or single-pole settling are similarly detrimental to SNR, and they have been treated elsewhere [10].

Nonideal DAC pulses can be compensated for by including additional degrees of freedom in the design [4], [10], [11] and some circuitry to tune them [12]. For example, a third

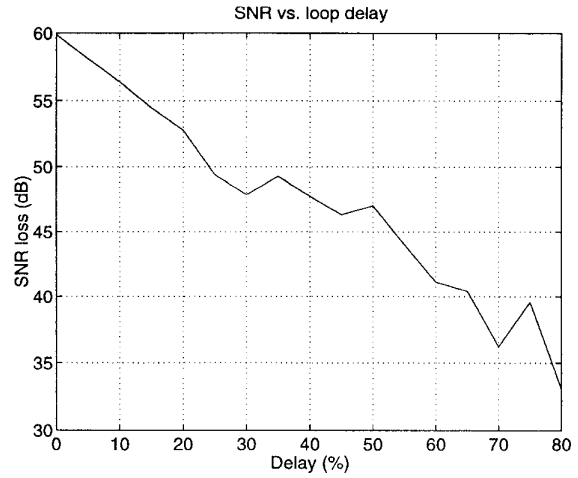

Figure 6: Effect of loop delay on SNR of double integration modulator.

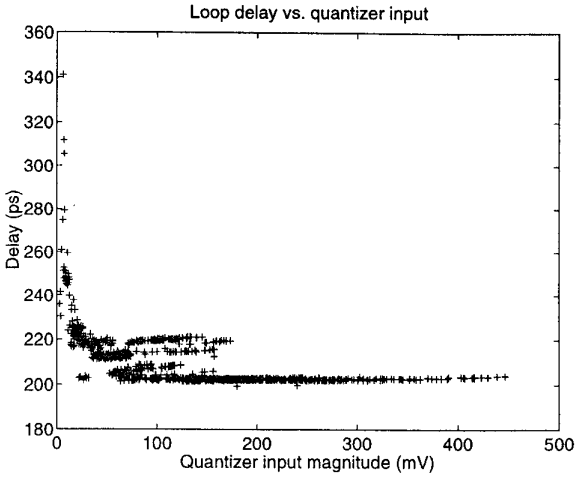

Figure 8: Loop delay versus quantizer input magnitude for a real CTΔΣM.

feedback loop using an RZ DAC pulse could be added to Fig. 1. The price of such compensation is an increase in circuit complexity.

IV. Clock jitter

In a CTΔΣM like the one in Fig. 1, the integral of the DAC current over a clock period determines modulator behavior. This integral varies linearly with timing variations caused by jitter in the quantizer clock. By contrast, in a typical DT (e.g., SC) ΔΣM, the variation due to sampling clock jitter in the amount of charge transferred is small because most of the charge is transferred at the beginning of a clock period. Hence, CT designs are more sensitive to clock jitter than DT designs [13].

The effect of jitter is to add white noise to the output spectrum, which "fills in the noise notch" and lowers SNR. Fig. 7 shows two sets of 1024 averaged 4096-point Hanning-windowed periodograms for the circuit in Fig. 1 clocked at 1GHz, one with no jitter and one with a normally-distributed

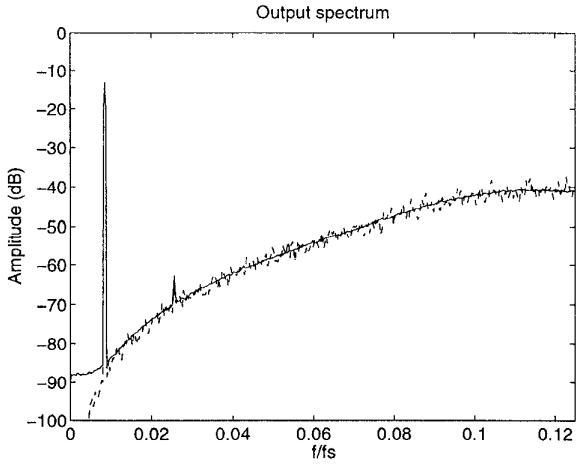

Figure 7: Jittered (solid) and unjittered (dashed) output spectra.

uncorrelated jitter with a standard deviation of 2ps. The simulation was performed using the direct mathematical approach described in [14]. The whitening of the noise floor near dc is clear; the performance of the modulator is degraded because of the higher in-band noise. [13] equation (14) gives an approximate formula for the maximum obtainable SNR when the jitter variance is σ_j^2:

$$\mathrm{SNR}_{\max} = 10\log_{10}\left(\frac{\mathrm{OSR}\cdot T_s^2}{4\sigma_j^2}\right) \tag{9}$$

For OSR=64 in Fig. 7, we find $\mathrm{SNR}_{\max}$ = 69.2 dB measured, and 66.0 dB as calculated by (9), indicating an acceptable agreement. Unjittered $\mathrm{SNR}_{\max}$ is found to be 78.1 dB.

Clock jitter is difficult to combat in CTΔΣMs. Using RZ DAC pulses in place of NRZ doesn't help because the falling edge of the RZ pulse is subject to jitter in the same way the rising edge is, thus leading to a similar variance in charge transferred seen in an NRZ DAC. [15] suggests using "impulse" DAC pulses, where the DACs are somehow charged first, then discharged with the sampling clock — much as is done in a SC design. It is not obvious how to adapt this to very high-speed circuits, however. For now, low-jitter crystal oscillators (or low phase-noise VCOs) and careful layout techniques to avoid substrate coupling, etc., seem to be the only ways to ensure clock jitter won't degrade performance significantly.

V. Signal-Dependent Jitter

Even with a perfectly uniform sampling clock, it is possible for a form of timing jitter to creep into a CTΔΣM like the one in Fig. 1. Usually, the quantizer input signal has a large enough magnitude so that a decision takes a fixed amount of time. However, the quantizer is a real regenerative circuit with finite regeneration gain; quantizer inputs close to zero volts, therefore, will take longer to resolve. Fig. 8 depicts this effect graphically for a transistor-level simulation of the cir-

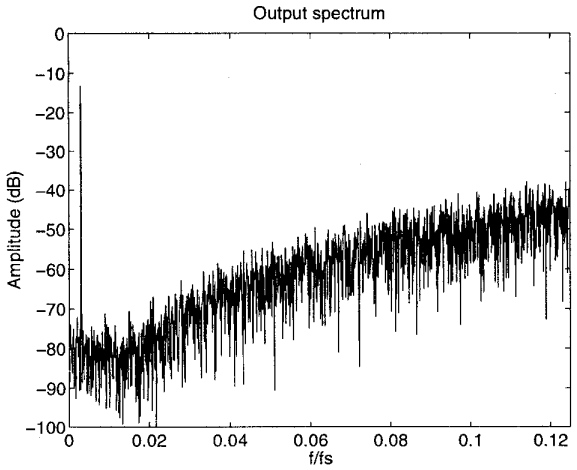

Figure 9: Output spectrum for SPICE transistor-level simulation.

cuit of Fig. 1 in SPICE. Loop delay is normally about 200ps, which is 20% of the clock period, but it begins to rise for quantizer inputs smaller than about 50mV.

Loop delay in a real circuit is thus a variable which depends on the magnitude of the quantizer input. A ΔΣM works to decorrelate the quantizer input x with the overall circuit input u so that x appears "random"; therefore, quantizer inputs close to zero will occur at times that appear random. Finally, then, loop delay will be increased at times that appear random. Changing the loop delay results in a variable amount of DAC charge integrated in a period — exactly the same thing that happens with clock jitter. However, since the variable loop delay is now *signal-controlled* (by x), it is appropriate to denote it as a "signal-dependent jitter" [16]. This is a manifestation of the metastability problem in digital latches.

Its effect is identical to that of clock jitter: adding wideband white noise to the output spectrum and degrading converter resolution. Fig. 9 shows a 16000-point Hanning-windowed spectrum of the output bit stream of the transistor-level SPICE simulation, where the spectral whitening at dc is clear. The magnitude of the whitening could be determined if the signal-dependent jitter variance σ_j^2 were known; in theory, this variance could be found from the pdf of the jitter, which is itself determinable from the combination of the quantizer input pdf and the quantizer delay vs. input voltage magnitude. Work in this area is proceeding.

There are two obvious ways to get around signal-dependent jitter problems. The first is to increase the quantizer gain sufficiently so that fewer inputs will be close enough to zero to cause resolution time to increase. However, quantizer gain can only be increased so far. Adding a preamplifier might help, though at the expense of increasing the fixed loop delay (which we have seen is detrimental to SNR). The second solution is to insert a latch between the quantizer output and the DACs, and to clock this latch (say) half a sample later than the quantizer. This way, the quantizer output has up to half a sample to settle, and now the only problem is avoiding jitter in the latch. But once again, this approach adds loop delay, which is detrimental to SNR. It is possible for signal-dependent jitter to be more deleterious to performance than fixed loop delay, but that depends on the exact circuit architecture.

VI. Conclusions

We have examined how loop delay, clock jitter, and signal-dependent jitter affect the performance of a CTΔΣM, and we have discussed what can be done to remedy these effects. All three effects will tend to become more severe as clock speeds are increased. The high-speed CT modulators published in the literature to date have yet to achieve a resolution comparable to the 12 bits by a commercial non-ΔΣ part at the same output rate of 50MHz [17]; in order for CTΔΣMs to achieve 12-bit resolution at rates of 100MHz and beyond, the issues presented in this paper must be tackled.

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