A 950MHz Second-Order Integrated LC Bandpass ΔΣ Modulator

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Abstract

This paper presents a second-order LC bandpass ΔΣ modulator implemented in a 0.5 μm bipolar process for digitizing RF and high IF signals. It employs an integrated LC resonator with active Q-enhancement and two non-return-to-zero digital-to-analog pulse shaping feedback loops. The modulator test chip achieves a signal-to-noise ratio of 56 dB over a 200 kHz bandwidth for converting a 950 MHz signal, and dissipates 135 mW with a 5-V supply.

Introduction

Digitizing signals early in a receiver, at a high IF or even in the RF stage, makes for flexibility and low component count at the cost of demanding specifications on the analog-to-digital (A/D) converters [1] [2].

In this paper, an integrated second-order LC bandpass ΔΣ modulator (BPΔΣM) implemented in a 0.5 μm bipolar process that converts 950 MHz RF signals with sampling rates of 3.8 GHz is explored. The modulator is built with an active Q-enhanced monolithic LC resonator and non-return-to-zero digital-to-analog (DAC) pulse shaping feedback loops. This modulator is a proof-of-concept prototype, showing a fully monolithic active-LC ΔΣ modulator for the first time, and showing GHz bandpass operation for the first time. A commercial version would probably have higher order and feature multi-bit quantization.

These circuits can be used to digitize IF signals for systems with carriers in the 5-30 GHz range such as LMCS/LMDS ("wireless cable") and wireless LAN. If re-engineered for increased sensitivity, they might even be applied to directly convert RF signals for microcell base stations.

Modulator Architecture and Circuit Design

To approach the speed required for RF direct A/D conversion, a continuous-time technique based on integrated LC resonators is utilized in the work. Fig. 1 shows a block diagram of our second-order LC bandpass ΔΣ modulator. Transconductor G_m translates the input differential voltage to an output differential current which is summed with DAC feedback switching currents and then fed into the differential LC resonators. Transconductor G_q is placed in positive feedback to operate as a negative resistor for compensating the losses in the monolithic inductors. The clocked comparator acts as a signal sampler and one-bit quantizer. The comparator output signal is latched twice (for one full clock delay) for one DAC feedback loop and three times (one and a half clock delays) for another feedback loop before it is used for noise-shaping. Feedback DAC pulse shaping coefficients are adjusted by tuning DAC switching currents to achieve the right noise-shaping transfer function and to compensate time-domain nonidealities [3].

The differential LC tanks plus transconductor G_m and transconductor G_q give a second-order bandpass filter response with Q-enhancement. A multi-tanh doublet using unbalanced series-diode-connected differential pairs proposed in [4] is used to implement G_m for obtaining reasonable linear range with tunability. The ratioed transistors are formed by connecting four transistors in parallel. A diode linearization technique, introduced in [5] to achieve a large linear range and tunability, is adopted here for the implementation of G_q. Fig. 2 shows the circuit schematic of the second-order bandpass filter. The LC filter was designed for a nominal center frequency of 1 GHz in a 0.5 μm bipolar technology. Two identical capacitors are connected in parallel as shown in the figure to keep balanced differential operation. The component values in the design are: L = 7.0 nH and C = 0.55 pF.

The one-bit quantizer shown in Fig. 3 is a clocked comparator which is a conventional master/slave type differential ECL comparator with a preamplifier [6]. The SPICE simulated propagation delay for both rising and falling edges is 130 ps. The conventional one-bit current switching DACs are formed by input emitter followers and simple current steered differential pairs which produce non-return-to-zero pulse waveforms.

Experimental Results

The modulator was implemented in a 0.5 μm double-polysilicon bipolar process with maximum f_t of 25 GHz. Two buffers with 50 Ω termination resistors were designed for the Q-enhanced LC filter and the modulator to test their performance. The implemented-core circuit of the modulator consumes a silicon area of 700x900 μm². The test chip was bonded in a CQFP package with 44 pins. The chip microphotograph is given in Fig. 4.

Fig. 5 shows the measured output bitstream spectrum with a -20 dBm input signal at 950 MHz and a 3.8 GHz clock frequency. The measured signal-to-noise ratio (SNR) is 56 dB over a 200 KHz bandwidth or 45 dB in a 3 MHz bandwidth. Fig. 6 plot& measured signal-to-noise ratio (SNR) and signal-to-noise plus distortion ratio (SNDR) in a bandwidth of 200 kHz as a function of input signal level for an input tone offset from $f_s/4$ by 50 kHz. The operation of the modulator draws a total current of 27 mA from a 5 V supply, of

which the Q-enhanced LC resonator consumes 12 mA.

Conclusion

An integrated second-order LC bandpass AZ modulator implemented in a 0.5 μm bipolar technology has been demonstrated for digitizing 950 MHz RF signals. The modulator chip achieved 9 bit resolution over a 200 kHz bandwidth and consumed 135 mW for a 5 V supply.

Acknowledgment

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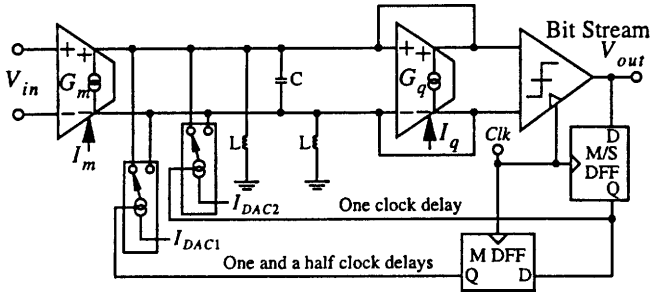

Fig. 1. Block diagram of a second-order LC BPΔΣM.

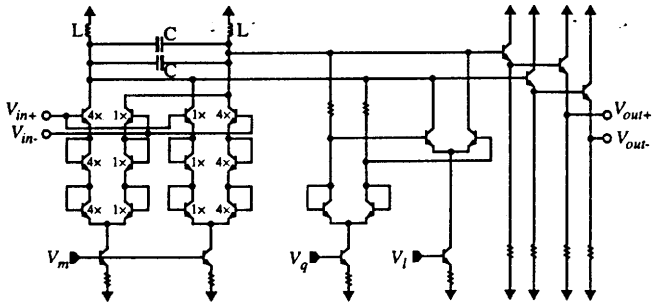

Fig. 2. Linear Q-enhanced LC filterschematic.

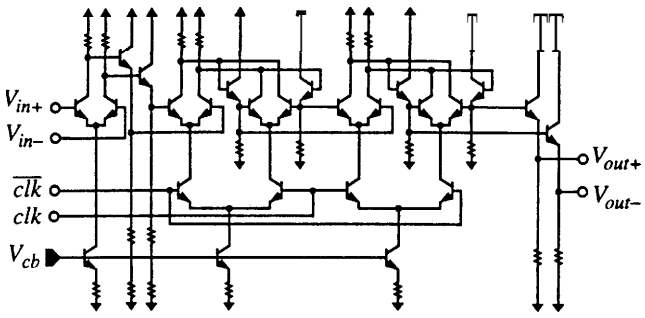

Fig. **3.** Master/slave type ECL clocked comparator.

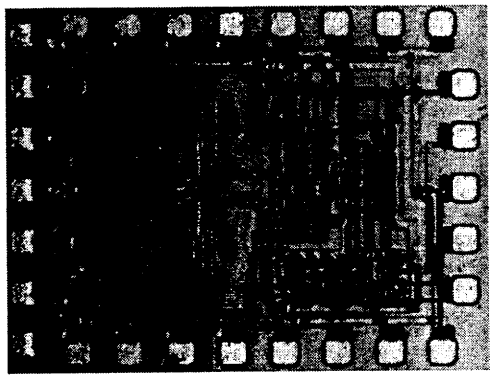

Fig. 4. Modulator die photograph.

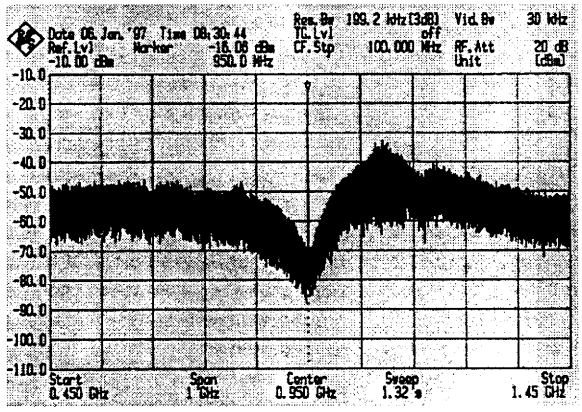

Fig. 5. Measured output spectrum of the modulator.

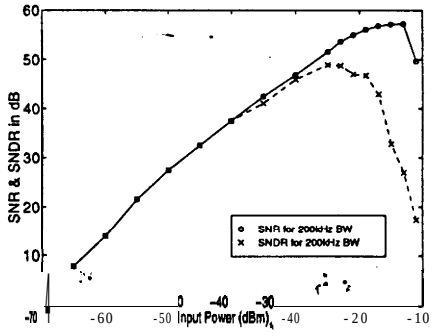

Fig. 6. Measured SNR and SNDR versus input power.