A Bipolar Sampled-Data Bandpass Delta-Sigma A/D Modulator

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Abstract

A second-order bandpass delta-sigma A/D modulator has been implemented in the bipolar subset of a 0.8µm BiCMOS process [10]. This prototype demonstrates the feasibility of a bipolar only delta-sigma modulator based on sampled data techniques. The circuit was clocked at 250 MHz and demonstrated a 40dB SNR in 1 MHz bandwidth for an input signal of 62.5 MHz. The circuit dissipates 350 mW when it operates from a 5V power supply.

Introduction

Digitizing a radio signal at an intermediate frequency (IF) stage of a radio receiver allows quadrature demodulation to be performed digitally eliminating any phase and amplitude imbalance between the in phase (I) and quadrature (Q) channels. Direct conversion at IF is done either by using a wide band video or ΔΣ analog to digital converter (A/D) or bandpass delta-sigma modulator (BP-ΔΣ).

Monolithic BPΔΣ modulators have been reported that digitize signals with a bandwidth up to 200kHz, for use in GSM, IS-54, or similar radio applications. They use switched capacitor (SC) techniques [1],[2] or continuous-time circuits with off-chip inductors as resonators [3]. Increasing demand for wider bandwidth applications requires higher oversampling or higher order design to achieve the required performance. Digitizing at a higher IF is also desirable in order to simplify the radio.

The SC approach has proven to be a very robust and linear technique that has a manufacturing advantage because it does not require any tuning but it has demonstrated limited speed, clocking at 10 to 100MHz. Continuous-time circuits that use G_m-C or LC based resonators are on their way [4] [5] [6]to addressing the need for wider bandwidth A/Ds.

In this paper, we present a second order BPΔΣ modulator. The modulator is designed using only npn bipolar devices. It demonstrates the feasibility and high speed of a sampled-data design style based entirely on a track and hold cell.

Architectures for Bandpass ΣΔ modulator

A second-order modulator is the simplest circuit that demonstrates bandpass operation, and so is useful to test new circuits and structures. It has limited linearity, though enough for radio receivers that include good filtering and low-speed AGC.

The second order ΔΣ bandpass modulator noise transfer function can be derived from the first order lowpass modulator noise transfer function by mapping the zeros of the transfer function form DC to $f_s/4$. This is achieved by a $z^{-1} \rightarrow -z^{-2}$ transformation. The stability and SNR characteristics of the resulting bandpass modulator will be identical to that of low pass prototype [7]. Based on this transformation the noise transfer function of the second-order bandpass ΔΣ modulator is $H_q(z) = (1+z^{-2})/z^{-2}$ and the signal transfer function is $H_s(z) = z^{-2}$.

The z-domain block diagram of the above second order modulator is shown in Figure 1. Note that there are two full delays from input to output and two full delays in the loop, and also note that we never have to sum more than two voltages at any node. This implementation makes possible the use of the 2-operand summer/subtracter cell described in [8] to sum the D/A feedback signal with the loop voltage..

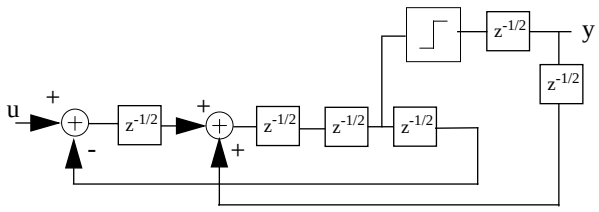

Fig 1. A second order bandpass ΣΔ modulator

Modulator implementation

The basic building block of the modulator is a bipolar track and hold circuit. Any track and hold circuit with a 50% duty cycle holds the sampled data for half of a clock period and therefore introduces half a clock delay. We can represent this action in the z-domain by saying that the track/hold circuit has a transfer function of $T(z) = Az^{-0.5}$ where A is the gain of the track/hold. Because we always use the half-delays in pairs, variation in clock timing from a 50% duty cycle is unimportant.

The modulator in Figure 1 can be implemented by cascading four track/hold circuits in a master-slave configuration.The complete circuit implementation is shown in

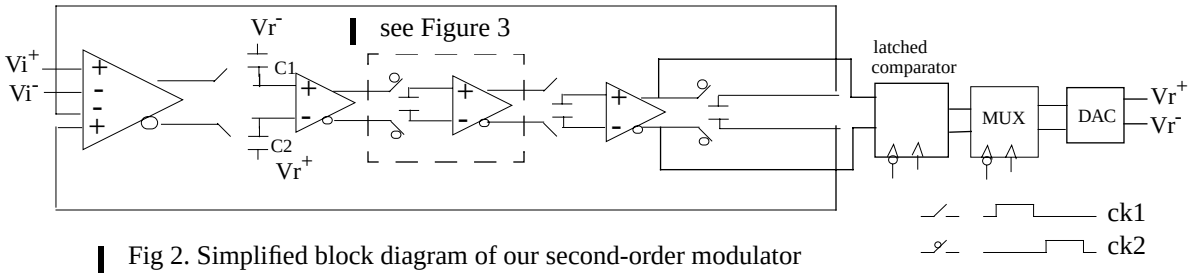

Fig 2. Simplified block diagram of our second-order modulator

Figure 2. For simplicity the track/hold circuits are presented as a pair of switches charging a capacitor followed by an amplifier. The quantizer is a master-slave latch D-type flip-flop providing a full clock delay for the quantizer feedback signal. The quantizer is followed by a multiplexer that controls the one bit DAC. During ck2 it passes the quantizer levels and during ck1 it inverts the quantizer levels. In this way it provides signal levels at the bottom plate of C1 and C2 that add to the loop signal by KVL, thus avoiding the need to sum signals at a virtual ground as is done in switched-C circuits.

The track and hold circuit design

A diode bridge based track/hold circuit was used for this design. The diodes were npn devices that had their bases tied to their collectors. Since the diode bridge is a single-ended circuit and the modulator requires a fully balanced signal a quasi-differential circuit was used (Figure 3), consisting of two bridges followed by a differential output buffer in a unity gain configuration [9].This way we reduce even-order distortion. The track/hold shown corresponds to the switches, sampling capacitor and buffer of Figure 2.

The buffer amplifier for the first stage is augmented with a second input differential pair to sum the input signal onto the first pair of capacitors. This stage limits linearity in the presence of high dv/dt signals and may cause intermodulation between the noise-shaped loop signals and overall input.

The input impedance of the buffer was designed to be fairly high to reduce droop caused by the input current to the output buffer that discharges the hold capacitor. Simulations predicted that the track/hold would have a small-signal bandwidth of 550 MHz and a small- signal gain of -0.5 dB in the hold mode. It also exhibits 8 bits linearity for signals up to 50MHz when clocked at 500 MHz. Its power consumption is 55mW when operated from a 5V power supply.

Summation/substraction implementation

Our $\Delta\Sigma$ implementation emulates the classic SC based designs. In a differential SC approach the number of switches required to perform a summation is eight. Following the same approach would increase the power

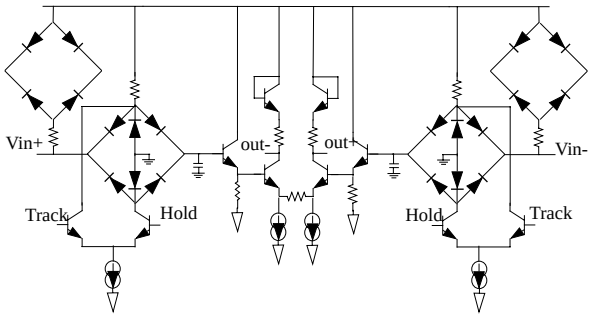

Fig 3. Schematic of the track/hold circuit.

consumption of our design drastically. Instead we prefer to use the SC approach shown in Figure 2 to sum the signal coming from the DAC. Because the DAC signal is balanced and has a set value we do not use any additional switches but we take advantage of the clock phasing by multiplexing back at the bottom plate of capacitor C1 and C2 the right DAC level to perform the summation. This method is not applicable for the loop filter feedback. For this feedback a continues time summation was used. A common emitter differential pair with separate parallel input provides current summation at the load resistors. The differential pair was emitter degenerated to achieve unity gain.

The comparator and the multiplexer are ECL based cells and there design will be discussed in this paper. They were optimized to meet the speed requirements of the modulator while try to minimize their power. Their total power consumption is 64 mW.

Experimental Results

A photomicrograph of the modulator is shown in figure 4. All the bitstreams for the results presented here were captured by a logic analyzer and a Hanning-windoed 32768 point FFT was performed. A typical output spectrum of the modulator when clocked at 250 MHz is shown in figure 5.Figure 6. is in-band plot of the same measurement. Based on this measurement the SNR was 41dB for 1MHz bandwidth

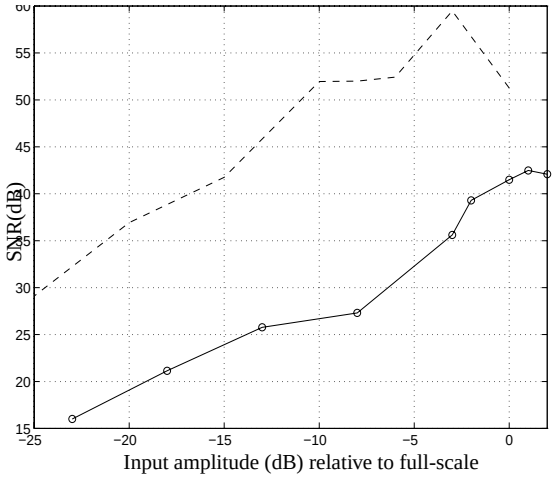

Fig. 7.:SNR for 1MHz bandwidth and a clock frequency of 250MHz.

Fig 4 Photomicrograph of the modulator.

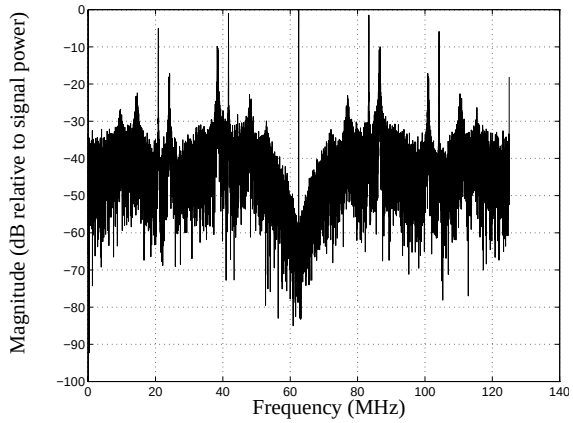

Fig. 5: Output spectrum of the second order bipolar BPΔΣ for a full-scale tone at fs/4. Clock frequency is 250 MHz

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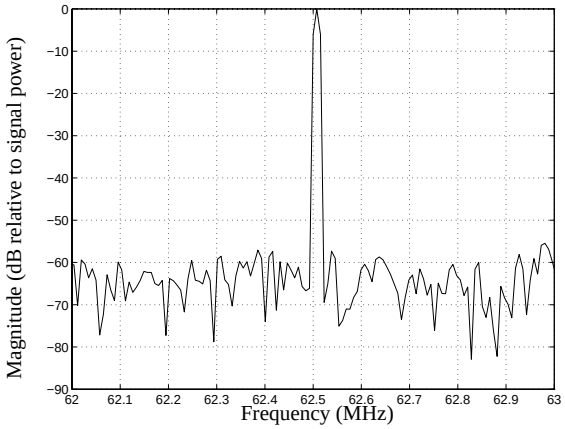

Fig 6.:In-band-plot of Fig 5.The abscissa contains131bins

Various measurements were taken for different input signal levels. The SNR at each signal level is plotted is plotted in figure 7. (solid line) and is compared with the SNR predicted by linear analysis of the second order bandpass sigma-delta modulator (dashed line). The experimental SNR is 20dB lower than what linear theory predicts. As it was noted in section 3.1. the track and hold gain is less than unity that reduces the in-band noise attenuation. Figure 8. plots the SNR predicted by the linear theory versus the percentage of unity gain reduction of the track and hold cell for half-scale tone input at 62.5 MHz for a clock frequency of 250 MHz and a signal bandwidth of 1 MHz.

Fig. 8. SNR (dB) versus percentage of gain reduction of the track/hold

Conclusions

The design and experimental evaluation a fully bipolar second order bandpass delta-sigma modulator were pre-

sented. The prototype design demonstrated the feasibility of bipolar only sampled data ΔΣ modulator. It can be an alternative to continuous time solutions to provide the high oversampling necessary for wide band applications. Because it is a sampled data technique it do not require any tuning to achieve the desired frequency of operation. It is important though to note the sensitive of the structure to the gain of the track and hold cell. Other bipolar track and hold circuits are under evaluation in an effort to provide a unity gain cell. Also, we would like to note that fourth order design would show less total behavior and higher SNR that can make this approach useful for some wide band applications.

Acknowledgments

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References

[1] Lorengo Longo and Bor-Rong Hong, “A 15b 30KHz bandpass sigma-delta modulator”, ISSCC-93 Digest, pp.226-227.

[2] Frank W. Singor and W. Martin Snelgrove, “Switched- capacitor bandpass delta-sigma A/D modulation at 10.7MHZ”, IEEE J. Solid-State Circuits, vol 30, no 3, pp. 184-192, March 1993

[3] G. Troster, et al, “An interpolative bandpass converter on a 1.2 sum BiCMOS analog/digital array”, IEEE J. Solid-State Circuits, vol 28, no. 4, pp. 471-477, April 1993

[4] Omid Shoaei “

[5] W. Gao

[6] J. F. Jensen, G. Raghavan, A.E. Cosand and R,H. Walden “A 3.2GHz second-order delta-sigma modulator Implemented in InP HBT technology” IEEE J. of Solid State Circuits, vol.30, no. 10, October 1995

[7] S. Jantzi, R. Schreier and M. Snelgrove, “The Design of Bandpass Delta-Sigma ADCs,” chapter in Delta-Sigma Data Converters, IEEE Press, to appear.

[8] Seyfi S. Bazarjani, Theodore Varelas and W. Martin Snelgrove, “Sample-and-Hold Based bandpass ΔΣ modulators

[9] Coleran

[10] R. Hadaway et al, “A sub-micron BiCMOS technology for Telecommunications” J. of Microelectronics Engineering, vol.15, pp. 513-516, 1991.