A Low-Power Gm-C-Based CT-ΔΣ Audio-Band ADC in 1.1V 65nm CMOS

Imran Ahmed, James Cherry, Ayaz Hasan, Akram Nafee, David Halupka,
Younis Allasasmeh, Martin Snelgrove
Kapik Integration Toronto, Ontario, Canada

Abstract

A low power CT-ΔΣ is presented which achieves 92dBA of dynamic range while consuming only 110μA from a 1.1V supply in 65nm. The ADC exploits the inherent virtual ground of the ΔΣ loop to enable low power Gm-C integrators, and a simplified excess loop-delay compensation scheme. A common-mode feedback circuit which enables low voltage operation is also presented.

Introduction

Low-power audio ADCs are key building blocks for battery-powered devices. For high-fidelity audio the ADC dynamic range needs to be >85dB in the audible bandwidth (<24kHz). The power dissipation of the ADC is also critical as it directly impacts the battery life. This work presents an audio-band ADC that consumes 121μW and achieves a dynamic range of 92dBA. Power savings are achieved by using the inherent virtual ground of a ΔΣ loop, which also enables the use of simplified excess loop-delay compensation. A low-voltage common-mode-feedback (CMFB) circuit is also presented. The presented ADC achieves a FoM better than most of the state-of-the-art [1]-[4], and the highest for CT-ADCs that can operate directly from a 1.2V battery; making it perfectly suited for battery-powered systems.

Amongst ΔΣ architectures continuous-time (CT) approaches generally achieve lower power than switched-C approaches due to lower noise and bandwidth requirements [5]. Additionally, CT approaches have an inherent anti-aliasing filter, thereby reducing system components and power. In CT-ΔΣ ADCs the first-stage integrator consumes a significant amount of total power, this work proposes a technique to reduce the power of the first-stage integrator, thereby significantly reducing the power consumption of the entire ADC.

Proposed Design

In CT-ΔΣ ADCs either active-RC integrators or Gm-C integrators, as shown in Fig. 1, are commonly used. Active-RC integrators achieve good linearity, but at the expense of additional power required to drive the feedback network with sufficient loop gain and phase margin. Gm-C integrators drive a capacitive load open loop and thus consume less power than active-RC integrators. However, they achieve poor linearity as a result of the large swing present at the input of the Gm cell. Furthermore, the supply voltage of the Gm cell typically limits the maximum allowable swing at its input, restricting the utility of the approach.

A ΔΣ loop is a feedback loop with its own virtual ground at the summation node of the input and feedback DAC. In this work low power is achieved by placing the Gm cell after the summation node as shown in Fig. 1(c). This results in the virtual ground of the ΔΣ loop being at the input of the Gm cell thus minimizing the Gm cell input swing and making it independent of the ADC input swing. The ΔΣ

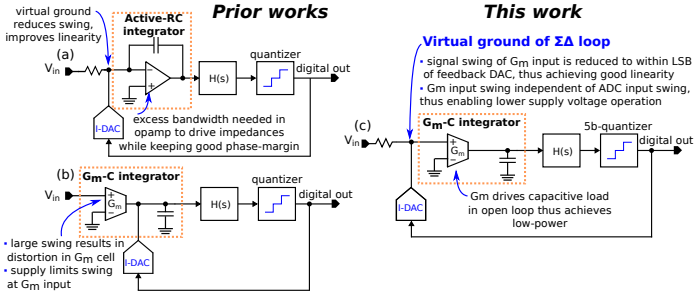

Fig. 1. Integrator implementations for ΔΣ ADCs (a), (b) used in prior-art and (c) this work.

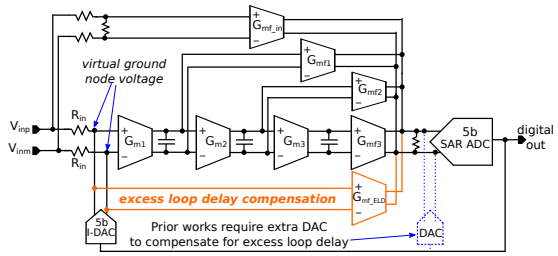

Fig. 2. Excess loop-delay compensation of this work.

loop drives the swing at the input of the Gm cell to be within 0.5LSB of the feedback DAC; hence, with a sufficient number of bits in the feedback DAC, the swing at the input of the Gm cell can be made sufficiently small to achieve the required linearity. Thus by using the virtual ground of the ΔΣ loop, the limitations of the Gm-C approach (poor linearity and limited ADC input swing) are mitigated.

A. Feedback Path

While early implementations of ΔΣ ADCs sought to minimize the number of bits in feedback to avoid DAC nonlinearity and quantizer complexity, dynamic element matching [6] and a SAR-based quantization enable additional bits in the ΔΣ feedback with minimal power; both techniques are employed in this work. For the audio level requirements of this work 5b in the feedback path was sufficient to restrict the swing at the input of the Gm cell to achieve the target linearity from a <1.2V supply-voltage.

B. Feedforward Path

To further relax the linearity requirements of the integrators in the ΔΣ loop, a feed-forward architecture was used as shown in Fig. 2. Excess loop delay (due to finite integrator bandwidths and quantizer delay) is typically compensated using an additional feedback DAC [5] as shown by the dashed lines in Fig. 2. An additional advantage of the architecture used in this work is that the compensation path can alternatively be realized by feeding the virtual ground node of the ΔΣ loop (appropriately scaled) to the quantizer input as shown in Fig. 2. This method is not applicable to prior approaches, Fig. 1 (a) and (b), as the virtual ground of the

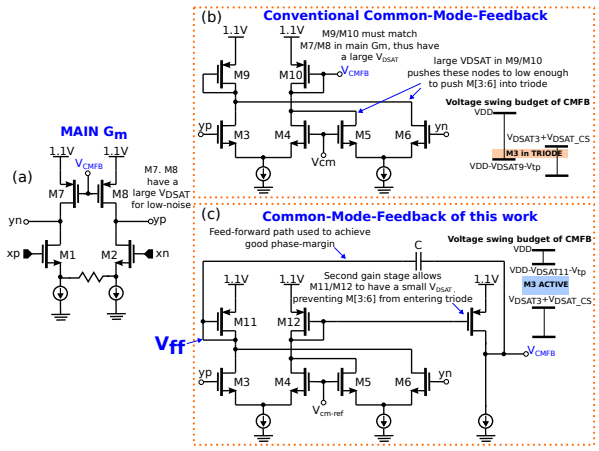

Fig. 3. The (a) Gm cell integrators, with (b) prior CMFB and, (c) the low-voltage low-noise approach used in this work.

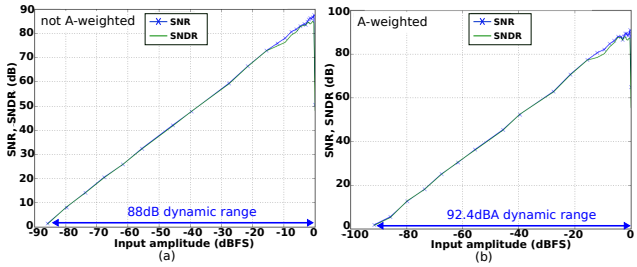

Fig. 4. Dynamic range and SFDR plots of the ADC.

$\Delta\Sigma$ loop is represented as a current, thus making it difficult to utilize its scaled quantity for excess loop delay compensation and necessitating the use of an extra DAC to provide compensation. In this work, the input resistance (Rin in Fig. 2) converts the virtual ground current into a voltage, which can be readily used to drive a Gm cell without the use of an extra DAC. Compensation is realized using the same Gm cell that is used to implement the feed-forward terms of the $\Delta\Sigma$ loop (with suitably modified Gm value).

C. Common Mode Feedback

Fig. 3(a) shows the source-degenerated Gm cell used in this work. To achieve low noise, transistors M7 and M8 are sized to have a large VDSAT. The commonly used CMFB circuit of Fig. 3(b) uses a low-gain single-stage amplifier (to maintain phase-margin) where the CMFB circuit relies on M9 and M10 to have the same VDSAT as M7 and M8 in the main Gm cell. As a result, if M7 and M8 are sized with a large VDSAT for low-noise, M9 and M10 also have a large VDSAT. However, in the presence of a low supply voltage, increasing the VDSAT of M9 and M10 pushes the differential pairs M3-M6 into triode. To enable low-voltage and low-noise operation of the main Gm, the CMFB approach of Fig. 3(c) was used. A second gain stage was added to the CMFB circuit to decouple the symmetry requirement between M7/M8 and M9/M10, enabling M11/M12 to have a much smaller VDSAT compared to M9/M10, thus enabling operation with a lower supply voltage. To compensate for the pole produced by the second gain stage a feed-forward zero is added. As shown in Fig. 3(c) the feed-forward path can be readily realized by capacitively feeding node Vff to the CMFB output.

Measured Results

The prototype is fabricated in a 65nm CMOS process with an area of 1.2mm x 0.5mm: including all reference buffers, biasing, and generously sized decoupling capacitors. The effective sampling rate of the ADC is 3.072MHz, and the input signal bandwidth is 24kHz. The ADC achieves a dynamic range of 88dB/92dBA, and peak SNDR of 85dB/89dBA as shown in Fig. 4(a) and 4(b). The full scale input voltage of the ADC is 600mVp-diff thus enabling the ADC to be interfaced to sensitive input sources (i.e. microphone) with little or no preamp gain. The current consumption of the entire modulator including all reference voltages and biasing currents is only 110μA from a 1.1V supply. The output spectra of the modulator with single and two-tone inputs are shown in Fig. 5(a), (b), and (c). The ADC of this work achieves a FoM [5] of 171dB, placing it amongst the most power efficient ADCs for its sampling rate and resolution, with the benefit of lower supply operation and smaller technology node. Fig. 6 shows comparison of this work to prior-art.

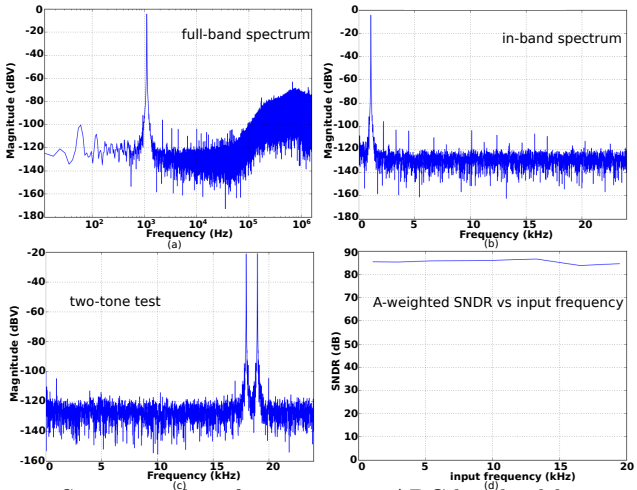

Fig. 5. Spectra and performance over ADC bandwidth.

Measurement	This work	[1]	[2]	[3]	[4]
Power	121µW	28.6µW	140µW	455µW	1200 µW
Dynamic range	88dB/92dBA	82dB	88dB	92dBA	92dB
Peak SNDR	85dB/89dBA	79dB	84dB	85dBA	77dB
Input bandwidth	24kHz	20kHz	100kHz	22kHz	20kHz
Input swing	0.6$V_{p\text{-}diff}$	0.6$V_{p\text{-}diff}$	1.5$V_{p\text{-}diff}$	1$V_{p\text{-}diff}$	-
Supply voltage	1.1V	0.6V	1.5V	1.3V	1.1V
Technology	65nm	130nm	180nm	130nm	45nm
FoM	171dB	170dB	177dB	169dBA	164dB
Architecture	CT	CT	DT	CT	CT

Fig. 6. Summary and comparison of key measurements.

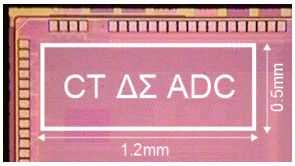

Fig. 7. Chip micrograph.

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