A Simple Implanted Backgate MOSFET. for Dynamic Threshold Control in Fully-Depleted SO1 CMOS

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INTRODUCTION

RecentIy Yang et al have reported a fully-depleted SOIAS MOSFET structure in which an oxide-isolated polysilicon backgate electrode is formed beneath the channel [l]. The device threshold voltage can be modulated by biasing this electrode. In this way the benefits of dynamic threshold adjustment in response to process variations, changes in temperature and operating requirements demonstrated for bulk CMOS ICs using ≈ 1 V power supplies [2] can be extended to fully-depleted SO1 technology, which offers inherent advantages of reduced source/drain capacitance and near-ideal subthreshold swing. This paper reports fabrication and testing of a very simple new backgated FD-SO1 MOSFBT structure that can also provide dynamic thresholdcontroL

DEVICE STRUCTURE

Fig. 1 shows a new SO1 MOSFBT structure in which a backgate electrode is formed by high-energy boron implantation through the silicon film and buried oxide into a lightly-doped n-type substrate. The backgate electrodes can be junction isolated by connecting the substrate to the most positive circuit potential, allowing different backgate biases V_B to be applied to n- and p-channel devices, or to different groups of devices. For example, V_{Tn} and $|V_{Tp}|$ could be raised in selected parts of an IC to lower power dissipation at the expense of reduced speed. (A structure similar to Fig 1 in which an implanted n-well was placed beneath p-channel transistors in thin buried oxide SO1 in order to enhance current drive and reduce parasitic capacitance was reported very recently by Yoshino et al [3], but no consideration was given to dynamic threshold control).

DEVICE FABRICATION

Prototype n-channel MOSFETs with implanted buried backgate electrodes were fabricated on 4 Ωcm SIMOX substrates with a buried oxide thickness of 360 nm and nominal post-process silicon film thicknesses of SO nm, appropriate values for a 1 μm gate length technology generation. Following device well isolation by mesa etching, backgate electrodes were formed by masked implantation of $^{11}B^{++}$ at a dose of $2x10^{13}$ cm^{-2} and ion energy of 300 keV. Fig. 2 shows the doping profile predicted by SUPREM3 simulation for this implant, along with actual SRP data for a bulk test wafer. It is apparent that a backgate electrode with boron concentration near 10^{18} cm^{-3} can be produced while leaving a residual backscattered boron concentration far below typical well doping levels in the silicon film. Here a 10 keV $5x10^{11}$ cm^{-2} $^{11}B^{+}$ implant was used to give a p-well doping (predicted by SUPREM3) of $4x10^{16}$ cm^{-3}. Following growth of a 25 nm gate oxide, a 10 min 1100'C anneal was used to raise the boron concentration at the interface between the backgate electrode and the buried oxide (Fig. 2). Processing was completed by deposition and patterning of polysilicon gate electrodes, doping of source, drain and gate regions by phosphorus diffusion, and application of a simple SLM aluminummetallization.

ELECTRICAL CHARACTERIZATION

Subthreshold characteristics for a backgated MOSFET are shown in Fig. 3, while V_T values obtained by extrapolation from the linear region of the I_D-V_{GS} characteristic are listed in Table 1. At $V_B=0$ the subthreshold swing is 66 mV/decade and $\Delta V_T/\Delta V_B$ is 90 mV/V, in good agreement with SIJPREM3 predictions, while V_T is slightly below the nominal target of 0.2 V. Leakage between the backgate electrode and the substrate was typically less than 30 nAcm^{-2} at 5 V reverse bias, compatible with backgate biasing using an on-chip charge pump. Fig. 4 shows the effect of backgating on the drain characteristics.

SUPREM3 predicts that it should be possible to control the threshold voltage of pMOSFETs by backgating in the same manner as for nMOSFETs, with similar sensitivity. Fabrication of CMOS test circuits including FD pMOSFETs with p^+ poly front gates and implanted p-type backgate electrodes is underway. Simulation also predicts that the implanted backgate structure can still provide effective V_T control as gate oxide, buried oxide and silicon film thicknesses are scaled to values appropriate for the 035 μm technology generation.

CIRCUIT APPLICATION

SOISPICE simulation was used to investigate the abiity of the structure of fig. 1 to provide a useful range of V_T adjustment for values of V_B attainable with an on-chip CMOS charge pump for 1 V power supply operation. The design of Dickson [4] was used to maximize pump output for low supply voltage. SOISPICE predicts that V_B values sufficient to restore V_{Tn} to the nominal 0.2 V target for initial values differing by as much as ± 0.25 V from this target can be generated. **Analogous results** apply to V_{Tp} adjustment.

CONCLUSION

It has been shown that a simple implanted backgate electrode can provide effective dynamic control of V_T in FD-SOI MOSFETs. SOISPICE simulation indicates the new structure should be useful for 1 V supply CMOS.

REFERENCES

1. I. Y. Yang et al, Tech. Dig. IEDM'95, pp. 877.
2. J.B. Burr et al Tech. Dig. 1994 IEEE Solid State Circuit Conf., p 84.
3. A. Yoshino et al, ***IEEE Electron Dev. Lett,*** EDL-17 p.106 (1996).
4. J.F. Dickson, ***IEEE J. Solid-State Circuits*** SC-11, p. 374 (1974).

Table 1 Threshold voltage dependence on backgate bii.

V_B (V)	V_T (V)
2	-0.20
1	-0.09
a	0.00
-1	0.09
-2	0.18

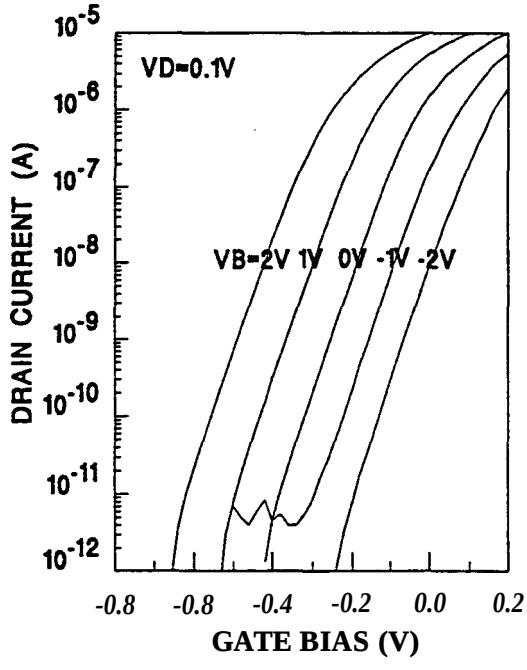

Fig., 3 Subthreshold characteristics for backgated SO1 MOSFET. W = 25 μm, L = 5 μm.

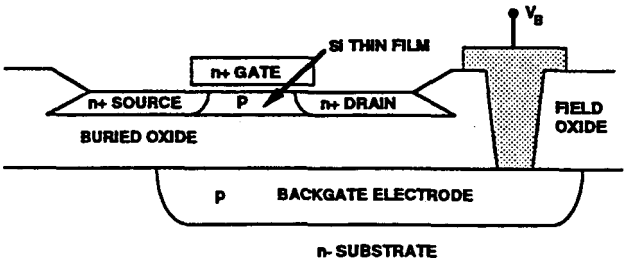

Fig. 1 Cross-section of SO1 MOSFET with implanted backgate electrode.

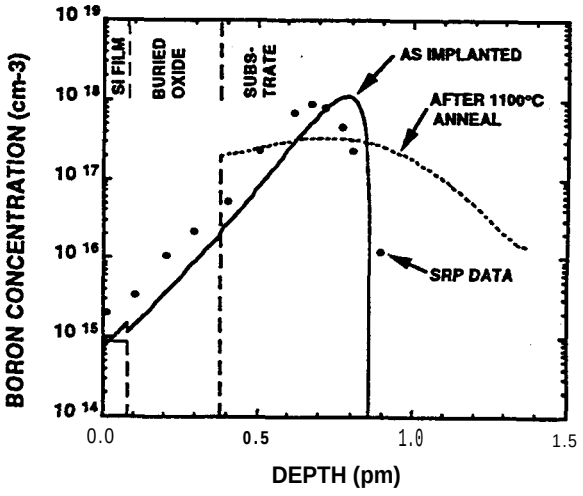

Fig. 2 Doping profile predicted by SUPREM3 for backgate electrode implant both as-implanted and after 1100 C drive-in Dots show SRP data from bulk test wafer with RTA implant activation.

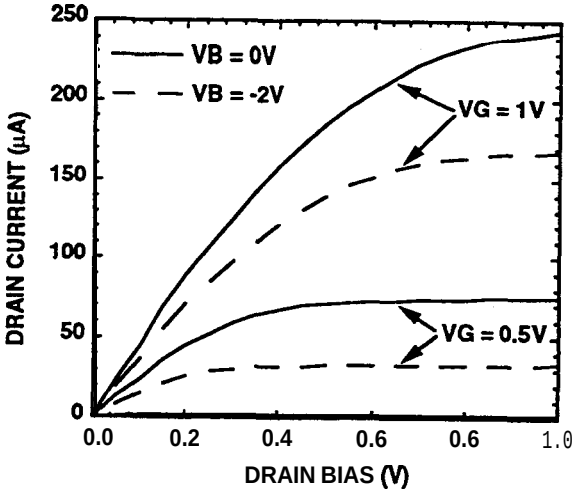

Fig. 4 Drain characteristics for device of **Fig. *3.***