A Monolithic Complex Sigma-Delta Modulator for Digital Radio

Ashok Swaminathan', Martin Snelgrove', Steve Jantzi2, and Seyfi Bazarjanil

'Department of Electronics, Carleton University, Ottawa, Canada KlS 5B6

*Department of Electrical Engineering, University of Toronto, Toronto, Ontario M5S 3G4

'swami@doe.carleton.ca

*steve@eecg.toronto.edu

Abstract

An architecture for a 1.9 GHz PCS receiver is described. This architecture uses a single IF and a Complex Bandpass Sigma-Delta Modulator (BPΣΔM) to digitize the signal at the IF. This demonstrates the feasibility of this type of modulator in I/Q radios. Image rejection is then done inDSI? A fourth order ΣΔ modulator has been realized in a 0.8um BiCMOS process for the receiver. The modulator is clocked at 4MHz, with a SNR of 48dB for an oversampling ratio (OSR) of 200 and has a power dissipation of 15OmW with a 5V supply.

I. Introduction

For the next generation cellular phones, designing high performance receivers with low power dissipation and component count will be critical. For most conventional radios, a super-heterodyne (two or more intermediate frequencies (IF's)) architecture is used [l]. At each IF mixing stage, however, unwanted image signals can be aliased into the desired signal, resulting in a need for image rejection at each stage. If a direct conversion architecture [2] is used image rejection is no longer a problem, however; l/f noise, DC offset, electro-magnetic interference (EMI), and even-order harmonic distortion becomes a concern. On top of this, the receiver has to meet certain wireless specifications, such as 8OdB dynamic range, interferers at +65dB, and minimal power consumption.

To meet these specifications, a single-IF radio is described (see fig. 1) similar to the architecture proposed in previous literature [3][4]. The IF is high enough to filter out some of the image with a relaxed filter. Image rejection is done with digital signal processing (DSP). The radio operates at an RF of 1.9 GHz and at an IF of 60 MHz. Furthermore, complex filtering and A/D conversion is done on the received signal. This way, the image-reject requirements can be split 35dB/35dB between analog filtering and DSP.

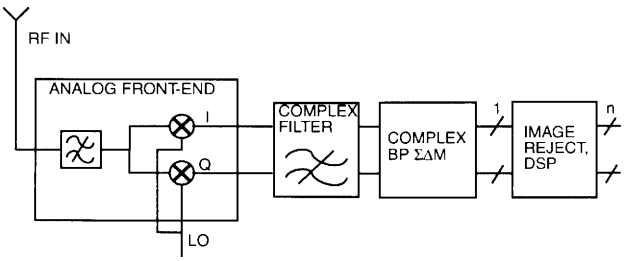

Fig. l: Receiver Block Diagram

II. Complex Filtering

Most filters have transfer functions that contain conjugate poles and zeros because they use real coefficients. A complex filter can be designed that has non-conjugate poles and zeros which takes a complex-valued input and gives a complex-valued output [6][7][8]. This makes it particularly useful for I/Q (real/imaginary) radio applications.

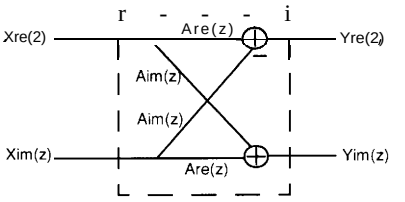

Fig. 2: Complex Filter Block Diagram

Even though the filter transfer function (TF) is complex, it can be constructed from cross-coupled real filters [3], for the real and imaginary parts of the filter TF as is shown in fig, 2. Typically the two parts of the TF have the same general structure (poles) so they can share much of the same hardware.

III. Complex ΣΔ Modulation

A bandpass ΣΔ modulator consists of a filter and a quantizer embedded in a feedback loop [9][lo] in order to shape A/D quantization noise out of the desired band of interest. By replacing this filter with a complex filter ~31~41~111~ we can realize an asymmetric frequency response (see fig. 3).

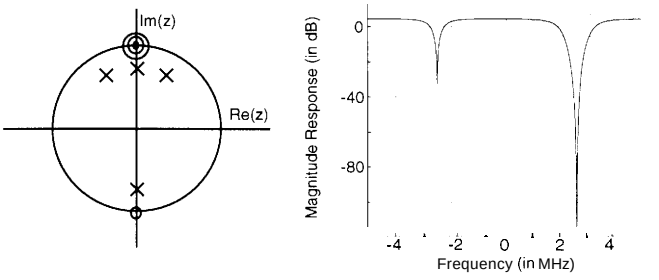

Fig. 3: NTF and Resulting Frequency Response

The modulator gains a bandwidth and SNR advantage over its real counterparts because of the extra noise transfer function (NTF) zero in its passband. It also gains

a stability advantage over a real modulator since a 6th order real modulator (with higher out of band gain) is needed to realize the same response as the 4th order modulator outlined above. This modulator can be easily realized by rotating the poles and zeros of a lowpass-equivalent in the Z-domain. However, the pole and zero placement must be carefully considered, because this transformation does not guarantee stability.

IV. Modulator Architecture

The modulator was designed by empirically choosing the NTF and signal transfer function (STF) so that the stability guideline of approximately 4dB out-of-band NTF gain was met [9]. Also, the coefficients were chosen so that after scaling, the ratio between coefficients was minimized. The poles and zeros of the modulator were:

$$Poles = \pm 0.2 + 0.7j, +\text{-}O.8j$$

$$NTF_{zeros} = j(3), -j$$

$$STF_{zeros} = 0.8j$$

This yielded an out-of-band NTF gain of 4.5dB, an inband STF gain of 6dB, and a maximum ratio between coefficients of 2.5:l. The architecture was based on delay-cells [l0], rather than a cascade-of-integrators [3][9] and is shown in fig. 4. This was chosen for two reasons: speed (less capacitive load to drive); and simplicity (less coefficients). There are inherent drawbacks to this structure however, namely low opamp gain causes worse performance than with integrators, but this problem is insignificant at gains of 6OdB, which is reasonably easy to achieve,

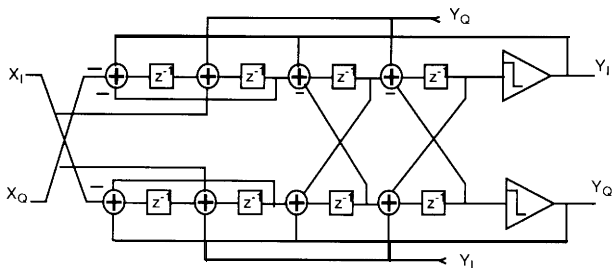

Fig. 4: Z-Domain Block Diagram

A fully differential switched-C implementation was used for the modulator design. The design used a telescopic cascode opamp with continuous-time common mode feedback[l4]. The gain of the opamp was 66dB (simulated), and the unity-gain frequency was 55OMHz. The opamp was simulated with a 1pF load, and was found to settle to 0.1% in less than 3.5ns. A switched capacitor version of the delay cell used can be seen in fig. 5 below (single-ended).

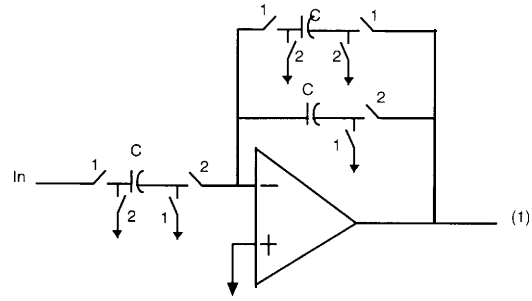

Fig. 5: Switched-C Delay Cell

V. Simulation Results

The modulator was simulated in SPECTRE, a mixed-mode simulator and the results are shown in fig. 6 for a 2048 pt. FFT. Over a 200kHz bandwidth (for a 1/4 scale input relative to the feedback voltage), the SNR of the modulator is 7OdB, sampling at 1OMHz; and 49dB, sampling at 8OMHz. This degradation is due to the settling time of the opamps. Because of the cross-coupling in the switched-C filter, the opamps have more capacitive loading than typical bandpass structures [10].

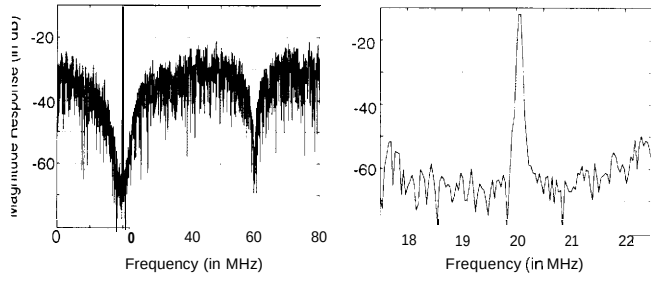

Fig. 6: Simulated Output Response - whole-band and inband

VI. Layout Considerations

This circuit was fabricated in a 0.8μm BiCMOS process, with triple-level metal and metal-metal capacitors. For the small unit sizes chosen (15OfF), the capacitors did not offer the same quality of matching as typical double poly capacitors, so matching techniques needed to be employed (common centroid geometries, Perimeter/Area ratio conservation [12]). Typical capacitor matching was

found experimentally to be about 0.6% for minimum-spaced capacitors. The layout of the modulator is shown in fig. 7.

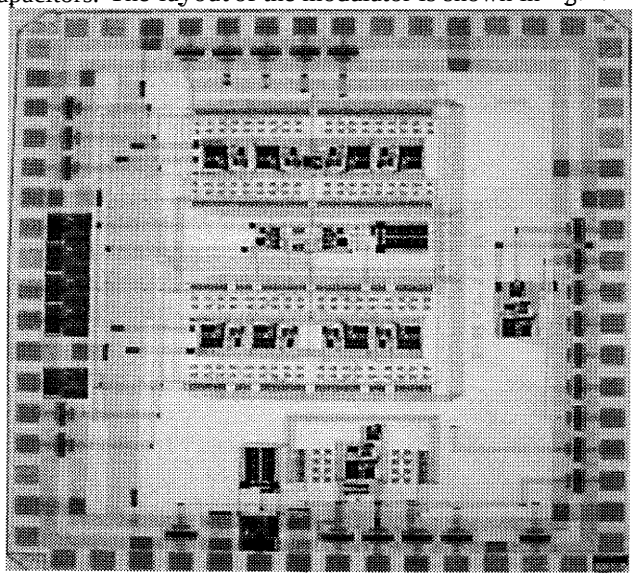

Fig. 7: 0.8µm BiCMOS Complex ΣΔ

VII. Matching Issues

In any complex system, channel mismatch becomes a problem because gain or phase imbalances cause the complex conjugate of the frequency response (or image frequency) to be aliased into the passband of the signal. This can be disastrous for a ΣΔ modulator, where the quantization noise at the image gets aliased inband. One technique to deal with this effect is to place a NTF zero at the image frequency [4]. The image noise is parially shaped, so it has less of an effect on the passband of the modulator. However, this does not have any effect on the image interferer that exists at that frequency. The effect of random coefficient mismatches on the designed modulator is shown in fig. 8 (8OMHz sampling, IMHz bandwidth, averaged over 10 modulators for a 16384 pt. FFT).

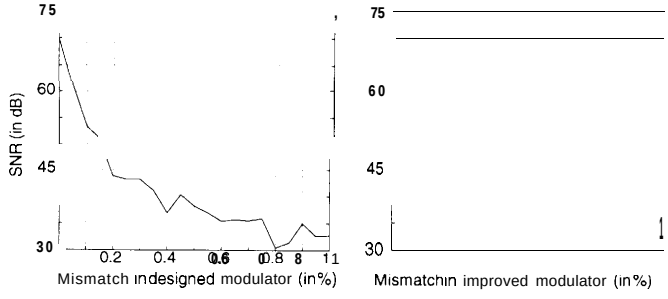

Fig. 8: SNR vs. Random coefficient mismatches

This is mainly due to the fact that the most sensitive coefficients happen to be the cross coupling in the complex-biquad section. In a complex system, any mismatch in the first stages tends to be filtered by later stages, so therefore, mismatch in the later stages tends to be more of a problem in the SNR [4]. One way to get around this is to put the most mismatch-sensitive section in the first stage of the modulator. This way, any mismatch in the first stage will be noise shaped by the second stage (which should be fairly mismatch insensitive). The results for mismatch in a modulator with the same STF and NTF and with the complex section at the beginning are shown in figure 8. As we can see, the modulator is much more insensitive to mismatch, and therefore gains a 35dB (-6 bit) improvement over the designed modulator.

These results lead us to believe that further compensation is necessary to make this designed modulator feasible. An additional method to reduce the degradation is to compensate for it with DSP. One possible method of implementing this is to use an adaptive LMS-tap filter [131 to estimate the effect of the image aliasing, and subtract it from the modulator output. An architecture for this is shown in fig. 9.

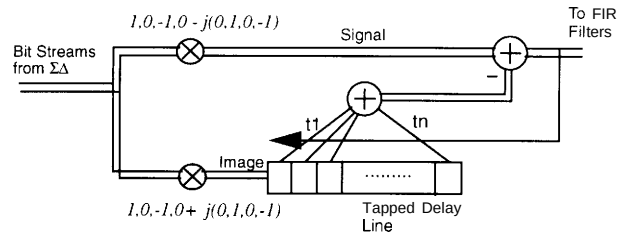

Fig. 9: DSP Solution to Channel Mismatch

This has the advantage that it also compensates for the image interferer signal, as well as image noise that is aliased inband. In fact, by using this method, it is possible that this may make the image notch unecessary, and therefore we can get better inband response from the same order modulator.

VIII. Experimental Results

Shown in figure 10 is the output spectrum for the monolithic modulator, sampling at 4MHz, with an input tone -6dB of full scale. The power dissipated is 200mW and the SNR in a 1OkHz bandwidth (which has the same oversampling ratio as a 200kHz bandwidth for a sampling rate of 8OMHz) is 48dB.

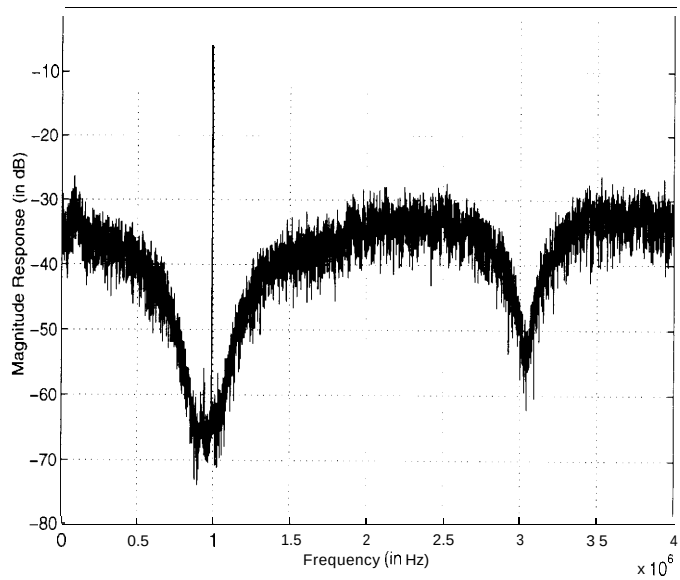

Fig. 10: Output Response (sampling at 4MHz with -6dB input)

These results seem to be less than simulations (by 22dB). This can be explained, as was stated before, by the mismatch between the I and Q channels in the circuit. And as seen in fig. 8, typical capacitor mismatches of 0.6% can result in 35dB SNR reduction! However, even with the SNR degradation, the modulator still exhibits wider bandwidths than a comparable real ΣΔ, which makes it ideal for wideband mobile standards like Qualcomm CDMA or DECT.

At 8OMHz, we can see in figure 11 that the maximum SNR is 32dB (5 bits). The simulations showed that an SNR degradation of 21dB was to be expected between *low* and high frequency operation because of opamp settling time. Our degradation is only 16 dB, because slightly higher bias currents were used in order to increase the opamp output current drive.

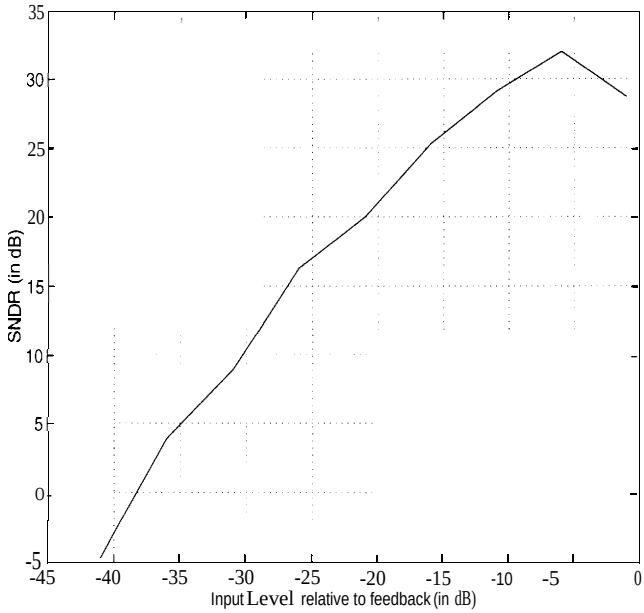

Fig. 1 I: SNDR vs. Input

IX. Conclusions

A single-IF receiver architecture for PCS radio has been described. The receiver contains the first reported implementation of a fourth order Complex BP ΣΔM. This type of modulator can convert I/Q signals and yield wider bandwidths than a real-valued equivalent.

X. Acknowledgements

This work was financed in part by NSERC, as well as by Micronet, a federally funded network of centres of excellence. The test board was designed by Phil Lauzon. I would also like to thank Theo Varelas and Philsar Electronics for valuable input on the design and testing. The ΣΔM was designed at Philsar Electronics, an IC design house in Ottawa, Ontario who also provided technology access to the 0.8μm process. The process was provided by IBM.

XI. References

[1] Krauss, H. L. *Solid-State Radio Engineering.* Wiley, 1980.

[2] G. Schultes et al. "Basic Performance of a Direct-Conversion DECT Receiver." *Electronics Letters*, vol.26 no. 2 1, pg. 1746- 1748, Oct. 1990

[3]S. Jantzi et al. "Complex Bandpass ΣΔ Converter for Digital Radio." *Proceedings of the 1994 IEEE ISCAS*, vol.5, pg.453, May1994.

[4]S. Jantzi et al. "The Effects of Mismatch in Complex Bandpass ΣΔ Modulators." *Proceedings of the ISCAS* 1996, pg. 227, May 1996.

[5] C. Marshall et al. "A 2.7V GSM Tranceiver ICs with On-Chip Filtering." *Proceedings of the 1995 IEEE ISSCC*, pg. 148, 1995.

[6] Q. L. Liu et. al. "Switched-Capacitor Implementation of Complex Filters." *Proceedings of the* 1986 *IEEE ISCAS*, vol. 3, pg. 1121, May, 1986

[7] R. Allen. "Complex Analog Filters Obtained from Shifted Lowpass Prototypes" MaSC Thesis, University of Toronto, 1985.

[8] W. M. Snelgrove. "Intermediate-Function Synthesis" PhD Thesis, University of Toronto, 1982.

[9] S. Jantzi et al. "A Fourth-Order Bandpass Sigma-Delta Modulator." *IEEE Journal of Solid-State Circuits*, vol. *28*, no. 3, pg. 282-291, March, 1993.

[10] L. Longo et al. "A 15b 30kHz Bandpass Sigma-Delta Modulator." *Proceedings of the 1993 IEEE ISSCC*, vol. 1, pg. 226, Feb, 1993.

[111 P. Aziz et al. "Performance of Complex Noise Transfer Functions in Bandpass and Multi Band Sigma Delta Systems." *Proceedings of the* 1995 *IEEE ISCAS*, vol. 1, pg. 641, May, 1995.

[121 R. Gregorian & G.C. Temes. *Analog IkfOS Integrated Circuits for Signal Processing.*Wiley, 1986.

[13] B. Widrow et al. *Adaptive Signal Processing.* Prentice-Hall, 1985.

[14] ??? (can't find the Tsividis Reference to Opamps! !)