# A CMOS BIQUAD AT VHF

Martin Snelgrove and Ayal Shoval
Dept Electrical Engineering
University of Toronto
Toronto, Ontario, Canada M5S lA4
(416)-978-4185

## Abstract

A differential transconductance-C biquad implemented in the digital subset of a 0.9μ CMOS process operates at frequencies up to 45OMHz and Q-factors to approximately 100 with SNR in the range 35-45dB. By switching in capacitors and adjusting control voltages it can be tuned to below 3OMHz. demonstrating the capability of operating over the entire VHF range. Active area is $0.029mm^2$ and power consumption is 30mW.

## Introduction

Several competing circuit technologies are available for implementing monolithic filters: active-RCl , MOSFET-C[2], switched-C[3,4], transconductance-C[5] and digital.[6] The diiferent characteristics of each defines its applications niches, and in new technologies it is generally appropriate to test the capabilities of the circuit styles in their areas of natural strength. We have developed and tested a chip to test the high-frequency limits of transconductance-C (Cm-C) filters in submicron CMOS.

Because transconductance-C filters use an integrator built from an open-loop transconductance amplifier driving a capacitive load they can be very fast (no compensation capacitors axe needed) but should not be expected to be very linear (linearizing circuits exist, but provide limited improvement in linearity and often compromise speed). At high speeds they tend to store state variables on small capacitors and therefore suffer large ***kT I C*** noise: this combines with their nonlinearity to limit their useful dynamic range.

The most natural applications for these filters are therefore those where speed is vital and low or moderate SNR acceptable, for example pulse-shaping and equalization for very high-speed data communications. For these reasons we chose to investigate the capabilities of $G_m$-C circuits in modem CMOS by emphasizing speed. Linearity, power consumption and area were considered only insofar as they did not seriously compromise high-frequency performance, but were all quite reasonable in the fmal design.

Placing the highest priority on speed implies use of minimum-length devices run at high gate-source voltages, and selects for simple circuits to eliminate parasitic poles. The single low (5V) supply voltage further discourages complex circuits, since even cascades quickIy consume all available bias headroom. In this sense the requirement of high operating frequency tends automatically to produce small areas.

## Linearized Transconductors

Figure 1 shows the use of a simple differential pair as a transconductor. Well-known circuits for large-signal linear rransconductors exist.[7,8,9,10] Figure 2 shows the circuit we use, which is simply a differential pair without the current source and is large-signal linear under the same conditions as the others. A similar block was recently reported.[11] The linearized circuits operate by cancelling the quadratic components of the drain currents of two devices, and are exactly linear when devices are exactly described by the long-channel pinch-off model.

$$i_D = K\frac{W}{L}(v_{GS} - V_T)^2 \tag{1}$$

Thus if the inputs consist of a differential signal superimposed on a common-mode bias voltage, $V_{CM} \pm v_d/2$, and M3 and M4 implement an ideal current mirror. then

$$i_o = K_1\frac{W_1}{L_1}\left(V_{CM} + \frac{v_d}{2} - V_T\right)^2 - K_2\frac{W_2}{L_2}\left(V_{CM} - \frac{v_d}{2} - V_T\right)^2 \tag{2}$$

and when the two transistors are identical $(K_1 = K_2, W_1 = W_2, L_1 = L_2)$,

$$i_o = 2K\frac{W}{L}(V_{CM} - V_T)v_d \tag{3}$$

which is linear in the signal voltage $v_d$.

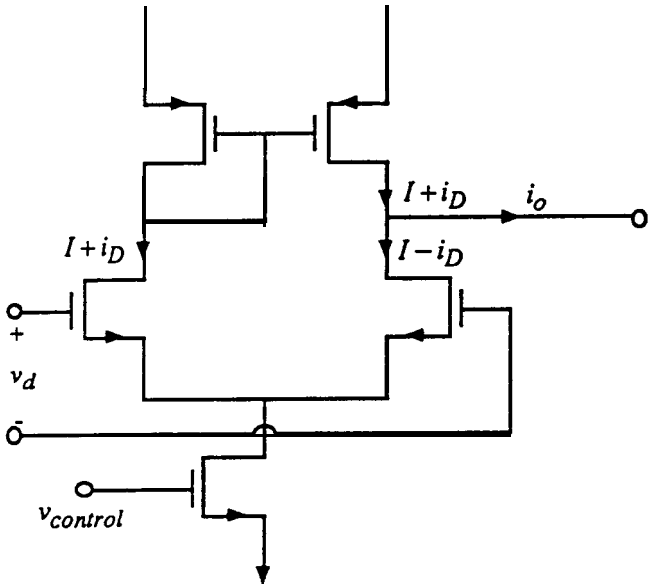


Figure 1: A differential pair as a uansconductor.

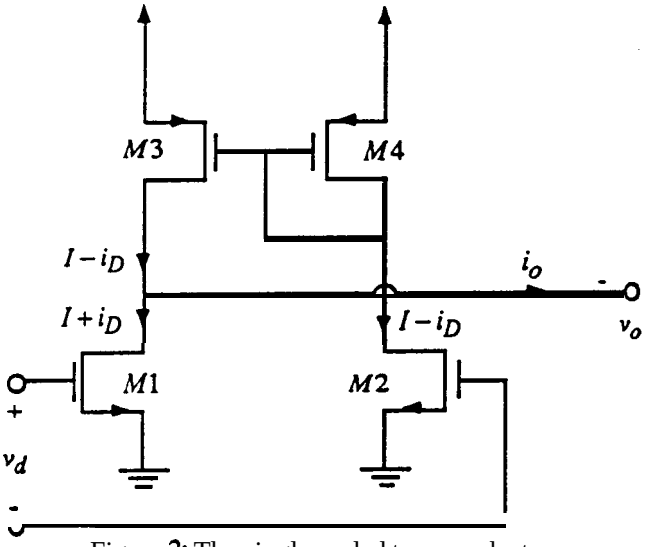


Figure 2: The single-ended transconductor

Since we are optimizing for speed, and hence using short-channel devices (0.9μ in this technology), equation (1) is not a good model. A simple correction term for transverse-field degradation of mobility[12], gives the equation

$$i_D = K\frac{W}{L}\frac{(v_{GS}-V_T)^2}{1+\theta(v_{GS}-V_T)} \tag{4}$$

For $\theta(v_{GS}-V_T) << 1$ equation (3) still applies, while for $\theta(v_{GS}-V_T) >> 1$ the devices are essentially linear transconductors already, and there are no quadratic components to cancel: the result is still large-signal linear, with

$$i_o = K\frac{W}{L\theta}v_d \tag{5}$$

Between these two extremes, however, the devices will produce output currents with odd-order terms not cancelled by the differential configuration and will not be exactly linear. For this reason there is an inherent trade-off between linearity (best at long channels) and speed (best with minimum channels). Our test chip is an experiment with one extreme of the resulting range.

In the presence of fmite output conductance, the circuit of figure 2 has nonzero common-mode gain, resulting from the asymmetry between connections of M3 and M4. A matching argument can be used to show that this produces a voltage gain of approximately -1. Transistors M2 and M4 form a ratioed inverter (which we have designed to have a voltage gain of about -1): for a purely common-mode signal in, and with like transistors matched and having finite output conductance, the Ml-M3 pair will operate at exactly the same gate-source and drain-source voltages as the M2-M4 pair when the drain of Ml (which is the output) tracks the drain of M2 (the ratioed inverter). This common-mode gain is expressed as a voltage gain: the common-mode rejection ratio should be expressed as a ratio of transconductances, and is $g_m$ I $g_o$. Because of the use of short-channel devices, this is low: about 20dB.

The transconductor is designed to operate with all devices in pinch-off. M 1 or M2 will enter mode if their drain voltages drop more than one threshold voltage below their gates, which sets an upper limit of about 1V on differential signal levels. Ml and M2 can also be driven into cutoff by signals larger than $2(V_{CM}-V_t)$, and this mechanism will dominate for low $V_{CM}$ (which will be needed when tuning for low transconductances, which in turn correspond to low frequencies, low input gains or high Q-factors). M3 can enter triode for high common-mode inputs.

The complex relationships between output swing and control voltage severely limit the useful tuning range of this uansconductor. Many of these problems are common to all CMOS transconductors but in the short-channel case the transverse-field terms further reduce the range of transconductance available from a given range of tuning voltage $(V_{CM}-V_t)$ .(note that in the limiting case of equation (5) no adjustment of transconductance is possible) Wide tuning range can only be practically obtained by augmenting the individual transconductor's poor tuning range with some other mechanism, such as by switching-in capacitors or by partially cancelling the outputs of two transconductors.

## The Differential Transconductor

A differential-output transconductor is obtained from a pair of single-ended circuits each producing one of the two outputs, with cross-coupled inputs to get appropriate signs. This kind of arrangement results in finite common-mode gain from mismatch between the two half-circuits, which may add to that from the finite $g_o$.

An ideal transconductor would, when capacitively loaded, produce a frequency response that rolled off at exactly 2OdB/decade and had exactly 90° of phase at all frequencies. Finite output conductance reduces gain and phase at low frequencies; parasitic poles in $g_m$ cause excess phase and reduced gain; and fmite gate-drain capacitance causes aright-half-plane zero for excess phase and increased gain. Practical transconductors work well at frequencies (geometrically) half-way between the low-frequency pole $g_o$ I C and the high-frequency pole (near $f_t$) or zero ($g_m$ I $C_{ds}$); at frequencies below this point the output conductance provides excess damping for filters using the element (hence reducing Q) and at higher frequencies the excess phase causes Q-enhancement or even oscillation. Our chip was overdamped up to frequencies near 3OOMHz, indicating that $g_o$ damping dominates over the VHF range.

## The Biquad Loop

We implemented a second-order loop, chosen as a simple structure that demonstrates the capabilities of the technology. This structure consists of a pair of differential transconductors connected in a loop as shown in figure 3, together with capacitors (to defme frequency $\omega_0$), damping devices $R_D$, and voltage sources $V_{CM}$ to set common-mode levels and thereby tune the transconductors. We implemented all of these components with MOS devices to obtain simplicity, reduced process sensitivity, and tunability at some cost in linearity

## Capacitors

We chose to use grounded, rather than differential, capacitors in order to control the common-mode loop caused by the fmite common-mode gain of the transconductors. This loop would ordinarily be highly unstable, since a loop of two integrators with gains having the same signs has real poles at $\pm \frac{G_{mCM}}{C_{CM}}$. Choosing to use grounded capacitors brings these roots as close to the origin as possible for a given differential-loop $\omega_0$. Grounded damping devices can then force both poles into the left half-plane to obtain stability at common-mode.

Because transconductance can only be controlled over a limited range, adjustable capacitors are used to obtain a broad tuning range. We implemented switchable capacitors by using the channel capacitances of a string of NMOS devices as shown in figure 4. These were laid out in a ring pattern to minimize parasitic $C_{min}$, which defines the maximum operating frequency. As transistors $M_{C1}$ to $M_{C4}$ are turned on by external control inputs, progressively lower frequency ranges are obtained The overall differential circuit structure cancels even-order distortion products, and also cancels signal currents in the control inputs. The signal-swing constraint resulting from the need to maintain

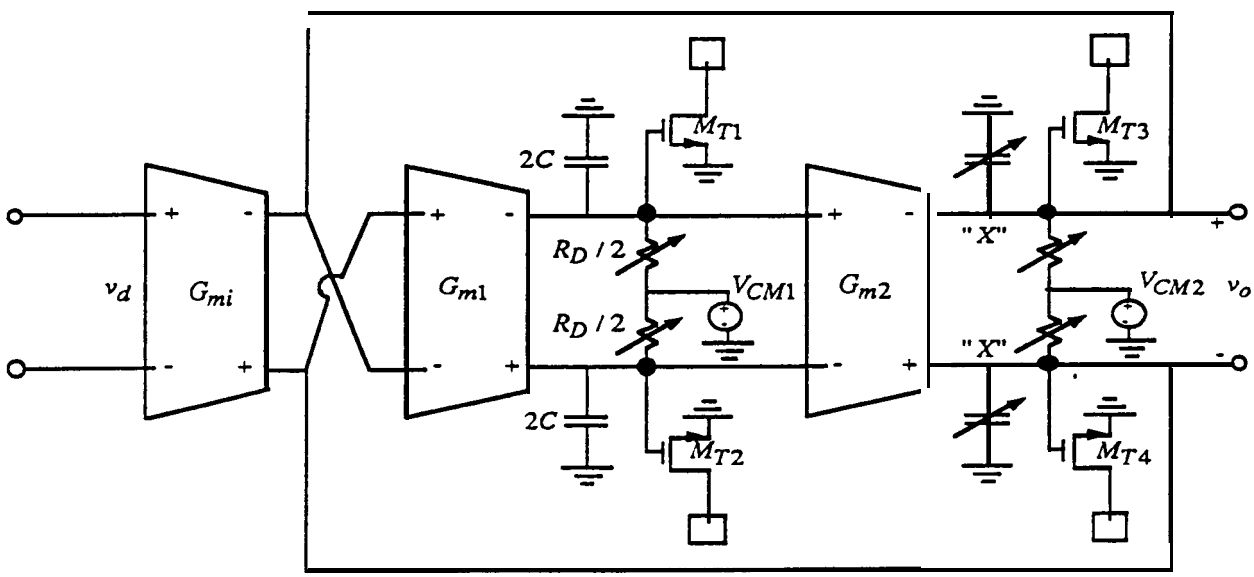


Figure 3: The second-order biquad loop. Capacitors and damping devices are detailed in figures 4 and 5a.

channels in these devices is identical to that required to bias the transconductors, and hence not important.

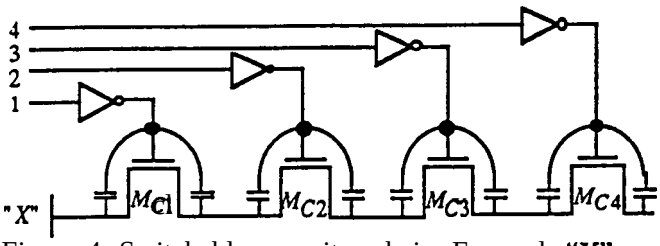


Figure 4: Switchable capacitor chain. For node "X" see figure 3.

As well as allowing coarse frequency-tuning and avoiding the need for a double-poly capacitor, using MOS capacitors reduces the effect of process variation: oxide thickness and channel width appear identically in expressions for transconductance and capacitance, leaving $g_m$ I C insensitive to these highly variable parameters. Channel length continues to contribute variability.

At low frequency settings, the series string of "on" devices has the structure of an RC line. This effect is conveniently more tolerable at low than high frequencies.

## Damping and Common-Mode Control

Although a self-connected transconductor can be used for damping, it is not the best choice here: it implements a differential resistor, and so does not stabilize the common-mode loop. We chose instead to use the source impedance of an NMOS device biased by a current source as shown in figure 5a. With only two transistors per side, this gives us common-mode control as well as damping by approximating the Thévenin equivalent of figure 5b. Even-order distortions are, of course, cancelled by the differential structure.

The ratio between device sixes in the transconductor and the damping circuit sets a nominal circuit Q, which can be adjusted at the cost of dynamic range. We chose a 2:1 ratio for purposes of experimentation.

## Probes

At the high-frequency extreme, node capacitances are well under 1pF. It is therefore difficult to probe the nodes without affecting the circuit.

While a conventional solution to this problem would be to add source followers as buffers, we preferred to use common-source devices $M_{T1} - M_{T4}$ as shown in figure 3.

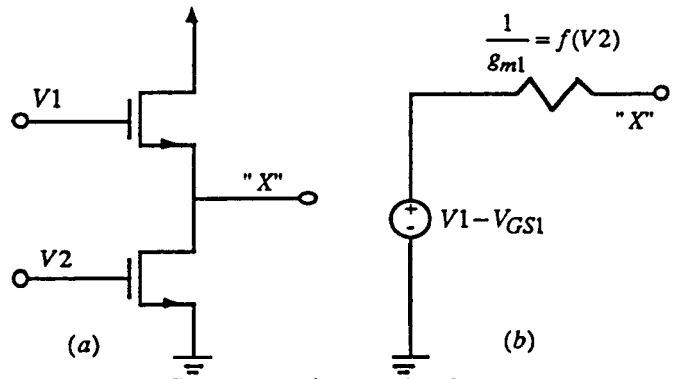


Figure 5: a) Common-mode control and damping details. b) A Thévenin equivalent of figure 5a.

These are linear under the same assumptions as the transconductor, and can directly drive a 50Ω load for RF measurements. Signal voltage swings, however, must be deduced indirectly.

In a practical system we might expect the signals from these filters to be consumed on-chip, so that these probe devices should be regarded as test equipment.

## Measurement

A photomicrograph of the circuit appears in figure 6. The active area is approximately 2551.t by 112µ. The transconductors and a capacitor are marked on the photograph. The entire biquad occupies roughly twice the area of a pad without having been very tightly laid out.

Depending on tuning voltages and the number of capacitors in use, a variety of $f_o$ and Q values can be obtained. Figure 7 is a scatter plot showing $(f_o, Q)$ values obtained experimentally. The points are labelled with numbers from 0 to 4 that specify the number of capacitors switched on in each case.

The plot shows, as expected, that higher Qs are obtained at higher frequencies, as A-related effects begin to cancel the $g_o$-induced damping that dominates at lower frequencies. These effects appear to balance at about 300MHz, below which the circuit is stable even with the explicit damping devices turned off. The lower-Q boundary of this plot has not yet been thoroughly investigated.

The point marked with an asterisk in figure 6, for which spectrum analyzer photographs are shown in figure 8, was selected for detailed characterization. Measured $f_o$ and Q were 276MHz and 21 respectively, as compared to 248 and 20 from simulation. Power supply current was 6mA, which also compares well to a simulated 5.3mA.

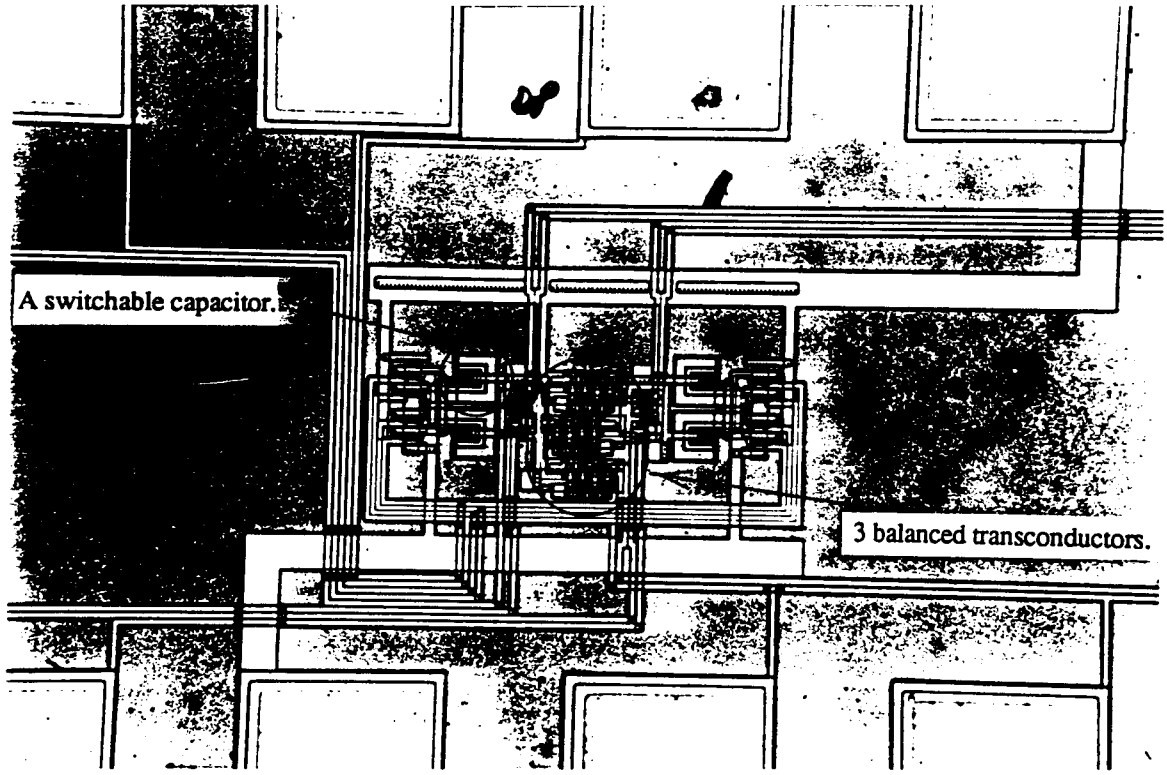


Figure 6: A photomicrograph of 0.9μ CMOS biquad.

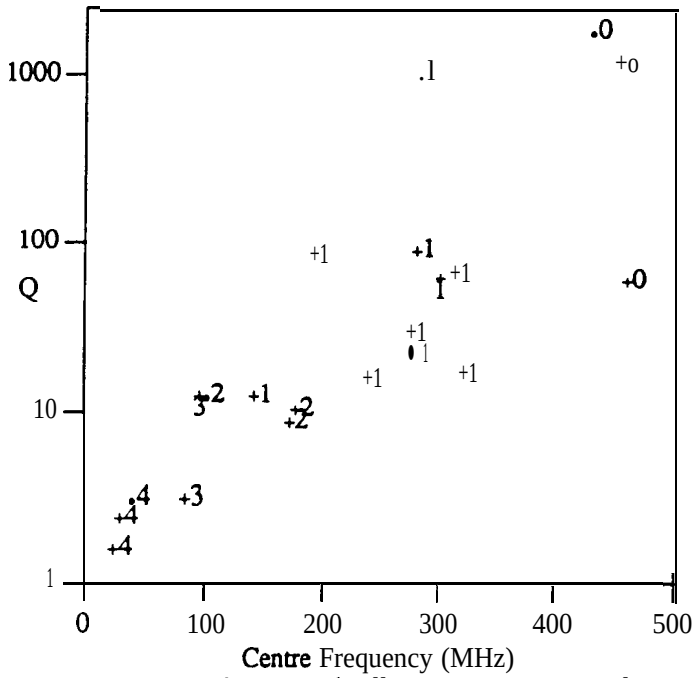


Figure 7: A scatter plot illustrating experimental ($f_o$ , $Q$) values.

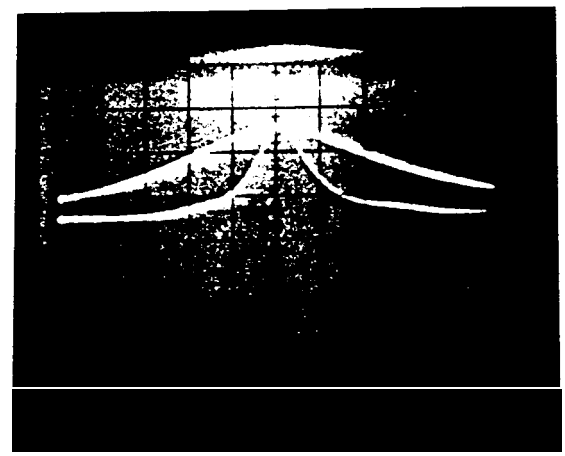

Figure 8: Obtained experimental spectrum: centre frequency 276MHz, traces: 5MHz/div, 20MHz/div, reference level -40dB.

We deduce internal signal levels from output current by estimating the transconductance of the test devices. The reasonable agreement between simulated and actual $f_o$ led us to use the simulation figure of $0.52\,m\mho$. The peak internal differential level obtained in the experiment of figure 8 was computed on this basis to be 122mV for a 14mV input level, as compared to 160mV in simulation.

High levels of nonlinearity distort the appearance of a spectrum, but an intermodulation-distortion (IM) test is more sensitive and direct. We chose to estimate the cubic distortion by measuring the output component at the upper 6dB frequency when inputs are at the bandcentre and the lower 6dB point. For signals with output levels at 14mV (276MHz) and 7.4mV (265MHz), a 0.7mV component at 287MHz was observed, for approximately 5% distortion. These levels correspond to a 384mVrms internal signal level.

Output noise was dominated by the test setup, because of the low gain of the probe devices. An estimated input-referred noise density of $70nV$ I $\sqrt{Hz}$ was calculated based on simulated transistor transconductance figures yielding 3.23mVrms noise power on a differential internal output. For the IM test conditions above, this level corresponds to a SNR of 42dB, making distortion dominant. At internal signal levels of 224mVrms, the two mechanisms would be equally important and would give a $S/N+D$ ratio of 34dB. In comparison, we obtained a simulated integrated noise power of 2.43mVrms on a differential output, suggesting slightly better SNR. SNR performance at the high end is "worst-case"; because the higher node capacitance when more capacitors are switched in for lower speeds reduces $kT/C$.

## Conclusions

We have demonstrated that a $0.9\mu$ CMOS process is capable of performing filtering in the VHF band with good Q factors and moderate SNR. Very simple circuits were used, and were very sparing of silicon area.

The most likely areas of application of this capability are in data communications, where high speeds, moderate SNR, and tunability are appropriate.

## Acknowledgments

The design was largely done during a sabbatical at AT&T Bell Laboratories in Reading, Pennsylvania, in the CMOS group led by T.R. Viswanathan. Discussions with him, and frequent discussions with Steve Lewis, Javier Fernandez, Jeff Sonntag and Scott Fetterman, all contributed to the work. We thank John Pastemak, University of Toronto, for his assistance in experimentation.

## References

1 J. J. Friend, C. A. Harris and D. Hilberman, "STAR: An active biquadratic filter section", *IEEE Trans. Circuits Syst.*, vol. CAS-32, pp. 115-121, Feb. 1975.

2 M. Banu and Y. Tsividis, "Fully integrated active RC filters in MOS technology", *IEEE J. Solid-State Circuits*, vol. SC-18, no.6, pp. 644-651, Dec. 1983.

3 J. T. Caves, M. A. Copeland, C. F. Rahim and S. 0. Rosenbaum, "Sampled analog filtering using switched capacitors as resistor equivalents", *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 592-600, Dec. 1977.

4 K. Martin, "Improved circuits for the realization of switched-capacitor filters", *IEEE Trans. Circuits Syst.*, vol. CAS-27, pp. 237-244, Apr. 1980.

5 K. W. Moulding, J. R. Quartly, P. J. Rankin, R. S. Thompson and G. A. Wilson, "Gyrator video filter IC with automatic tuning", *IEEE J. Solid-State Circuits Syst.*, vol. SC-15, no. 6, pp. 936-968, Dec. 1980.

6 A. V. Oppenheim and R. W. Schafer, *Discrete Time Signal Processing*, Prentice-Hall Inc., Englewood Cliffs, New Jersey, 1989.

7 F. J. Femandez, "Linear CMOS transconductance element", U. S. Patent, No. 4734654, March, 29, 1988.

8 C. S. Park and R. Schaumann, "Fully Integrated analog filters in CMOS technology", *IEEE 1986 Int. Symp. Circ. System, San* Jose, California, pp. 1161-1164.

9 R. Castello and P. R. Gray, "A high-performance micropower switched-capacitor filter", *IEEE J. Solid-State Circuits*, vol. SC-20, no. 6, pp. 1122-1132, Dec. 1985.

10 A. Nedungadi and T.R. Viswanathan, "Design of linear CMOS transconductance elements", *IEEE Trans. Circuits Syst.*, vol CAS-31, pp. 891-894, Oct. 1984.

11 Scott T. Dupuie and Mohammed Ismail, "High frequency CMOS Transconductors", in *Analogue IC design: the current-mode approach*, Edited by C. Toumazou, F.J. Lidgey and D.G. Haigh, Peter Peregrinus Ltd., London, U.K., pp. 181-238, 1990.

12 C. Duvvury, "A guide to short -channel effects in MOSFETs", *IEEE Circuits and Devices Magazine*, vol 2, no. 6, pp. 6-10, Nov. 1986.