10.7MHz Bandpass Delta-Sigma A/D Modulators

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Abstract

Two second-order bandpass delta-sigma A/D modulators have been implemented in a 0.8um BiCMOS [2] process to demonstrate the feasibility of converting a 10.7MHz radio IF signal to digital form. The circuits, based on switched-C biquads, are clocked at 42.8MHz and demonstrated 55dB SNR in a 200kHz bandwidth while dissipating 60mW of power from a 5V supply.

Introduction

There is industrial interest in A/D conversion at the intermediate-frequency (IF) stage of a radio [1], because that allows demodulation and IF filtering to be done digitally. The robustness of the digital circuitry gives manufacturing advantages and allows the use of sophisticated algorithms, which are especially useful with digitally coded transmissions. A/D conversion can be done in quadrature at baseband, using a "zero-IF" receiver, but that requires precision matching and is susceptible to a variety of DC instabilities and electromagnetic compatibility problems. Alternately, a bandpass signal can be directly converted using a video or ΔΣ converter.

ΔΣ converters consist of a filter and comparator (or other low-resolution A/D) in a feedback loop, and are oversampled. Monolithic fourth-order bandpass delta-sigma (BPΔΣ) modulators have been reported [3],[4] with centre frequencies of 455kHz and 2MHz and bandwidths of 10kHz and 200kHz respectively. Another device obtained a 55dB SNR at a 6.5MHz centre frequency [5] and 200kHz bandwidth using off-chip inductors as resonators. A 200kHz bandwidth makes the technology practical for applications like GSM telephony.

Using oversampling with wideband signals implies fast clocking, so there is a question as to how wideband a monolithic realization can be. This work demonstrates in monolithic second-order prototypes that a 10.7MHz bandcentre is possible, with 55dB SNR performance in a 200kHz band. This study uses switched-C technology because it is proven for high resolution at baseband and because it is a monolithic technology capable of delivering precision analog performance. Inductor- [5][6] or transconductor-based technologies can be expected to dominate at very high speeds, but are more difficult in that they involve tuning.

This paper presents two different types of second order switched-C bandpass delta-sigma modulators. The two structures both use fully differential op-amps with continuous time common mode feedback, but use different clock phasings to experiment with different trade-offs between active and passive sensitivities.

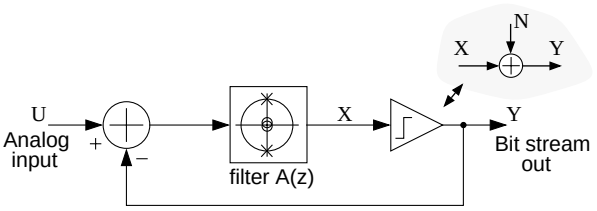

Figure 1 Bandpass Delta-Sigma Modulator

Modulator Design

The basic 1-bit ΔΣ modulator consists of a quantizer and a loop filter as shown in Fig. 1 [7]. By choosing the loop filter [3] we can shape the quantization noise away from any frequency band desired. Modelling the quantizer by a linear white noise source, (shaded area in Fig. 1) we can derive a noise transfer function $H_q(z)$ and a signal transfer function $H_u(z)$: $H_q(z) = 1/(1 + A(z))$ and $H_u(z) = (A(z))/(1 + A(z))$.

For a simple second-order BPΔΣ modulator with a centre frequency at one quarter the sampling frequency the filter response is given by $A(z) = (-1)/(z^2 + 1)$ giving a noise transfer function $H_q(z) = (z^2 + 1)/z^2$ and a signal transfer function $H_u(z) = -1/z^2$. The output spectrum of the resulting ideal modulator with dither added to the input sine wave to destroy tones [8] is shown in Fig. 2.

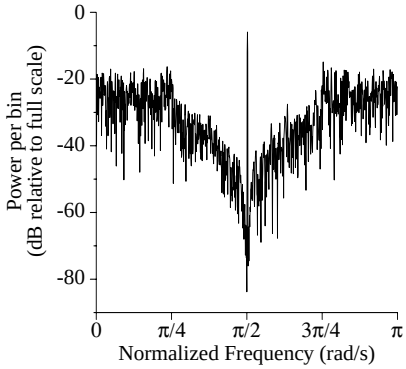

Figure 2 Output spectrum of ideal second order modulator. The abscissa contains 2048 bins.

SC Filter Design

Several different biquad structures can be used to realize the filter response desired. In this section we compare two of them. One, shown in Fig. 3, uses lossless discrete integrator (LDI) clock phasing which results in 1 delay around the loop joining capacitors C_r, C_{i1}, C_x and C_{i2}. With ideal op-amps this structure guarantees that the poles will be on the unit circle, regardless of actual

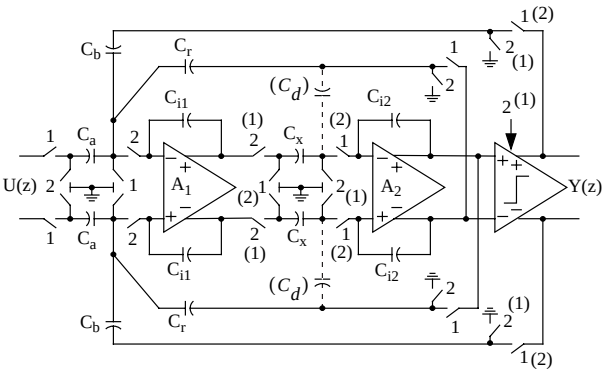

Figure 3 a) LDI BPΔΣ modulator
b) Forward Euler BPΔΣ modulator add C_d and use ( ) clock phasing

capacitor ratios. Capacitor ratio mismatches cause errors only in the location of the notch frequency. This advantage comes at the expense of increasing load capacitance, slowing settling.

The second filter in Fig. 3 is obtained by using the clock phasing in parentheses "( )" and adding capacitor C_d. With this phasing a "Forward Euler" filter is obtained. The disadvantage of this structure is that magnitudes of the poles are dependent on matching of capacitor ratios, but now settling is faster.

Nominal capacitor values for the two filters are as shown in Table 1.

Table 1: Nominal capacitor values for the two biquads

Component	C_a	C_b	C_{i1}	C_{i2}	C_x	C_r	C_d*
Value (pf)	0.2	0.2	0.5	0.3	0.5	0.6	0.6

* capacitor C_d is not present in the LDI biquad

Effects of Non-ideal Op-Amps

The effects of finite op-amp gain, bandwidth and slew rate were considered, both by simulation and analytically, when determining the equations that would predict the phase and magnitude errors in the two different biquads. The effects of finite gain and BW on switch-C biquads for zero output impedance op-amps were previously investigated by Martin and Sedra [9]. These results were then generalized to transconductance op-amps, where the transient due to charging amplifier loads is important, by Ribner and Copeland [10]. Neither of these methods considered slew rate limited op-amps or input and output parasitic capacitances. These extensions are made in [12], and the resulting equations fit experimental data well.

Pole positions are affected by incomplete settling on both clock phases, which can be analyzed as providing reduced gain and a phase error. The effective gain of a partially settled amplifier, for example, is of the form $1/(1-\beta e^{-K})$, where K represents the number of time-constants available after slewing. Our op-amp spent approximately half of each phase slewing, thus reducing the time available for linear settling by a factor of two. Slew rate and hence speed can be increased, but at the cost of higher bias current.

The LDI circuit requires that its amplifiers respond to an input transient and drive a load simultaneously, making settling slower than for the FE case where input and load are clocked on opposite phases. It treats both op-amps symmetrically, while settling for the FE structure is dominated by the second op-amp.

Errors in phase result in shifting the centre frequency of our modulator from the ideal, reducing SNR in the band selected for decimation. Magnitude errors result in lowering the Q of the filter and again reduce the obtainable SNR. Low Q also produces "deadband" behaviour and may result in intermodulation distortion, particularly when the inband signal has an AM component.

Op Amp Design

A fully differential folded cascode opamp with continuous time common mode feedback was designed in the 0.8um BiCMOS process (Fig. 4). An infinite input impedance was required for the SC filters to avoid charge leakage, so we used MOS inputs. PMOS devices were used so that the much faster NPN bipolar devices could be used as the bottom current source where the second pole occurs $P_2 \approx \frac{g_{m,\,bibolar}}{c_{dg}+c_{ds}}$. The second pole is now at a much higher frequency because of the much higher g_m of the bipolar device and as a result excellent phase margin is obtained. The simulated results for the folded cascode opamp are given in Table 2.

Table 2: Simulated results for the Folded Cascode Opamp

Parameter	**Value**
DC gain	58 dB
Phase Margin	75^0
Unity gain frequency	500 MHz
0.1% settling time	11.2 ns
slew rate	1200 V/us
power consumption	26 mW

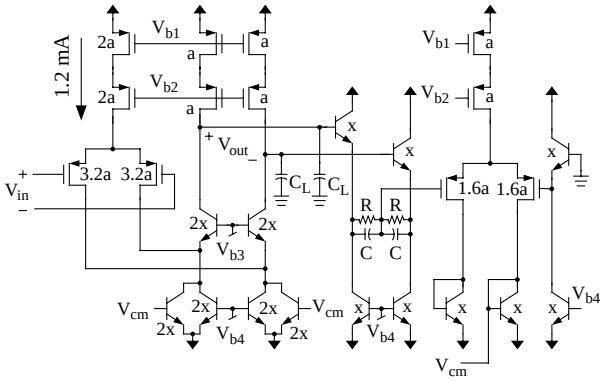

Figure 4 Folded Cascode Op-Amp with continuous time CMFB.

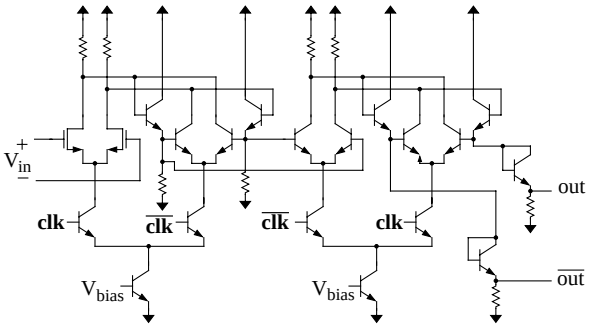

Figure 5 Latched Comparator

* C_L = 1.0 pf in all simulated tests

Comparator Design

The comparator (Fig. 5) was a version of an existing part [11] modified by replacing bipolar inputs with NMOS devices so as not to load amplifier A_2 at DC. (which would reduce its gain and settling accuracy) It has approximately 8 bit accuracy at 200 MHz, which is sufficient for our modulators, since ΔΣ circuits are known to be tolerant of comparator offsets and hysteresis.

Experimental Results

Fig. 6 is a photomicrograph showing both the FE (labelled “SigDel2ph” on the layout in reference to the two-phase delay around the loop) and LDI (SigDelLDI) BPΔΣ modulators. Test structures were also fabricated for an individual op-amp and a switched-C settling test circuit. A typical output spectrum, one for the FE BPΔΣ modulator when clocked at 45 MHz, is shown in Fig. 7. It broadly matches the simulated spectrum in shape (with a fatter noise band attributable to the larger variance expected from using a larger number of bins), but has significant tone power well out of band at about $1/8$ and $3/8$ of the clock frequency.

Figure 6 Photomicrograph of BPΔΣ modulators

Fig. 8 is an expanded in-band plot of the same measurement. Clock and input frequency generators were asynchronous, so the input tone is not confined to a single FFT bin, and there is also sideband power from both frequency sources. Note that the spectra in these experiments are obtained digitally, rather than (as is commonly done) simply by running the digital stream into an analog spectrum analyzer. The latter technique can be misleading because it hides the effects of clock jitter.

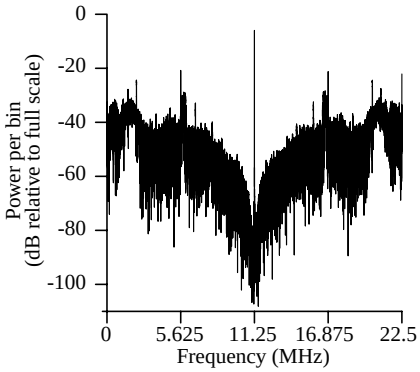

Figure 7 Output spectrum of the FE BPΔΣ modulator for a half-scale tone input near the centre of the band of interest. Clock frequency is 45 MHz

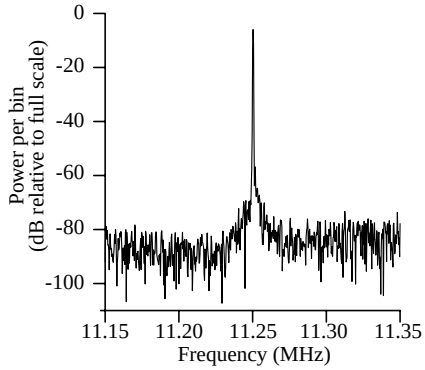

Figure 8 In-band plot of Fig. 7. The abscissa contains 656 bins.

Bit streams were obtained for both modulators at several different clock frequencies. A Hanning-windowed 65536 point. FFT was performed on the bit streams and the notch frequency was determined to give the points plotted in Fig. 9. A +0.3% error in the capacitor ratio C_d/C_{i2} and +0.2% error in the capacitor ratio C_r/C_{i1} were estimated to be the capacitor ratio mismatches, resulting in a small frequency error even at low clock rates. These mismatches are quite plausible due to the small unit capacitor value we are using. The plot shows that settling is essentially complete below about 30MHz and

that the FE structure is still good to 1% at the 42.8MHz clock needed for a 10.7MHz IF.

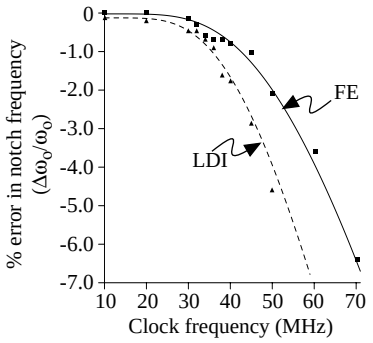

Figure 9 Percentage error in notch frequency resulting from non ideal op-amps. Points are experimentally measured and lines are mathematically predicted by equations in [12].

Signal levels were varied at a constant clock frequency, producing the plot of SNR against signal level shown as Fig. 10. There is a large deviation from the straight-line behaviour predicted by the linear model and by simulations: this is similar to the characteristic already known for first-order lowpass ΔΣ modulators in the presence of a small offset, and which should be expected for second-order bandpass. It suggests that tones tend to be out-of-band at low input levels.

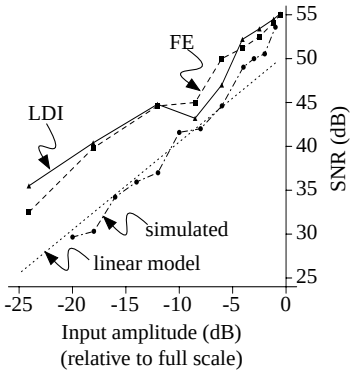

Figure 10 SNR for a 200 kHz bandwidth and a clock frequency of 20 MHz.

Conclusions

Switched-capacitor bandpass ΔΣ technology appears to be practical for A/D conversion of radio IF signals at 10.7MHz, although a production version of the chip would need an improved op-amp (particularly slew rate) to get the performance margin needed to cover process and temperature variation. We have initial simulation results suggesting that an op-amp almost twice as fast should be possible in this process, so this re-engineering does not seem impractical.

A second-order modulator gives a 55dB SNR in a 200kHz bandwidth when clocked at these rates, but shows pronounced non-ideal noise behaviour. Using a fourth-order structure (shown to work at lower clock rates in [3] and [4]) with the high-speed technology demonstrated here should give improved bandwidth and SNR, which in turn would give more margin and flexibility to the system designer. For example, scaling the performance of [4] by a factor of 5 in speed would give 1MHz bandwidth and allow digital fine-tuning of channels in a GSM or CT-2 mobile telephony system.

Forward-Euler switch phasing gives a significant speed advantage over LDI, and its sensitivity to ratio errors does not appear to seriously degrade SNR. Fourth-order systems are less sensitive to Q errors, so the FE structures should work even better there.

Acknowledgments

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