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ABSTRACT

A simple technique to compensate for DC offsets in many analog circuits is presented. An offset-free, infinite DC gain integrator is established in a feedback loop about the uncompensated circuit, resulting in a high-pass system output response. The ***ideal*** integrator is realized via the use of a counter resulting in the cancellation of the signal's median rather than the usual case of the signal's mean. Thus, the technique is limited to applications where the signal's median is equal to its mean -a common occurrence in many applications.

I. INTRODUCTION

Fabrication tolerances, temperature, circuit non-linearities and non-idealities all give rise to DC offsets which degrade the performance of integrated analog circuits. Consequently, much work has been devoted to alleviate this problem including: manual trimming, AC-coupling, chopper stabilization [1] and reset switches [2]. These techniques are either inefficient, require large integrated circuit area, or have limited performance. More importantly, the latter two techniques do not compensate for signal offset.

In situations where DC transmission is unimportant, establishing a low-pass (integrator) feedback loop around the circuit requiring offset compensation results in the cancellation of both signal offset and circuit-generated offset [3-5]. For optimal DC rejection the feedback integrator must be ideal(pole exactly at DC, zero input offset) [2,3] and in certain applications may require a large integration-time-constant. Thus, realizations for this integrator in the analog domain often require difficult design techniques. To overcome these limitations, we propose a binary counter together with a digital-to-analog converter (DAC) as an ideal integrator.

The use of the above digital integrator in DC offset cancellation rather than an analog equivalent results in some interesting properties. One such property is the fact that the signal's median rather than its mean is cancelled. Fortunately, many applications have the property that the signal's mean equals its median. Another property is that while an offset-compensated gain stage will have an output offset equal to the input-offset of a comparator, an offset-compensated comparator will ideally have a DC-free output sequence. One of the main applications for an offset-compensated comparator is in the area of analog adaptive filters where DC offsets are particularly troublesome [6-10].

The outline of this paper is as follows. First, the proposed technique is described and constraints on the input signal's statistics are discussed. Next, analysis is performed on an offset-compensated gain stage showing the 3-dB cutoff frequency is dependent on the input signal level. A design alternative is then described to replace the DAC which could occupy much silicon area. Finally, experimental results are given verifying the analysis, where some approximations were made, and demonstrating the practicality of the approach in an analog adaptive application.

II. CIRCUIT PRINCIPLE

To explain the strategy, consider a slicer whose input is a sinusoidal signal disturbed by a superimposed DC offset. The output sequence will not be an accurate representation of the AC signal, but will contain a 'DC component exhibited by a duty cycle other than 50%. If the slicing level were adjusted to the overall DC leve1 the required DC-free output sequence will be attained.

The simplest form of the proposed system, shown in Fig. 1, automatically trims the threshold, y(t). The input signal, x(t), is periodically sliced about y(f), the comparator makes its decision and the counter increments or decrements accordingly. Given some elapsed time, the updated counter value will alter the DAC state, hence the threshold level. Due to the negative feedback, the output, $\hat{x}(t)$, will attain a steady-state condition where the counter increments and decrements occur with equal probability implying the input signal spends half its time above the threshold level and half its time below. Therefore this time varying threshold estimates the signal median and since the median value is equal to the mean value for this sinusoidal signal, the comparator is "AC-coupled", that is, $y(z) \approx x_{DC} + V_{offc}$. ($y(t)$ becomes the signal median for an infinite precision DAC and counter.)

2.2. Input *Signal Constraint*

While for a sinusoidal signal the mean equals its median, this is not true in general. The median of a stochastic process X is that value x for which $P(X \le x) = P(X \ge x) = 0.5$ where $P(\bullet)$ denotes the probability operator. When unique, the median is the ordinate which separates the probability density function (PDF) into two parts of qual area. For a symmetric PDF the mean and the median coincide [11]. Therefore, if a unique median for some symmetric distribution can be obtained, this median would be an accurate estimate of the mean. Under this condition, the threshold approximates the mean and the system of Fig. 1 behaves as a true "AC-coupling" network. Most physical signals, such as speech (Fig. 2a) [12], posses this property.

In certain cases there may exist a median **interval**[1] such that $P(X \le x_1) = P(X \ge x_2) = 0.5$, and so a unique median will not exist. When the input signal has a wide median interval, as is the case for a square wave (Fig. 2b), the threshold could drift between the two extremes in this interval. Whether this drift can be tolerated depends on the application,

22. *The Zdeal Integrator*

For the elements shown in the dotted box of Fig. 1, the up/down counter realizes an offset-free integrator with a pole precisely at DC while the DAC provides an analog output. With $\hat{x}(t)$ a square wave of unit magnitude and variable duty cycle, **then**

$$u(n\Delta T) = \frac{1}{\Delta T}\sum_{i=0}^{n-1}\hat{x}(i\Delta T)\Delta T \qquad (1)$$
$$y(n\Delta T) = \alpha u(n\Delta T)$$

where AT represents the sampling **period** ($1/f_{CLK}$), α is a scaling factor describing an M-bit **counter/M-bit DAC** block

1 **The** ordinate interval between the smallest and largest median is referred to as the median interval.

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such that $\alpha \equiv \frac{V_{fs}}{2^M}$ and V_{fs} is the full-scale DAC output. For $n\Delta T = t$ and for AT small, the summation in (1) approximates an integration,

$$y(t) \approx \frac{\alpha}{\Delta T}\int_0^t \hat{x}(\tau)d\tau, \qquad (2)$$

hence an **ideal integrator** is obtained with an equivalent integration-time-constant given by $\tau \approx$ AT I a. Thus, given that the input signal's median equals its mean, the system shown in Fig. 1 provides a "high-pass" response.

From above it appears that τ depends on the counter size M; hence, to realize a large time constant requires a large DAC. Alternatively an N-bit DAC, where N<M, could be used as long as this DAC is connected to the top N bits of the M-bit counter so τ remains a function of M to a first order. In fact, ignoring the lower order bits of the counter can improve the steady-state response. The choice of N depends on the maximum offset compensation level, $\pm V_{fs}/2$, and on the maximum tolerable trimming step size, $V_{fs} I 2^N$. In addition, since the DAC is used in an infinite DC gain feedback loop to trim an analog circuit, its design specifications are not stringent. Offsets arising from DAC non-linearity will be compensated for by the feedback topology. The design of an area efficient DAC for trimming purposes is currently being investigated.

2.3. *Circuit Extension*

To highlight some aspects of the proposed scheme, the amplifier system, Fig. 3, is presented as it is closer to a linear system. Considering the aforementioned mean-median condition, the slicer output in Fig. 3 can be expressed as

$$\hat{x}(t) = \frac{\tilde{x}(t) - V_{offc}}{\left|\tilde{x}(t) - V_{offc}\right|} \qquad (3)$$

Choosing to approximate $\left|\tilde{x}(t) - V_{offc}\right|$ by some constant parameter η' such that $\left|\tilde{x}(t) - V_{offc}\right| = \eta' + \varepsilon(t)$, allows a simplified quasi-linear expression for (3). Minimizing the mean square value of the error term, $\varepsilon(t)$, with respect to η' for a specific input level results in

$$\eta' = \frac{1}{T}\int_0^T \left|\tilde{x}(t) - V_{offc}\right| dt \qquad (4)$$

This value is often called the L_1 norm of $\tilde{x}(t) - V_{offc}$, denoted as

$$\left\|\tilde{x}(t) - V_{offc}\right\|_1. \qquad (5)$$

Analyzing the complete loop in the frequency domain, making use of (2, 3-5), gives the following input-output transfer-function[2]

$$\tilde{X}(s) \approx \frac{G}{1 + \frac{\alpha G}{s\Delta T \eta'}}\left[X(s) - V_{offa}(s)\right] + \frac{1}{1 + \frac{s\Delta T \eta'}{\alpha G}} V_{offc}(s) \qquad (6)$$

Hence all DC terms are rejected at the output (high-pass response) except for V_{offc}. From (4), (6) and the fact that at the 3-dB cutoff frequency $\tilde{x}_{ACrms}(t) \approx \frac{G}{\sqrt{2}} x_{ACrms}(t)$, it can be shown that the cutoff frequency is

$$f_c \approx \sqrt{2}\,\frac{f_{CLK}}{2\pi}\,\frac{V_{fs}}{2^M}\,\frac{1}{\eta} \qquad (7)$$

where $\eta \equiv \left\|x_{AC}(t)\right\|_1$. Note that the 3-dB cutoff frequency depends on the input signal level through η. This effect is important since to obtain low distortion the frequency of the input signal should be much greater than the cutoff frequency which is variable. Thus, assuming a fixed input frequency, the circuit has the unusual attribute that lower input signal levels will produce higher distortion. Notice also that due to the non-linearity in (3) the cutoff frequency (7) is independent of G, unlike the case in linear feedback control loops.

III. DESIGN ALTERNATIVE

The DAC may impose a big demand on integrated-circuit area, therefore a simpler architecture for the feedback circuit, Fig. 4, is proposed here. The basic circuit (dotted box in Fig. 4) is a cascade of two integrators -an offset-free infinite DC gain integrator (counter) and a damped integrator (charge-pump). Unfortunately it exhibits an excess phase of 90' which can cause system instability in closed loop applications. The secondary path (outside the dotted box) provides stability. To appreciate this, consider the comparator system with the circuit of Fig. 4, which realizes a second-order low-pass response comprising two poles (one at DC, the other depends on capacitor values) and a zero, in the feedback path. The output y(n) is

$$y(n) = \gamma y(n-1) + V_{ps}\beta\hat{u}(n-1) + V_{ps}\delta\hat{x}(n-1)$$

where V_{ps} is the digital supply level, $\hat{u}(n)$ is the MSB of the counter and

$$\gamma = \frac{C}{C + C_1 + C_2}, \quad \beta = \frac{C_1}{C + C_1 + C_2}, \quad \delta = \frac{C_2}{C + C_1 + C_2}.$$

The maximum trimming step size is a_ $= V_{ps}(\delta + \beta)$. Let the comparator input be a DC level. For small trimming step sizes[3] and with $C_2 = 0$ the expected step response, $y(n)$, will be underdamped. (The second pole ($z = \gamma$) is near DC.) Hence overshoot (triangular in shape for this non-linear system) decay will be negligible [13]. This (second-order) response is unacceptable and the secondary path is useful in damping the overshoots. An increase in the ratio C_2 / C_1 increases the system phase margin resulting in a more acceptable response.

Unlike in the system of Fig. 1, the circuit time constant is not a function of counter size (only the MSB is used), but a function of the charge-pump update frequency and a_. To obtain a large time constant it is possible to reduce ϕ, even below the Nyquist rate. Since only the DC output of the feedback integrator is significant, aliasing is tolerable. In an integrated-circuit device leakage currents will put a limit on the lowest update rate possible. For this reason, a floating gate element to replace the charge-pumps is being investigated. Finally, it can be shown that, due to the counter's pole at DC, all offsets are rejected at the output, including the input-referred offset of the secondary path.

IV. EXPERIMENTAL RESULTS

4.1 Offset-Compensated Gain Stage

Fig. 5 depicts typical transfer-functions for the amplifier system of Fig. 3 for different input levels. Clearly the system response is high-pass and the cutoff frequency is signal level dependent. Experimental results for different signal levels, op-amp gain and counter size agree within 10% of the theoretical expression in (7) [13]. In the time domain (Fig. 6) a sinusoidal input with DC offset comparable to signal peak was applied to the amplifier. The AC-coupled output clearly displays an improved signal to offset ratio.

2 It should be noted that since non-linear circuits are used, a transfer-function in the conventional sense does not exist. However, this quasi-linear analysis provides insights into the behavior of the circuit.

3 Although difficult to implement small steps directly in an integrated circuit, practical steps can be applied at an internal node (comparator bias current), corresponding to a delicate trim in the input-referred offset.

4.2, *Analog Adaptive Filter Application*

Our main purpose for developing the circuits proposed here is the implementation of the least mean square algorithm (LMS) in an analog adaptive filter. An accurate implementation of the algorithm is sometimes difficult, thus simplified versions [10], [14] are often realized. The simplest version is the sign-sign update equation for the *ith* coefficient, w_i:

$$w_i(t) = \mu \int_0^t sgn[e(\tau)]sgn[g_i(\tau)]d\tau \quad (8)$$

where e(r) is an error signal, μ is a small step size which controls the rate of convergence, $g_i(t)$ denotes the ith gradient signal, $\frac{\partial y(t)}{\partial w_i(t)}$, and $y(t)$ is the filter's output.

The presence of DC offsets arising from device mismatches and non-idealities affect the LMS algorithm in such a way that the filter settles at a non-optima1 state, exhibiting an excess mean-square-error (MSE) after convergence[8], [10]. The circuits discussed here can be used to implement (8) while compensating for DC offsets as depicted in Fig. 7 (note the hardware simplicity). The block LPF is either the counter/DAC ideal integrator or the second-order low-pass circuit of Fig. 4, the multiplier is an XOR gate.

Experimental results are given for the LPF of Fig. 4. (Similar results were obtained for the counter/DAC LPF.) The gradient and error signals were taken directly from an integrated third-order IIR programmable filter [15]. These had offset levels of about 5OmV, 50% of signal levels. A model matching set-up was configured and two coefficients (zeros) from a total of six were adapted. Without offset compensation for the comparators and input signals (nodes 1 and 2 tied to ground, Fig. 7) the adaptive filter attained the state shown in Fig. 8a. Clearly, excess MSE due entirely to signal offset and comparator input offset is demonstrated. With full compensation a considerable improvement in the convergence of the sign-sign algorithm was obtained, Fig. 8b, illustrating the benefit of the proposed circuits.

V. CONCLUSIONS

An ideal integrator to trim analog circuits was presented and its applicability in realizing an "AC-coupled" comparator was demonstrated. Two topologies for the LPF were proposed and the dynamics of each were briefly discussed. The benefit of the proposed scheme in the important area of analog adaptive filters was also illustrated. The next step would be to quantify the improvement obtainable in an integrated system.

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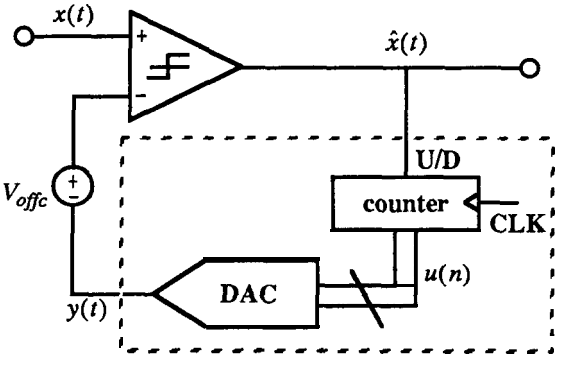


Fig. 1. The DC-compensated comparator loop.

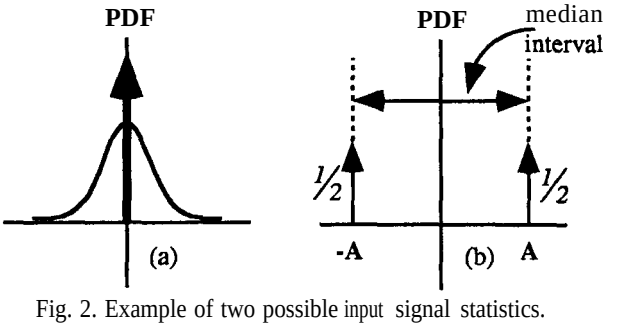


Fig. 2. Example of two possible input signal statistics.

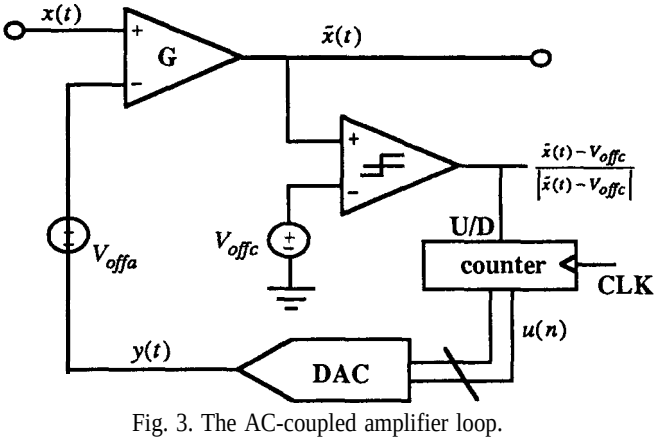


Fig. 3. The AC-coupled amplifier loop.

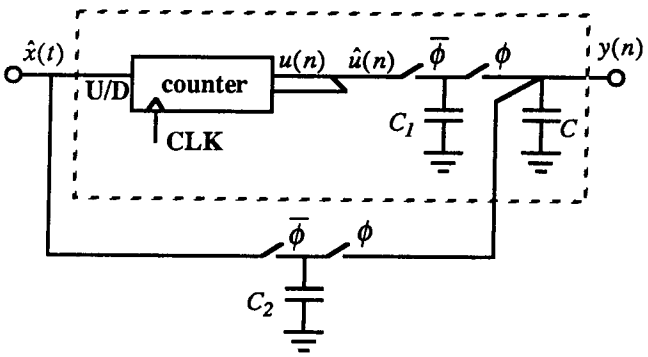


Fig. 4. The second-order low-pass circuit.

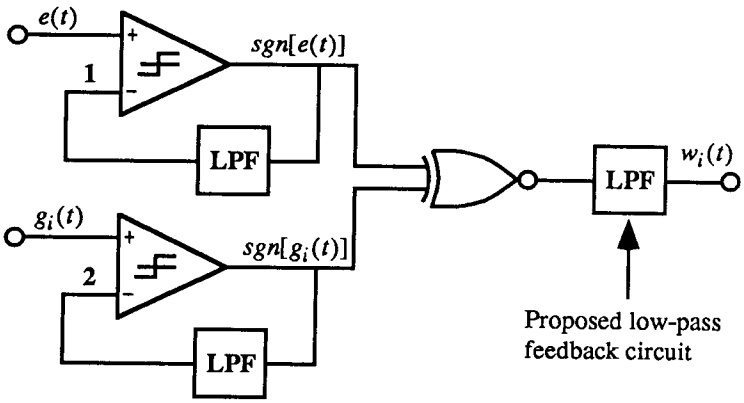


Fig. 7. Block diagram of the offset-free sign-sign LMS algorithm.

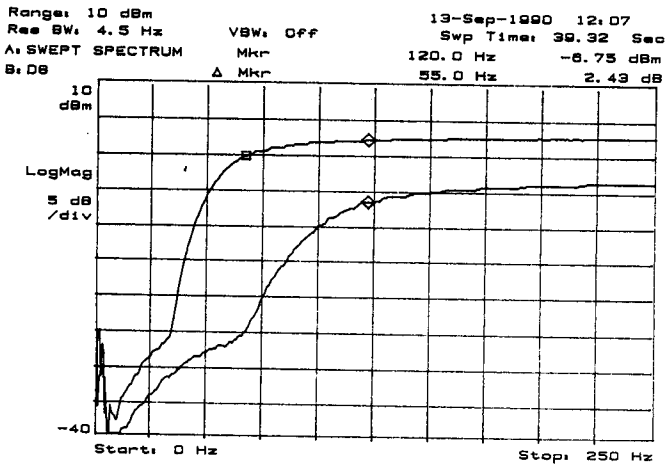


Fig. 5. Amplifier loop experimental results.
Input: swept sinusoid, ±0.2V upper curve, ±0.1V lower curve.
$M = 11$, $f_{CLK} = 25.641kHz$, $G = 2$, $V_{fs} = 2V$.

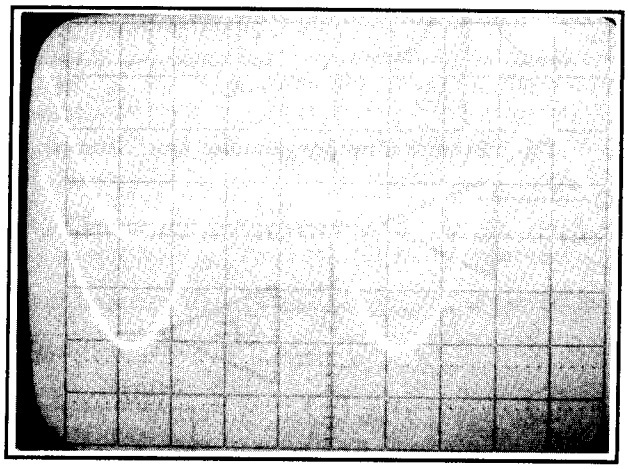
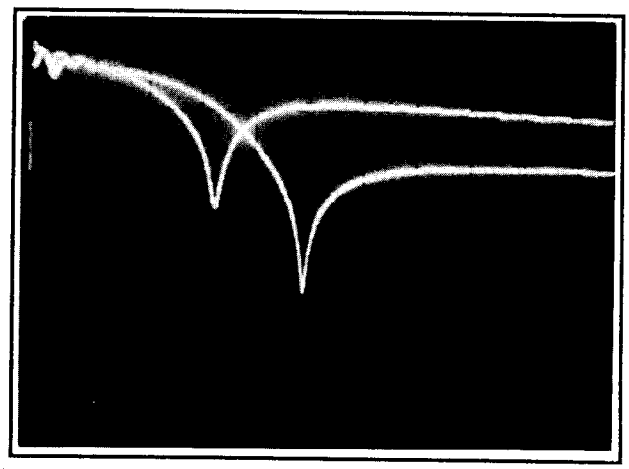
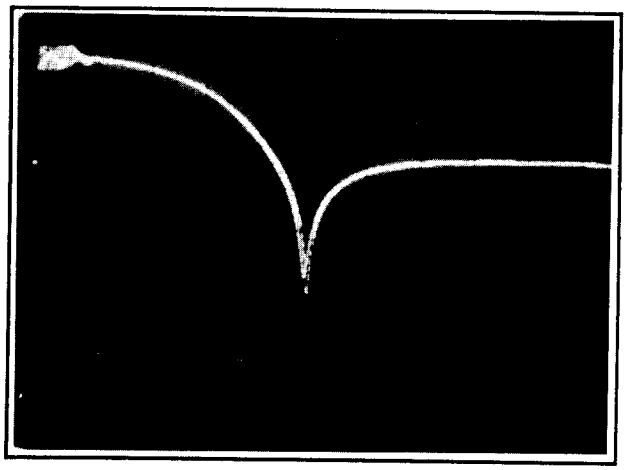


Fig. 6. Illustrating DC cancellation, G=1. Input: upper curve 0.4V offset, 1kHz. Output: lower curve. Scale, both curves: 0.2ms/div, 0.2V/div.



(a)



(b)

Fig. 8. Convergence of the sign-sign algorithm a) without offset compensation, lower curve: reference filter, upper curve: adaptive filter. b) with offset compensation.