A 1V Switched-Capacitor ΣΔ Modulator

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Abstract

This paper describes a 1V first order Switched-Capacitor (SC) ΣΔ modulator implemented in a 0.5μm n+/p+ dual poly gate CMOS process using natural threshold voltage MOSFETs. The natural transistors in this process have threshold voltages of about 180mV (nMOSFETs) and 200mV (pMOSFETs) which is suitable for 1V circuits. Modification to the process is minimal and involves the removal of the threshold adjust implant step. This modulator operates at 1V and has 54dB dynamic range for an oversampling ratio of 128 (sampling frequency 1MHz and signal frequency 4KHz) and consumes about 100μW.

1.0 Introduction

Lowering the supply voltage is the most effective way of achieving low power consumption because power dissipation in CMOS is a quadratic function of supply voltage. Digital circuits capable of operating at a very low supply voltage (200mV) have been demonstrated [1]. In analog circuits, however, lowering the power supply reduces signal to noise ratio (or dynamic range) because thermal noise can not be scaled down. A 1V power supply offers a compromise between low voltage (desired for low power digital circuits) and sufficient dynamic range (required by analog circuits). Moreover, 1V circuits can operate directly from a single-cell battery requiring no dc-to-dc converter.

For 1V operation, the threshold voltage (V_t) of MOSFETs must be reduced to maintain the high speed performance of opamps, analog switches, and digital gates. In [2], low V_t MOSFETs are fabricated by adding an extra mask to the process and a SC filter operating at 1.4V is reported. Here, low V_t natural MOSFETs in a *0.5μm* n^+/p^+ dual poly gate CMOS process are proposed for low voltage operation. This requires no additional mask to the baseline CMOS process and only involves the removal of the threshold adjust implants.

A 1V first order SC ΣΔ modulator is fabricated in a *0.5μm* dual poly gate CMOS process using natural MOSFETs. Measured signal to noise+distortion (SNDR) of the modulator correlates well with theory and simulation results. To our knowledge, this is the first 1V SC ΣΔ modulator circuit using low V_t MOSFETs. The only reported 1V ΣΔ modulators [3] uses an active RC integrator instead of an SC integrator- arguing that leakage current of low V_t MOSFETs switches degrades the accuracy of SC circuits. The impact of leakage current on the accuracy of SC as well as methods of reducing the subthreshold leakage are considered in [4].

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2.0 Process and Devices

In deep submicron (*0.5μm* and less) CMOS technologies surface-channel MOSFET devices are desired due to their reduced short-channel effects. Fabrication of surface-channel MOSFETs requires a dual poly gate process technology where n^+-poly is used for nMOSFETs and p^+-poly is used for pMOSFETs. In such technologies, the natural threshold voltages of the transistors (set by the well implant) are relatively symmetric and are given by,

$$V_t = V_{FB} + 2\phi_F + \sqrt{2q\varepsilon_{si}N_W(2\phi_F)}/C_{ox} \quad (1)$$

where V_{FB} is the flat-band voltage, ϕ_F is the bulk Fermi potential, and N_W is the device well doping concentration. In the *0.5μm* n^+/p^+ dual poly gate CMOS technology used here, natural nMOSFETs and pMOSFETs have threshold voltages of about *180*mV and *200*mV respectively.

3.0 SC ΣΔ Modulator Design

A simple single-ended first order SC ΣΔ modulator is chosen as benchmark to demonstrate the feasibility of using natural MOSFETs for 1V SC design. The architecture of a first order SC ΣΔ modulator is shown in figure 1. It consists of a discrete integrator and a two level quantizer in a negative feedback loop.

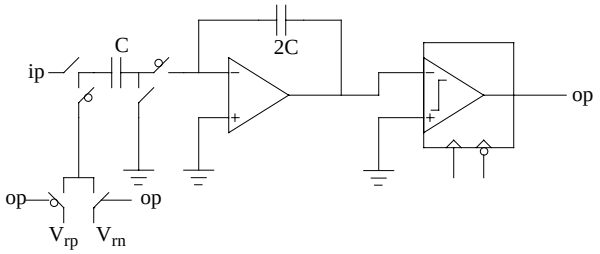

Figure 1: A first order SC ΣΔ modulator

Opamp and Comparator: Lowering the power supply voltage directly reduces the dynamic range and consequently the accuracy of the analog circuitry. Thus rail-to-rail signal swing is desired to maximize the dynamic range. In a SC circuit, signals at the inputs of the opamp are at analog ground, thus no input signal swing is required. However, the output(s) of the opamp must provide the largest possible signal swing. Each transistor at the output stage requires certain voltage to be kept in saturation ($v_{DS} > v_{GS} - V_t$) which limits the output signal swing. Therefore, cascode structures are avoided at the output stage of the amplifier. A two stage pole splitting opamp, figure 2, provides enough gain and maximum signal swing at the output of the amplifier.

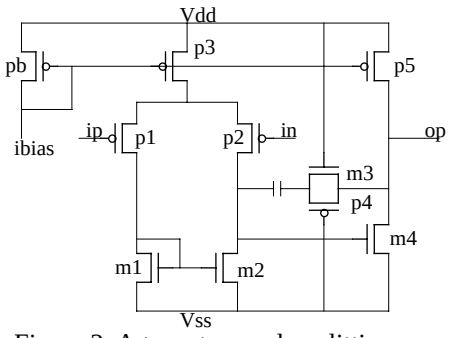

Figure 2: A two stage pole-splitting opamp

This amplifier operates at 1V supply, has a dc gain of 60dB, a unity gain bandwidth of 40MHz, and a phase margin of 60° when driving 1pF load and consumes 30μW. The slew rate of this opamp is 10V/μs.

In ΣΔ modulators the performance of the comparator is not critical. A class AB comparator similar to [5] is used. This comparator has a delay of 6ns for a 1V power supply.

Switches: Switches are the critical component in low voltage SC design. A good MOSFET switch must exhibit a low on-resistance when turned-on and a very low current leakage when turned-off. The MOSFET on-resistance is given by:

$$R_{on} = 1/\left(\mu C_{ox}\frac{W}{L}(v_{gs}-V_t)\right) \qquad (2)$$

With 1V power supply a $W/L = 1.5\mu m/0.5\mu m$ natural nMOSFET switch has an on-resistance of 10K when biased at midrail. In SC circuit of figure 1 two of these switches and the sampling capacitor constitutes an RC circuit. For a sampling capacitor of *1*pF the time constant (τ) will be *20*ns. Settling to *0.1*% of the full scale require *140*ns (7τ) allowing an upper limit of *3.5*MHz operation for this switch.

A turned-off MOSFET transistor with $v_G = 0$ operates in the weak inversion regime. Assuming $v_{DS} > 3\phi_t$, where $\phi_t > kT/q$ the subthreshold current is simplified to:

$$i_{OFF} = I_{D0}\frac{W}{L}10^{-\frac{(v_S+V_t)}{S}} \qquad (3)$$

Here, I_{D0} is the value of drain current for a unit transistor ($W/L = 1$) with gate to source voltage biased at the threshold voltage $v_{GS} = V_t$. S is the subthreshold swing - v_{GS} change needed to increase i_{DS} by one decade. Typical values of I_{D0} and S in this process are *100*nA and *86*mV/ decade respectively.

Increasing the source to substrate voltage reduces the leakage current exponentially. Measurement of subthreshold leakage shows a reduction of more than two orders of magnitude in leakage for a *200*mV increase in source to substrate voltage. The operating signal swing is between *0.25*V-*0.75*V that keeps the leakage current through switches below *10*pA. This is acceptable as discussed in [4].

4.0 Experimental results

The modulator was fabricated in a *0.5*μ*m* n^+/p^+ dual poly gate with linear poly-poly capacitor and triple level metal CMOS process. The chip die photo is shown in figure 3.

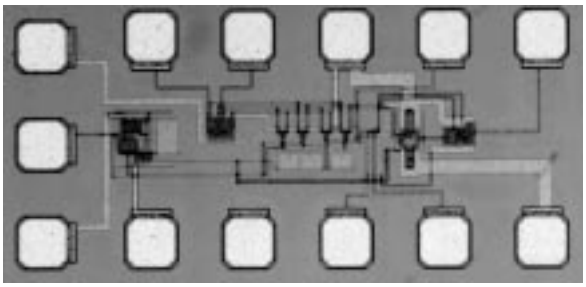
Figure 3: Chip die microphotograph

The modulator was tested at a clock frequency of 1MHz using a 1V supply voltage and reference voltages of $\pm 0.25V$ (with respect to analog ground). The output spectrum for an input signal of *4*KHz and *-6*dB is shown in figure 4. The output bit-stream was captured by a logic analyzer and *131072*-point FFT was performed in Matlab. For an oversampling of *128*, SNDR of *54*dB is obtained.

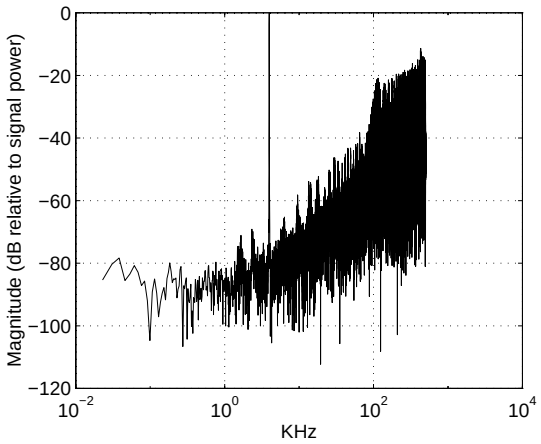

Figure 4: Measured spectrum (Vip=210mV)

Acknowledgments

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