OPTIMIZING THE NATURAL MOSFETS IN A 0.5μm DUAL POLY GATE CMOS PROCESS FOR 1V MIXED-SIGNAL APPLICATIONS

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Abstract

A 1V analog CMOS technology is developed as a subset of a *0.5μm* n^+/p^+ dual poly gate CMOS process. In this process, “natural” threshold voltage MOSFETs are optimized to have a V_t of about *200mV* set by well implants. Process architecture, SUPREM3 simulations, and some measured data are presented.

1.0 Introduction

1V mixed analog/digital signal processing capability is desired in applications requiring low power dissipation, such as battery powered portables [1]. In CMOS, however, such a low supply voltage will cause severe speed performance degradation unless the threshold voltage (V_t) is scaled down. An optimum V_t for 1V mixed signal processing is determined to be about *200mV* based on the energy efficiency of the digital gates and precision/speed of the analog Switched-Capacitor (SC) circuits [2]. Low V_t "natural" MOSFETs can be fabricated as a by-product of a dual poly gate process, where threshold voltages are set by well implants [3]. A process architecture that does not require any threshold adjust implant (for "natural" MOSFETs) is discussed along with some SUPREM3 simulations. Measured results correlate well with theory and simulations. A process designed for 1V operation may be further simplified by eliminating the steps required for hot-carrier reduction i.e., LDD (Lightly-Doped-Drain) implant and formation.

2.0 Optimum V_t for a 1V Supply

In digital circuits the value of the threshold voltage has a direct impact on speed of operation as well as power dissipation. Reduced threshold voltage increases speed but at the expense of increased subthreshold leakage off-current. For analog SC circuits the trade-off is between speed and accuracy. The minimum value of V_t in analog circuits is determined by the required precision.

Analog: MOSFETs used in analog circuits operating in class A or class AB mode do not set any stringent constraints on the minimum threshold voltage. This is the case for transistors used in opamps. However, any transistor operating as a switch must exhibit low on-resistance when closed, and very low leakage current when opened. The required precision of analog circuits determines the maximum allowable subthreshold leakage off-current, which in turn sets a lower limit on threshold voltage. In [2], the effects of leakage through switches have been analyzed in the context of an SC integrator and it is concluded that a V_t~*200mV* is acceptable for many applications.

Digital: A simple (first order approximation) analysis is performed on a CMOS inverter to obtain an optimum supply voltage for minimum energy dissipation. The energy required per operation is approximately [2],

$$E = (fC^2 V_t/\beta)(m^3/(m-1)^2) \quad (1)$$

where C is the load capacitance, f is the operating frequency, $\beta = (1/2)\mu C_{ox}(W/L)$, and $m = V_{DD}/V_t$. Equation (1) has a minimum at $m = 3$. Simulations indicate that $V_{DD} \sim 4V_t$ is the optimum supply for natural MOSFETs and the energy curve is flat around m=4. This reinforces the V_t=*200mV* required by analog circuits for 1V supply voltage. Process and temperature variation of V_t is assumed to be controlled through back bias [2].

3.0 Device Fabrication

Natural threshold voltage CMOS transistors have been fabricated using a *0.5*µ*m* CMOS process. The starting material is *13 -17*Ω*-cm* p-type silicon wafers. A 5µ*m* thick 4-16 mΩ-*cm* p-type buried layer is formed epitaxially followed by a *4.2*µ*m* epi film doped with boron to $1x10^{15}/cm^3$. Device wells are formed using a PBL LOCOS technique and a *6000Å* field oxide grown. N and P regions are implanted to form the wells followed by a *120Å* thermal gate oxide. 3000Å of amorphous silicon is deposited and given a blanket phosphorus implant to complete the gate electrode. The gate electrode is now patterned and etched followed by the implant of the n^- and p^- LDD regions. A PECVD oxide is used to form the side wall spacers and the source/drain regions for the nMOSFET and pMOSFET transistor are formed using implantation. An RTA anneal at *1025°C* for *40* seconds is used to activate all implants.

4.0 Process Simulation.

Simulations of the above process flow were carried out using SUPREM3, a 1-D process simulator capable of modeling RTA processes. Simulations have been carried out up to and including the source/drain RTA. The nMOSFET channel profile is illustrated in figure 1 and the pMOSFET channel profile in figure 2. In both of these devices the natural threshold voltage has been set by the well implants.

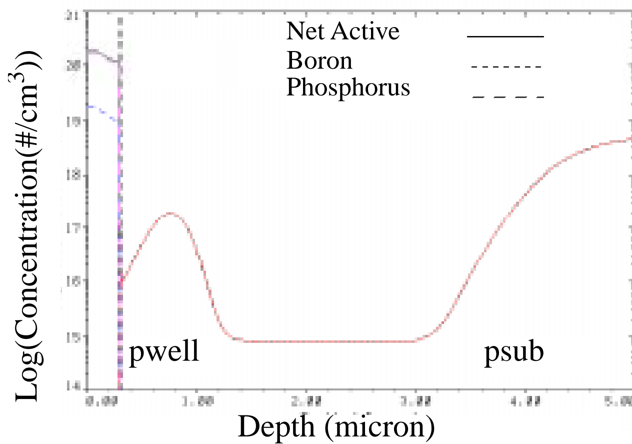


Fig. 1: Simulated 1-D "natural" nMOSFET channel profiles.

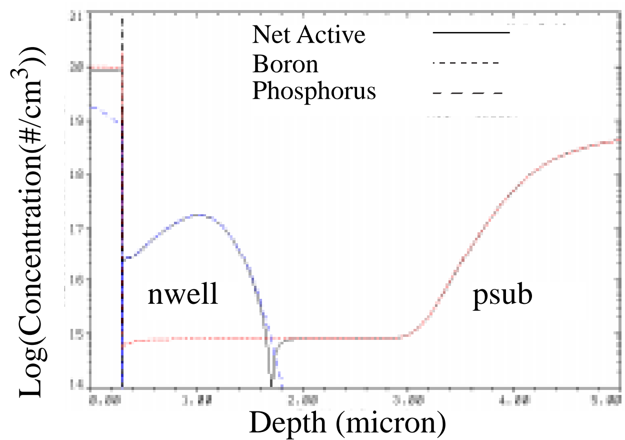
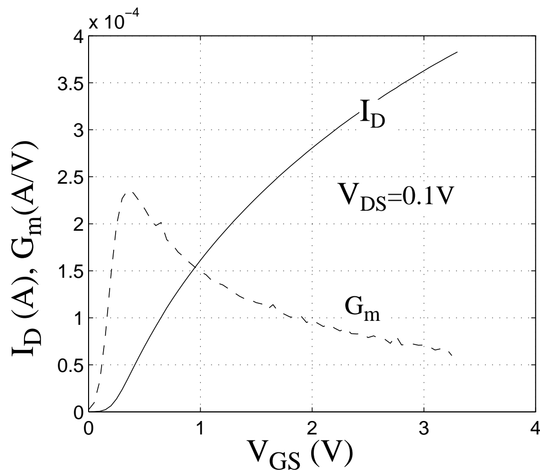


Fig. 2: Simulated 1-D "natural" pMOSFET channel profiles.

5.0 Device Characteristics

The threshold voltages of short channel (*0.5*µ*m*) nMOSFET and pMOSFET devices are measured to be *202*mV and *197*mV respectively. Figures 3 and 4 show the I_D and G_m versus gate voltage for a 20µ*m/0.5*µ*m* nMOSFET and a *20*µ*m/0.5*µ*m* pMOSFET biased at $V_{DS}=0.1V$ respectively. Subthreshold slopes are about *78*mV/decade as illustrated in figures 5 and 6.



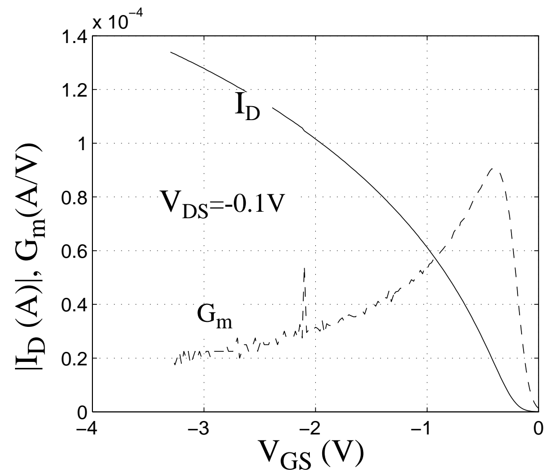
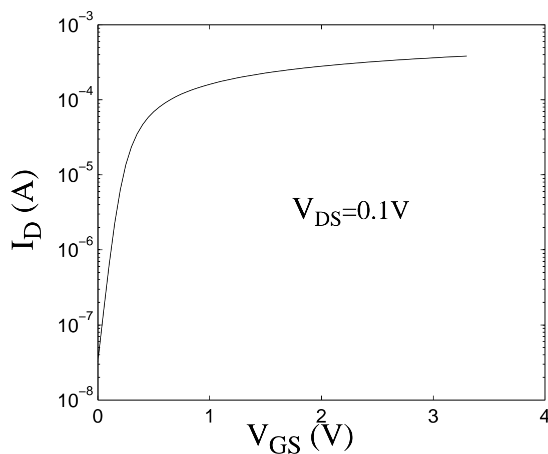


Fig. 3: Measured I_D (A) and G_m (A/V) versus V_{GS} (V) for "natural" nMOSFET.

Fig. 4: Measured $|I_D$ (A)$|$ and G_m (A/V) versus V_{GS} (V) for "natural" pMOSFET.



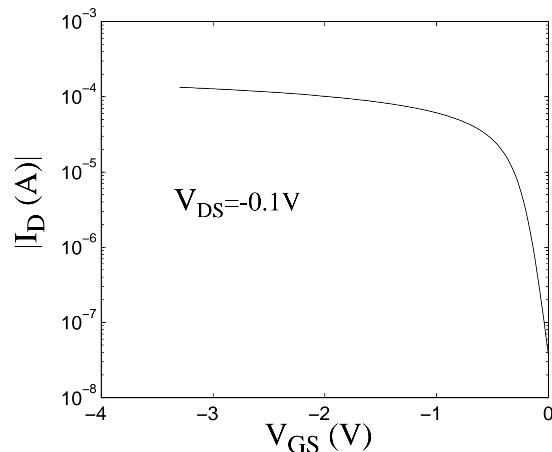


Fig. 5: Measured "natural" nMOSFET subthreshold characteristics

Fig. 6: Measured "natural" pMOSFET subthreshold characteristics

6.0 Conclusions

This paper showed that low threshold voltage "natural" MOSFETs in a *0.5*µ*m* dual poly gate CMOS process can be optimized for 1V mixed-signal applications.

Acknowledgments

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References

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