A 4th Order SC Bandpass ΣΔ Modulator Designed on a Digital CMOS Process

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Abstract

This paper presents a 4th order bandpass ΣΔ modulator which is about 30% faster than a previously reported [1] counterpart. Higher speed is achieved without any increase in power dissipation or chip area. This modulator is implemented on a single poly digital CMOS process using SC resonators. It is shown that a resonator built with two SC analog delay circuits in a negative feedback loop is insensitive to capacitor non-linearity. Thus, pMOSFETs operating in strong inversion are used as capacitors. The complete design was verified in the Eldo analog simulator.

1.0 Introduction

Bandpass ΣΔ modulators allow A/D conversion to be performed on narrow-band signals at IF frequencies. These A/D's are useful in some communication systems such as: AM radio, digital radio, and high speed modems.

In this paper a fourth order bandpass ΣΔ modulator is discussed. This modulator is derived from a second order low pass prototype (double integration sigma delta modulator) using a $z^{-1} \rightarrow -z^{-2}$ transformation. A SC implementation of this modulator using cascade of resonators is presented. It is shown, through analysis of the opamp settling time, that the modulator proposed in this paper is about 30% faster than the one in [1].

To be compatible with digital VLSI technologies, pMOSFETs are used as capacitors (instead of double poly capacitors). Analysis of the unity gain SC delay element shows that this architecture is insensitive to capacitor non-linearity. Thus using MOSFET gate capacitors does not compromise the performance of the resonator or degrade the linearity of the bandpass ΣΔ modulator.

The modulator proposed in this work uses resonators with a gain of half. A circuit technique to realize such a resonator that is insensitive to capacitor non-linearity is also discussed.

2.0 Bandpass ΣΔ modulator

The structure of a basic one-bit sigma delta modulator comprised of a loop filter H(z) and a quantizer Q is shown in figure 1. A bandpass sigma delta modulator is obtained by choosing a bandpass filter (e.g. a resonator) for $H(z)$. The noise transfer function of this modulator will have a band-reject shape. Thus, the quantization noise is pushed away from the signal band at the desired center frequency.

2.1 Transfer function design

A simple way of designing bandpass sigma delta modulators is to perform a lowpass to bandpass transformation. One such transformation in discrete-time domain is achieved by a $z^{-1} \rightarrow -z^{-2}$ change of variable, where zeros of the lowpass prototype are mapped from DC to $f_s/4$. The stability and SNR characteristics of the resulting bandpass modulator will be identical to that of the low pass prototype [2]. In the following we apply this transformation to a second order lowpass ΣΔ modulator.

$$H_{lp}(z) = \frac{z^{-1}(2 - z^{-1})}{(1 - z^{-1})^2} \quad (1)$$

$$H_{bp}(z) = \frac{-z^{-2}(2 + z^{-2})}{(1 + z^{-2})^2} \quad (2)$$

This fourth order bandpass ΣΔ modulator (2) is guaranteed to be stable due to the stability of the second order low pass (1) prototype.

Lowpass ΣΔ modulators are usually implemented by a cascade of integrators. A natural choice for bandpass modulators seem to be a cascade of resonators. One such architecture is shown in figure 2. The values of $k1$ and $k2$ are found to be -0.5 and 2 respectively. Since the second resonator is followed by a high gain quantizer the coefficient k_2 is irrelevant [3] and is set to 0.5, as is the coefficient of the first stage. This architecture is a direct map of the lowpass ΣΔ modulators in [3] to bandpass by transforming integrators to resonators. Analogous to the low pass prototype, the signal swings at the output of the resonators are almost within the full scale input range. Simulation shows that the fourth order bandpass in [1] exhibits much larger signal swing at the output of its resonators i.e., it has a lower MSAR (Maximum Stable Amplitude Range) and consequently lower SNR.

2.2 Resonator and Modulator Designs

The SC resonators can be implemented in several different ways. In [4], resonators are implemented using LDI and FE integrators. Another approach is to use two SC delay cells in a negative feedback loop [1], as shown in figure 3. Here, the latter design is used because it is

slightly faster [4], and also because this structure is immune to capacitor non-linearity (as discussed in section 3.3). A SC implementation of the 4th order bandpass ΣΔ modulator based on delay elements is shown in figure 4. All the capacitors are identical (C_u) except for the four marked by asterisk which have a value of $2C_u$. The worst case opamp loadings for both this structure and the one in [1] are shown in figure 5. The settling time constant of the design presented here is 30% less than the one in [1].

3.0 SC Implementation on a Digital Process

SC circuits are traditionally implemented in analog CMOS processes where linear double poly capacitors are available. However, in some SC circuits the linearity of the capacitor is not a requirement (see section 3.3) and therefore MOSFET gate capacitance can be used.

3.1 MOSFET Capacitor

The C-V characteristic of an nMOSFET is shown in figure 6. The gate capacitance is relatively flat in the accumulation ($v_{gs} < 0$) and the inversion ($v_{gs} > V_t$) regions. A negative back bias postpones the inversion and thus the linear portion of the C-V curve is reduced. In an n-well process, pMOSFETs can be used as capacitors without any back bias (bulk shorted to source and drain).

The value of the C_{gs} changes depending on v_{gs} from C_{ox} to C_{dep}. This means that the kT/C noise consideration must be based on C_{dep} (the lower value of C_{gs}) and the settling time requirement must be satisfied for C_{ox} (the upper value of C_{gs}). Obviously, this would not be an optimum design. Therefore, MOSFET capacitors must be biased properly such that only the flat part of the inversion or accumulation regions are used. This requires an opamp with different input and output common mode levels.

3.2 Cascode opamp

A fully differential non-folded cascode opamp [5] was designed in a 0.5um technology to fulfill the requirement of having different input and output common mode voltages. Some of the Opamp's characteristics are as follows:

- DC gain =62dB
- UGBW=800MHz (1pF load)
- Phase margin = 60°
- Input common mode voltage $V_{icm} = 1.3v$
- Output common mode voltage $V_{ocm} = 3v$

If the output signal swing is $1.0v$ then $2.2v < v_{gs} < 1.2v$. That is an acceptable range in the C-V curve.

3.3 SC delay cell

Figure 7 illustrates the unity gain delay cell implemented with pMOSFET capacitors. At the end of ϕ_1 the voltage across C_1 is $(V_{ocm} - V_{icm}) + v_{in}$. During ϕ_2 the charges on capacitor C_1 will be transferred to C_2 and at the end of ϕ_2 the voltage on capacitor C_2 will be $(V_{ocm} - V_{icm}) + v_{in}$. Thus, at the end of ϕ_2 capacitor C_2 is biased at the same voltage that capacitor C_1 was biased at the end of ϕ_1. This means that both C_1 and C_2 have identical v_{gs} and therefore (from figure 5) have equal capacitances. Similarly, at the end of the next ϕ_1 phase capacitor C_3 is also biased by $(V_{ocm} - V_{icm}) + v_{in}$. Thus, non-linearity of the capacitors in this configuration is irrelevant to the accuracy of the circuit.

Resonators are implemented with two SC delay cells in a negative feedback loop. To obtain a resonator with a gain of half, capacitor C_2 in the second delay cell must have a value of $2C_u$. The output of this resonator is valid during ϕ_2. Since the voltage across this capacitor is $(V_{ocm} - V_{icm}) + 2v_{in}$, this circuit is sensitive to capacitor non-linearity. However, linearity of the MOSFETs in strong inversion over a small range of v_{gs} (e.g. 1v) is sufficient for low resolution ($SNR < 40dB$) applications.

Capacitor C_2 can be implemented by eight MOSFET gate capacitors in a series-parallel configuration as shown in figure 8. If the input and output common mode levels are equal, all the MOSFETs see identical voltages across their V_{gs}. This structure is also insensitive to capacitor non-linearity. In this configuration the MOSFET capacitors operate in both accumulation and depletion regions.

3.4 Simulation

The fourth order bandpass ΣΔ modulator of figure 4, using pMOSFETs as capacitors, was simulated in the Eldo at the transistor level. The sampling frequency was set to 102.4MHz and signal was at 25.5MHz with an amplitude of $\pm 0.25v$. FFT on 1024 output bits was carried out in MATLAB and the resulting spectrum is shown in figure 9. The noise shaping is clearly seen; however, due to the small number of FFT points this simulation only shows 28.5dB SNR (36dB expected) over a band of 5MHz.

4.0 Conclusion

An architecture for high speed, fourth order bandpass ΣΔ modulators was presented and it was shown that is it 30% faster than a previously reported one. It was shown

that resonators implemented with SC delay cells are immune to capacitor non-linearity. A SC bandpass ΣΔ design which is compatible with digital VLSI CMOS processes (using MOSFET capacitor) was also described.

Acknowledgment

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References:

[1] L. Longo, B. Horng, "A 15b 30kHz Bandpass Sigma-Delta Modulator," in *Proc. ISSCC*, San Francisco, CA, Feb. 1993, pp. 226-227.

[2] S. Jantzi, R. Schreier and M. Snelgrove, **"The Design of Bandpass Delta-Sigma ADCs,"** chapter in *Delta-Sigma Data Converters*, IEEE Press, to appear.

[3] B. Boser, B. Wooley, "The design of sigma-delta modulation analog to digital converters," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1298-1308, Dec. 1988.

[4] F.W. Singor, W.M. Snelgrove, "10.7MHz Bandpass Delta-Sigma A/D Modulators," *Proc. of IEEE 1994 CICC*, May 1994, pp.163-166.

[5] D. Senderowicz, "CMOS Operational Amplifiers," in J. Franca and Y.Tsividis, Eds., *Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing*, Prentice Hall, 1993

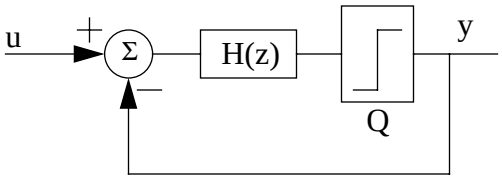


Figure 1: Basic structure of a ΣΔ Modulator

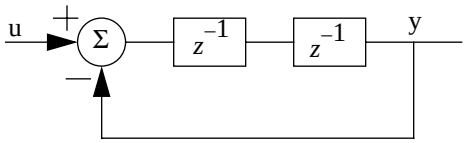


Figure 3: Resonator using delay cells

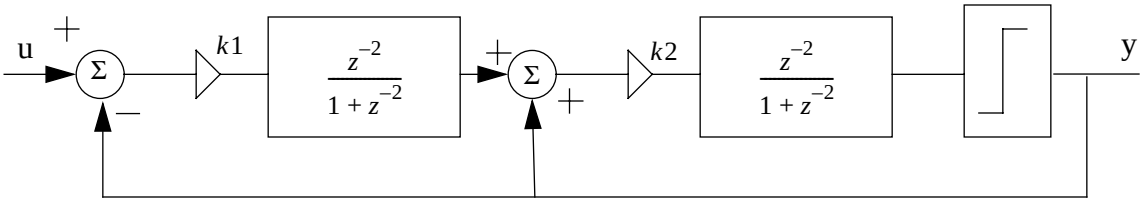


Figure 2: Fourth order double resonator bandpass sigma delta modulator

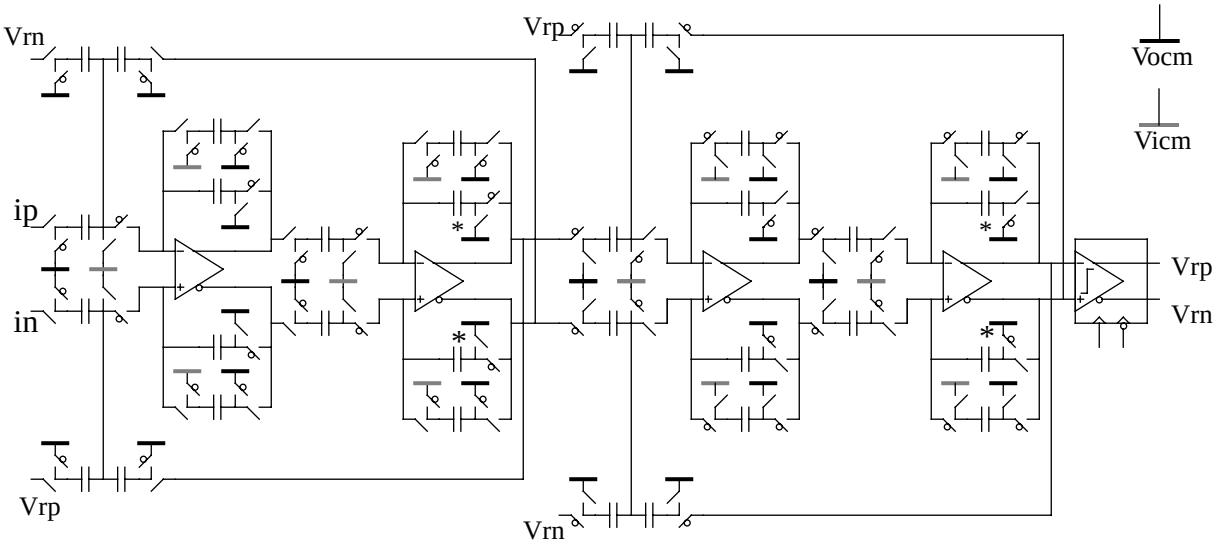
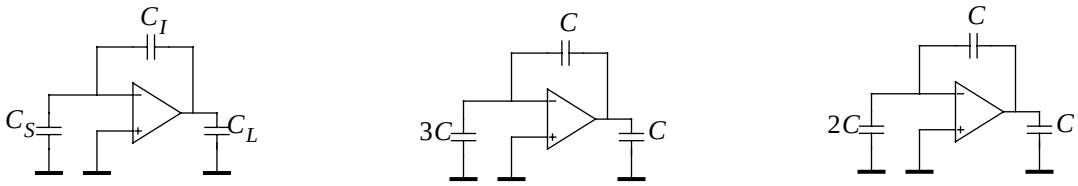


Figure 4: SC implementation of the 4th order bandpass of Figure 2



$$\tau = \frac{1}{\beta\omega_t} \quad \beta = \frac{C_I}{C_I + C_S}$$

$$\omega_t = \frac{g_m}{C_L + (C_I \| C_S)}$$

First op amp (ϕ_2)

$$\tau = 7\frac{C}{g_m}$$

Second Opamp (ϕ_1)

$$\tau = 5\frac{C}{g_m}$$

(a) (b) (c)

Figure 5: Worst case opamp loading (a) settling time equations
(b) Bandpass in [1] (c) Present work

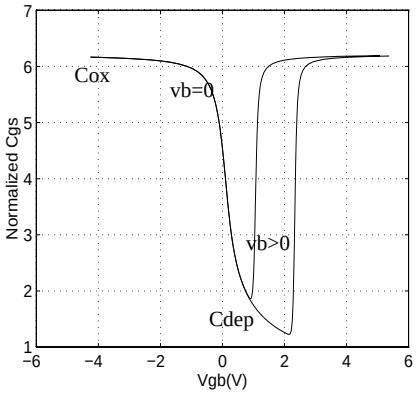


Figure 6: MOS C-V Curve

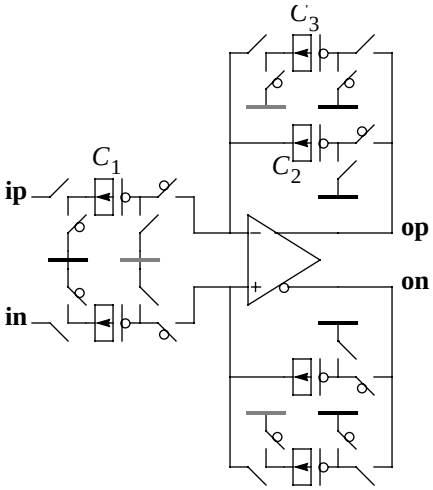


Figure 7: SC Unity gain delay cell
using pMOSFETs as capacitors

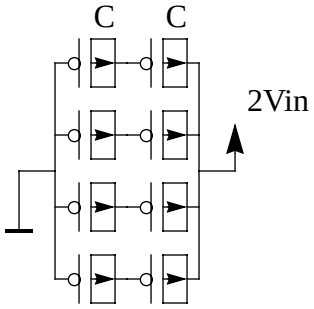


Figure 8: Capacitor of value 2C built from
8 MOSFETs. Voltages across all
MOSFETs are equal to Vin.

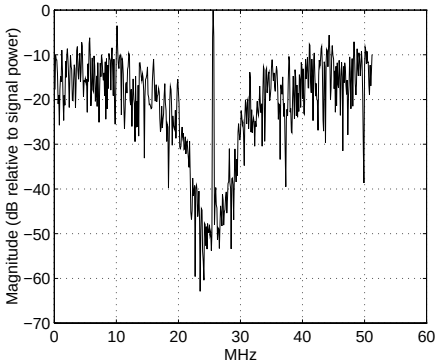


Figure 9: Simulated output spectrum of
the 4th order bandpass modulator