Low Voltage SC Circuit Design with Low -V_t MOSFETs

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Abstract

In this paper, low threshold voltage (V_t) "natural" transistors, available in some n^+/p^+ dual poly gate CMOS/ BiCMOS processes [1], are proposed for low voltage switched capacitor circuit design. The impact of the subthreshold off-current of these low V_t devices on the performance of analog switched-capacitor (SC) circuits is analyzed. Methods for reducing the subthreshold off-current in analog switches are discussed and two new switch topologies (series transmission gate and composite switch) addressing this problem are presented.

1.0 Introduction

Analog integrated circuits are usually implemented using switched-capacitor (SC) techniques due to their high circuit accuracy. For low-voltage design, the most critical component in an SC circuit is the transmission gate switch which requires a gate voltage of at least $2V_t$ for proper, full-swing (strong inversion) signal handling [2]. In general, to achieve full signal transmission through a switch with acceptable on-resistance, either the gate voltage must be increased (i.e., clock multiplication if $V_{DD}<2V_t$) [3], or the threshold voltage of the MOSFETs must be reduced. The former solution requires extra circuitry for voltage multiplication, may need an off-chip capacitor, and is noisy. The second solution solves the on-resistance problem, but may require process modification [4]. It also raises concerns regarding the leakage current during the "off" phase. However, the second approach is compatible with the future of CMOS technology and low power digital design [7,8], because power supply scaling will eventually force V_t down-scaling. Moreover, in some dual n^+/p^+ poly gate processes [1], low-V_t MOSFETs (called "natural" transistors) are available without requiring any extra masks.

In the following sections, the "natural" MOSFETs and associated subthreshold leakage off-current are briefly described. Then impacts of the leakage off-current on the precision of SC circuits are analyzed. Finally, methods and circuit techniques for reducing the leakage off-current through analog switches are discussed.

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2.0 Low V_t Natural MOSFETs

As channel lengths of MOSFET transistors are shrunk to *0.5μm* and below, buried-channel pMOSFET devices with strong short-channel effects must be replaced with surface channel devices. This requires a dual poly gate technology, where n^+ poly is used for nMOSFET and p^+ poly is used for pMOSFET. In some dual n^+/p^+ poly gate processes [1], it is possible to mask out the threshold adjust implant and obtain the low-V_t MOSFETs called "natural" transistors. The threshold of the natural transistors is about *0.2V-0.3V* which is suitable for low voltage (e.g., $V_{DD} = 1\,\mathrm{V}$) design.

2.1 Subthreshold off-Current

A turned off MOSFET ($v_G=0$) operates in weak inversion mode where drain current is exponentially dependent on the value of "v_{GS}-V_t". In saturation (i.e., when drain-source voltage is much greater than the thermal voltage, *25mV@*room temperature), the subthreshold off-current is given by the following simplified equation

$$i_{off} = I_{D0}10^{-(v_S + V_t)/S} \quad (1)$$

where, I_{D0} is the value of the drain current when the gate to source voltage is set to V_t [2] and S is the subthreshold swing. Equation (1) shows that as V_t reduces, the off-current increases, causing degradation in the precision of the analog SC circuits, as described below.

2.2 Effects of leaky switches in an SC integrator

A stray-insensitive SC integrator and its associated non-overlapping clocks (ϕ_1 and ϕ_2) are shown in Figure 1. For rail-to-rail signal handling, switch $S1$ is implemented with a full transmission gate (an nMOSFET and an pMOSFET in parallel) and all the others switch to analog ground ($V_{ag} \approx V_{DD}/2$) and thus can simply be nMOSFET transistors.

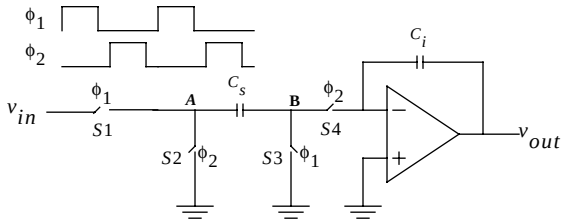

Figure 1: A non-inverting SC integrator

Subthreshold leakage current through the "off" switches cause error in the circuit response. In the following, error voltage on nodes A and B for different periods of a complete clock cycle is analyzed.

During ϕ_1: The equivalent circuit of the SC integrator during ϕ_1 is shown in Figure 2.

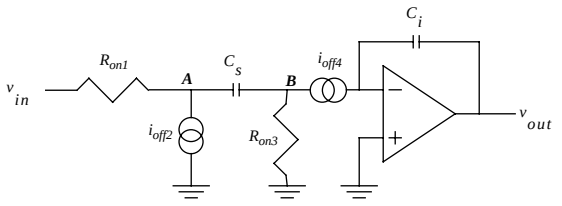

Figure 2: Equivalent Circuit of Figure 1 during ϕ_1

The leakage off-current i_{off2} (through $S2$) is largest for signal level closest to V_{SS}. This causes an error voltage (Δv_1) in the transmission of signal from v_{in} to V_A.

$$\Delta v_1 = R_{on1} i_{off2} \tag{2}$$

where $R_{on} = 1/g_{on}$ and g_{on} is:

$$g_{on} = \mu C_{ox}(W/L)(v_{GS} - V_t) \tag{3}$$

This error voltage (Δv_1) is a nonlinear function of the input signal and causes offset and gain errors as well as distortion at the end of the cycle at the output. The maximum value of Δv_1 occurs when v_{in} reaches its minimum, i.e $v_{in} = V_{SS}$. Assuming $S1$ and $S2$ have the same $(W/L)_n$, the maximum error voltage is:

$$\Delta v_1\big|_{max} = \frac{\phi_T^2}{V_{DD} - V_t} 10^{-\frac{V_t}{S}} \tag{4}$$

where ϕ_T is the thermal voltage ($kT/q = 25mV$ @ room temperature). A required dynamic range implies an upper limit on the error voltage and from equation (4) one can find the minimum required threshold voltage. In the same way, for a given dynamic range and R_{on} the maximum tolerable i_{off} can be found. For example, a *100dB SNR* with a power supply of *1V*, and an on-resistance of *10kΩ* requires an off-current of less than *1nA*.

Switch $S4$ is biased at mid-rail (analog ground and virtual ground); thus, ideally there is no potential across this switch and leakage off-current through it is zero. However, due to non-idealities (finite opamp gain, etc.) there will be some voltage across switch $S4$. Since this switch is biased at mid-rail the subthreshold leakage is reduced by two different mechanisms; threshold increase due to body effect, and negative gate to source voltage. The subthreshold leakage current will be 'p' decades below I_{D0}, where p is:

$$p = (V_{DD}/2 + V_t)/S \tag{5}$$

For some typical values $W/L = 10/1$, $I_{D0} = 100nA$, and $V_{DD} = 1V$, a device with $V_t = 180mV$ and $S = 90$ mV/decade will have a leakage off-current of about 0.1pA which is very small; comparable to junction leakage.

Non-overlapping period: The equivalent circuit of SC integrator during the non-overlapping period is shown in Figure 3. As discussed in the previous section the leakage off-current through $S3$ and $S4$ are negligible.

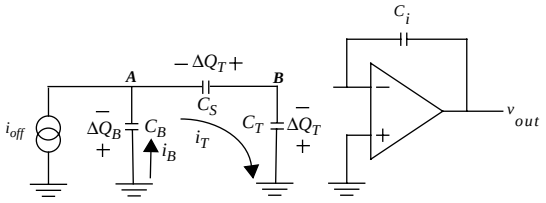

Figure 3: Equivalent Circuit of Figure 1 during the non-overlapping period.

In this circuit C_T and C_B are the top and bottom plate of capacitor C_S to ground. The sum of leakage currents through $S1$ and $S2$ is called i_{off}, which is provided by i_T and i_B.

These leakage currents cause a change in charge across each capacitor as shown in the above Figure. The error charge ΔQ_B across C_B is causing no net error at the output (stray insensitive configuration), because during ϕ_2 node A is shorted to analog ground and ΔQ_B is dumped to ground. The error charges ΔQ_T on capacitors C_S and C_T have different polarities (during ϕ_2) and as such cause no net error at the output.

During ϕ_2: At the beginning of ϕ_2, the voltage at node B is changed suddenly from analog ground to $-v_{in}$. This can cause switch $S3$ to become leaky (for v_{in} close to V_{DD} the source of $S3$ will fall to V_{SS} resulting in $v_{GS} = 0$). Any charge lost by $S3$ will cause an error voltage (Δv_2) at the output,

$$\Delta v_2 = \int_0^{\delta t} (i_{off3}/C)dt \tag{6}$$

where δt is the time taken for the opamp to force V_B back to virtual ground.

3.0 Methods of Reducing the off-Current

As described in the previous section, subthreshold off-current through analog switches implemented with low threshold voltage MOSFETs ($V_t < 200mV$) introduces error in SC circuits and reduces the dynamic range of the

analog operations. Methods of reducing the off-current through analog switches are described in the following.

3.1 Limiting the Signal Swing

If the signal swing is reduced by ΔV from each rail, the subthreshold off-current (1) will be reduced by $\Delta V/S$ decades. Notice that for a $\Delta V=200mV$ (which may be required for drain-source saturation voltage in the amplifier) and $S=90mV/decade$, the off-current is reduced by more than *100* times. Measurements of some natural transistors (V_t = $200mV$) correlates well with theory and simulation results.

3.2 Adjusting V_t by back bias

A major problem with low V_t MOSFET transistors is the threshold voltage variation due to processing errors (about $\pm 100mV$) and temperature (about $-1.5mV/°C$). These can have a compounding effect and increase the off-current drastically. The V_t can be set to a constant by adjusting the substrate voltage. Figure 5 shows negative feedback circuitry which generates a substrate voltage to keep V_{tp} equal to a constant *Vref* [5,8]. The amplifier in this circuit operates with supply voltages of V_p and V_{DD} where $V_P>V_{DD}$ is the positive supply (generated by a charge-pumped circuit) to keep source/drain and bulk junctions reversed biased at all times.

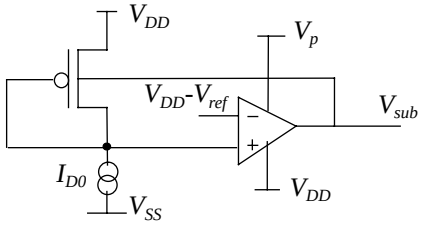

Fig. 5: Negative feedback V_t adjust Circuit

3.3 Series transmission gate Switch

In a stray insensitive SC circuit (e.g., Fig. 1), off-switches have one side connected to analog/virtual ground (either directly or through another switch). An nMOSFET switch during the off-phase is shown in Figure 6a.

For a $V_A>V_{DD}/2$ the subthreshold leakage off-current is low because of the negative gate to source voltage and an increase in V_t due to back bias. The i_{off} current is,

$$i_{off} = I_{D0}10^{-p} \quad (7)$$

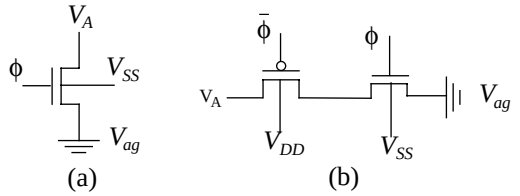

Fig. 6: (a) nMOSFET and (b) Series transmission gate switches

where $p=(V_{DD}/2+V_t)/S$. However, as voltage V_A drops below $V_{DD}/2$, subthreshold leakage increases exponentially and reaches a maximum for $V_A=V_{SS}$. In this case the exponent ($p=V_t/S$) is small for low V_t devices and results in a large off-current. In a similar situation a pMOSFET switch has the opposite behavior. For V_A close to V_{SS}, the leakage off-current is low and increases as V_A is raised from $V_{DD}/2$ to V_{DD}.

A very low leakage switch (with one side tied to analog ground), is obtained by a series transmission gate switch as shown in Figure 6b. The maximum subthreshold leakage off-current through this switch is similar to an nMOSFET switch with $V_A=V_{DD}/2$, as analyzed previously. Figure 7 illustrates the subthreshold leakage current through an nMOSFET and a series transmission gate (STG) switch. Threshold voltage of MOSFETs are set to 110mV and $(W/L)_p = 2(W/L)_n = 10$.

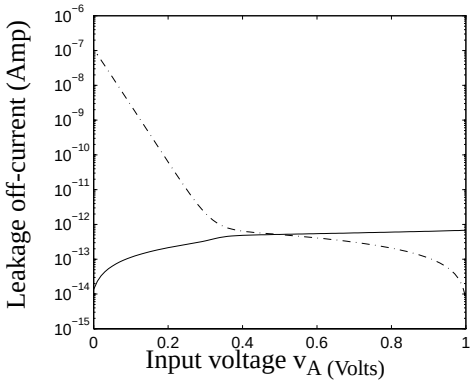

Fig. 7: Leakage off-current through an nMOSFET switch (-.-.) and a STG switch (___)

The leakage off-current through STG switch is very low (~pA) while low V_t nMOSFET has a relatively high leakage off-current (~10nA) for low input voltages.

A series transmission gate switch has higher on-resistance than a simple nMOSFET, but only by a factor of *2* or *3* (depending on the size of the pMOSFET device). Assuming $V_{tn} = V_{tp}$, $\mu_n C_{ox}(W/L)_n = \mu_p C_{ox}(W/L)_p$ and using the simple equations of (3) for the on-conductance of MOSFETs, it can be easily shown that the maximum on-conductance for a STG occurs at $V_{DD}/2$. This is exactly where all the switches to analog ground are operating. Simulation for on-conductance, Figure 8 confirms the above analysis.

A drawback of the series transmission gate switch is the limited input signal swing. This switch cannot conduct signals that are within a V_t of the supply rails.

In a multi-threshold process, such as dual poly-gate CMOS, the high V_t (threshold adjusted) transistors can be used in a parallel transmission gate (TG) configuration along with the series transmission gate

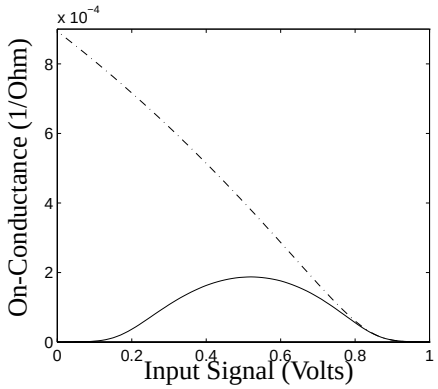

Fig. 8: On-conductance of the nMOSFET and STG switch versus input signal

switch to handle rail-to-rail switch capability. The composite switch is shown in Figure 9 (bold type devices are the V_t adjusted MOSFETs).

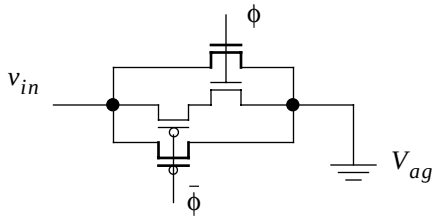

Fig. 9: Full swing composite switch

In this configuration, the high V_t parallel transmission gate conducts well when the signal is close to the rails, and low V_t series transmission gate conducts well when the signal is at mid-rail. The on-conductance and leakage through this composite switch is simulated along with high V_t and low V_t parallel transmission gates and are illustrated in Figures 10 and 11.

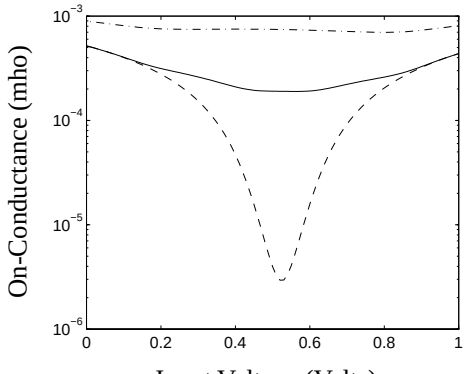

Fig. 10: On-conductance for low Vt TG (-.-.), high Vt TG (---), and Composite switch (___).

Simulations: The functionality of all the circuits has been verified by analog simulation in an experimental *0.5*µ*m* dual poly gate CMOS process. Since an accurate MOSFET subthreshold behavior is required for these simulations, MISNAN [6], a physically based model, was used. Threshold voltage for "natural MOSFETs"

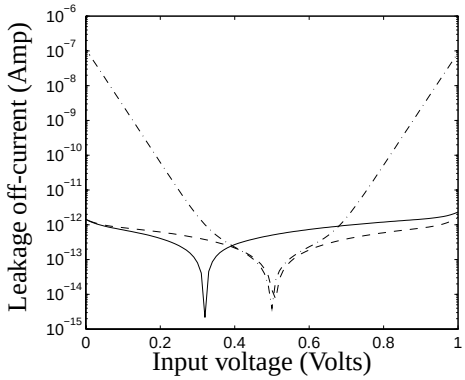

Fig. 11: Leakage off-current through low Vt TG (-.-.) high Vt TG (---), and composite switch (___)

are about 150mV and threshold adjusted MOSFETs (high V_t) have a threshold voltage of 0.5V.

4.0 Conclusion

This paper showed that low voltage SC circuit design is possible using natural transistors. Low threshold voltage devices are leaky and can cause inaccuracies in analog SC circuits. Methods of reducing the subthreshold off-current leakage in analog switches were presented.

Acknowledgment

The authors would like to acknowledge the financial support received from Bell Northern Research and thank Tom MacElwee for providing the "natural" MOSFETs and helping in the measurements.

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