Low Voltage SC Circuit Design Using Short-Channel MOSFET Switches

Seyfi S. Bazarjani‡, W.M. Snelgrove, N.G. Tarr, and K. Howlett*

Department of Electronics, Carleton University, Ottawa, Ontario, Canada K1S 5B6

* Telecom Microelectronics Centre, Northern Telecom, P.O. Box 3511, Station C, Ottawa, Ontario, Canada K1Y 4H7

Tel: (613)763-8473, E-mail: seyfi@bnr.ca or seyfi@doe.carleton.ca

Abstract

Analog switches, which are known to be the bottle-neck for reducing the supply voltage, are analyzed. MOSFET transistors with channel lengths shorter than the minimum feature size (L_0) in a given technology are proposed for use as switches operated at a low supply voltage. These MOSFETs have lower threshold voltage and higher punchthrough currents compared to a transistor of L_0 length (due to short channel effects). Measurements and Medici simulations show that a narrow window of optimum channel length exists where punchthrough current is acceptable for low voltage short channel switches.

1.0 Introduction

Low voltage circuit design in existing 5V BiCMOS (CMOS) processes is desired in applications requiring low power consumption, battery operation, line fed telecommunication capability, etc. Reducing the supply voltage degrades the performance of digital circuits. However, speed loss is not significant (down to supply voltage of $V_{DD} = 3V_t \approx 2.4V$) and is tolerated in many applications. If higher speed is required, parallel architectures can be employed. Analog switched-capacitor (SC) circuit design, on the other hand, becomes more challenging. Low-voltage/high-speed operation (>10MHz) of SC circuits is limited by the gate voltage of a switch that must be more than $V_c = V_{tn} + V_{tp}$ for full swing signal handling (to keep MOSFETs in strong inversion). In a typical BiCMOS (CMOS) process with threshold voltages $V_{tn} = V_{tp} = 0.8V$, such as Northern Telecom's 0.8µm BiCMOS process (BATMOS) [1], temperature, process variation, and back bias (of 1.5V) together bring V_c to about 2.7V. Thus, high speed SC circuit design with a supply voltage less than 3V will be problematic in this technology. Increasing the width "W" of a MOSFET helps to reduce switch on-resistance at the expense of increased clock feedthrough and channel charge injection. For extremely small $V_{on} = V_{gs} - V_t$, a better solution might be to apply clock voltage multiplication to increase v_{GS}, although this technique requires extra circuitry that is noisy and may need off-chip capacitors. In this paper, a simple third solution is presented. MOSFET transistors with channel lengths shorter than the minimum feature size of a given technology (called "short-channel devices" hereafter), have lower threshold voltage due to short channel effects (SCE). These "short-channel devices," can be used as efficient switches due to higher V_{on} (as a result of lower V_t), higher aspect ratio(W/L) for the same width, and lower charge injection (based on channel length reduction). However, undesirable SCEs, such as increased subthreshold swing and punchthrough current, set a limit to the minimum channel length acceptable for the "short channel devices." Since these devices will be used solely as analog switches, a small number of them (typically less than hundred) are needed on a chip. Thus device yield may not be degraded significantly. Furthermore, low voltage operation (2.5V) allows the use of short-channel devices as switches with acceptable punchthrough current. Medici, a 2-D device simulator, was used to find the minimum achievable channel length for a useful short-channel device. Measurements were also carried out on different sizes of "short-channel devices" to verify the simulation results. This technique was applied to an existing second order $\Sigma\Delta$ modulator designed in the BATMOS process for 3.3V operation. Modification was minor and involved changing all the switches. The new design which is expected to be capable of operating at $2.5 \pm 0.25V$ has been resubmitted for fabrication.

2.0 Switches

An ideal switch has the following properties: (a) zero on-resistance; (b) infinite off-resistance, i.e., no leakage current, and; (c) full signal swing capability. In a SC circuit, analog switches are implemented with MOSFET transistors which have non-idealities and limitations as described below.

- On-resistance: MOSFET transistors used as a switch operate in triode mode with on-resistance of approximately

‡ Currently on educational leave of absence from Northern Telecom/ Bell Northern Research.

$$R_{on} = 1/\left(\mu C_{ox}\frac{W}{L}V_{on}\right). \quad (1)$$

Two of these resistors along with a sampling capacitor (such as $S1$, $S3$ and C_s during ϕ_1 in Figure 1), constitutes an RC circuit with a time constant $\tau = 2R_{on}C_s$. At the end of the sampling phase the signal on the capacitor C_s contains an error due to incomplete settling. For a desired dynamic range ($DR = V_{signal}\big|_{rms}/V_{noise}\big|_{rms}$), assuming C_s is constant, a conservative value for on-resistance is determined by

$$T_s = 2(2R_{on}C_s)ln(DR) \quad (2)$$

where, T_s is the sampling period.

• Off leakage: MOSFET switches do not completely turn off when $v_G = 0$ due to subthreshold and/or punchthrough currents. The maximum allowable leakage current depends on the required dynamic range. During sampling phase ϕ_1, when switch $S1$ is closed and acts like a resistor of value R_{on}, and $S2$ is open with a total leakage current of i_{OFF}, an error is introduced. This sampling error (ΔV) must be less than the desired resolution. Assuming rail to rail signal swing, the following relationship must hold:

$$\Delta V = i_{OFF}R_{on} < V_{DD}/DR \quad (3)$$

• Full Signal Swing: A parallel nMOSFET and pMOSFET switch (transmission gate) has full swing capability. The minimum supply voltage required to fully turn on an analog transmission gate switch is

$$V_{DD} = V_{te,n} + V_{te,p} + 2V_{on} \quad (4)$$

where the effective threshold voltages, $V_{te,n}$, and $V_{te,p}$ are:

$$V_{te} = V_{t0}(Max) + \Delta V_t(T) + \Delta V_t(V_{SB}) \quad (5)$$

$V_t(Max)$ is the 3σ upper value of threshold voltage due to process variations, $\Delta V_t(T)$ and $\Delta V_t(V_{SB})$ are the threshold voltage changes due to temperature, and the back bias.

$$\Delta V_t(T) = a(25 - T) \quad (6)$$

$$\Delta V_t(V_{SB}) = \gamma(\sqrt{2\Phi_B + V_{SB}} - \sqrt{2\Phi_B}) \quad (7)$$

Here, T is temperature in degrees Celsius, and "a" is the slope of threshold voltage as a function of temperature, which is about 1-2mv/° C. Other parameters are, $\gamma \approx 0.5$: the body effect coefficient, Φ_B: the bulk potential, and V_{SB}: the source to bulk voltage.

3.0 Short-Channel Devices as Low-Voltage Switches

As the channel length of a MOSFET transistor is made smaller than a critical value (L_{min}), several 2-D phenomena known as short channel effects (SCEs) will occur. The onset of SCE is empirically given [2] by the following formula:

$$L_{min} = 8.8[r_j t_{ox}(W_S + W_D)^2]^{1/3} \quad (8)$$

Normally, process engineers select the minimum feature size of the technology (L_0) to be slightly greater than L_{min}.One of the characteristics of short channel devices is that threshold voltage rolls off quickly as channel length is reduced below L_{min} (Figure 2).

This is an interesting feature because low voltage switches require low V_t and high W/L for low on-resistance, both of which come with short channel devices. However, short channel devices might not properly turn off due to subthreshold conduction and punchthrough current. In addition, process variation adds to the complexity of the problem. A drawn channel length (L_0) can vary by "ΔL" due to error in lithography and etching. For channel lengths below L_0, this variation might be larger. Thus, the optimum channel length is selected such that devices with the absolute minimum channel length obtained on silicon have acceptable subthreshold and punchthrough currents.

3.1 Subthreshold Current

A MOSFET transistor with $v_{GS} < V_t$ operates in the weak inversion regime with drain current given by [3]:

$$i_{DS} = I_{D0}\frac{W}{L}e^{\left(\frac{v_{GS}-V_t}{n\Phi_t}\right)}\left(1 - e^{-\left(\frac{v_{DS}}{\Phi_t}\right)}\right) \quad (9)$$

For an off switch $v_G = 0$, and assuming $v_{DS} > 3\phi_t$ ($\phi_t > kT/q$), the subthreshold current is independent of drain to source voltage and (9) is simplified to:

$$i_{OFF} = I_{D0}\frac{W}{L}10^{-\frac{(v_S + V_t)}{S}} \tag{10}$$

Here, I_{D0} is the value of drain current for a unit transistor ($W/L = 1/1$) with gate to source voltage biased at the threshold voltage ($v_{GS} = V_t$), which is about 100nA in BATMOS. S is the subthreshold swing (v_{GS} change needed to increase i_{DS} by one decade) with a typical value of 86mv/decade in BATMOS.

For a desired dynamic range maximum tolerable i_{OFF} and, consequently, minimum $V_t + v_S$ can be computed. Note that subthreshold leakage is also reduced by increasing the source to bulk voltage (i.e. limiting the signal swing).

Medici simulation shows that devices with channel length as low as 0.4μm have a V_t of 0.5V.

3.2 Punchthrough Current

Short channel MOSFET devices are susceptible to barrier lowering that results in an unwanted current flow from drain to source. This phenomenon is affected by L and v_{DS}. For $v_{DS} = 0$, the peak potential barrier is lowered if the channel length is not larger than the sum of the two depletion region widths (source and drain to substrate). The barrier is lowered further for $v_{DS} > 0$, because field lines penetrate from drain to source [4]. Resulting punchthrough current has a two dimensional nature and no analytical model predicting it exists. Two dimensional computer simulation and experiments show that punchthrough current decreases as v_{DS} is lowered or negative bulk to source voltage is applied. A close observation of Figure 1 shows that all of the "off" switches have both back bias and v_{DS} is lower than $V_{DD}/2$. Off switches have one side connected to analog ground and the other side is connected either to virtual ground ($S3$ and $S4$), or signal voltage ($S1$ and $S2$). Thus, the maximum voltage across an off switch is:

$$v_{DS}\big|_{max} < (V_{DD}/2) - v_{signal} \tag{11}$$

and the bulk to source is reverse biased by: $v_{SB} = v_{signal}$.

Medici simulation of a 0.4μm device shows that for $v_{DS} = 1.5$ and zero gate, source, and bulk voltage the total leakage current is less than 10nA.

3.3 Experiments

Characteristics of different "short-channel devices" (all with $W = 10\mu m$) were measured for both nMOSFET and pMOSFET transistors. At supply voltage of 3V, the on-resistance of switches biased at mid-rail ($V_{SB} = 1.5V$ and $V_{DB} = 1.6V$) were measured. Results are shown in Table 1. Further measurements of the 0.6μm nMOSFET switch show that R_{on} of 1.25K is achieved with a supply voltage of 2.1V.

Figure 3 illustrates i_{DS} vs. v_{GS} characteristic of an nMOSFET with 0.6μm channel length under two different v_{DS} conditions.

Since the turn off leakage (i.e. $v_G = 0$) is of prime importance to us, i_{DS} vs. v_{DS} is also measured for the same device (a 0.6μm nMOSFET), with different back bias voltages. It is seen (Figure 4) that extremely low current leakage is obtained by setting the back bias to 0.5V. Both Figure 3 and 4 show current per width of the transistor. Measurements of a 0.6μm pMOSFET device gave similar results.

4.0 Conclusions

Short channel MOSFETs were proposed for low voltage/high speed SC circuits in a conventional 5V BiCMOS or CMOS process. Measurement and simulation show that in BATMOS, MOSFETs with channel length of 0.6μm can operate efficiently as a switch with supply voltages of $2.5 \pm 0.25V$.

Acknowledgments

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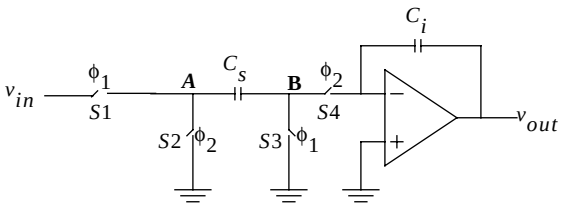

Figure 1: A non-inverting SC integrator

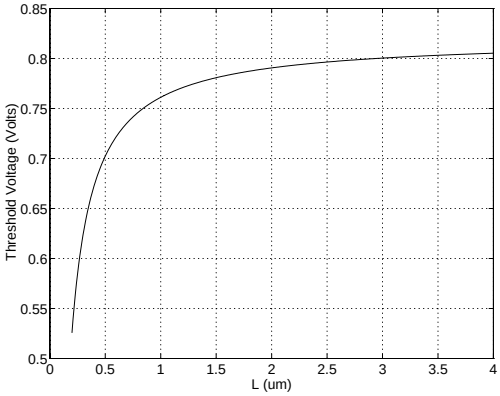

Figure 2: Threshold voltage as a function of channel length.

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Table 1: On-resistance of switches with W=10μm

Transistor Type	R_{on}		*%reduction*
	L=0.8μm	L=0.6μ*m*	
nMOSFET	*1.3K*	*0.709K*	*83%*
pMOSFET	*5.8K*	*3.2K*	*81%*

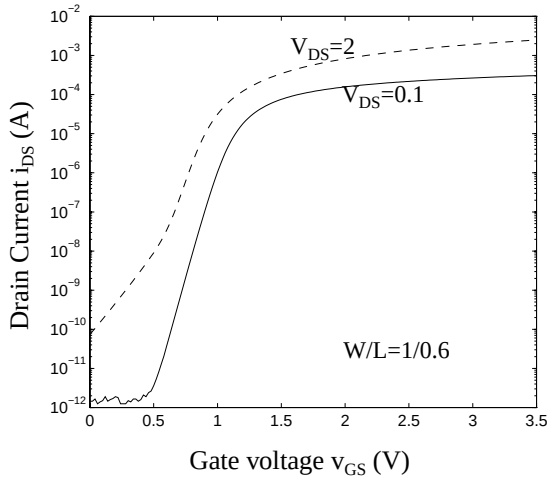

Figure 3: Drain current versus gate voltage for a 0.6μm nMOSFET

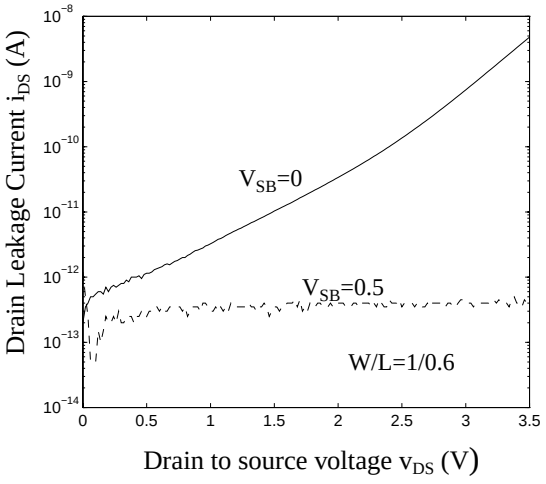

Figure 4: Drain leakage current versus drain to source voltage for a 0.6μm nMOSFET