High Speed Polyphase CIC Decimation Filters

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ABSTRACT

Polyphase structures for CIC (cascaded-integrator-comb) decimation filters are proposed in this paper. With the new structures, the proposed filters can operate at much lower sampling rate yet achieve almost the same performance as Hogenauer's CIC filters. They have advantages in high speed operation and low power consumption. Issues such as high speed commutator design, polyphase components, finite word length, truncation, and rounding have been discussed. Some important applications are also given in this paper.

1. INTRODUCTION

In digital radio receivers, the trend is to push DSP as close to the antenna as possible due to the many advantages of digital technology [1]. This means that we prefer either digitizing IF signals at the highest frequencies practical or even directly digitizing RF signals [2]. With the feasibility of a 3.2 GHz ΔΣ modulator [3], the DSP is pushing towards GHz rate for decimation. However, CMOS implementation of digital downconversion (or decimation) at such a high frequency could be a problem. Another challenge in wireless communications, especially in cellular handset devices, is low power consumption. To reduce the power, we can lower either the voltage supply or clock rate [4]. Lowering the voltage supply, however, will increase circuit delays and therefore put a bound on operation frequency. One solution to the above two problems is to use parallel processing.

Polyphase decomposition has been traditionally used to implement parallel structures in DSP. In this paper, two versions of polyphase decimation filters intended for high speed data stream are proposed. The polyphase decimators were derived from Hogenauer's structure [5] which has been proven to be very efficient.

2. CIC DECIMATION FILTERS

Hogenauer's CIC decimation filter [5], shown in Fig. 1, consists of N cascaded digital integrators operating at a high input sampling rate, f_S, and N cascaded differentiators at a low rate, f_S / R, where R is the integer downconversion factor. Its transfer function is

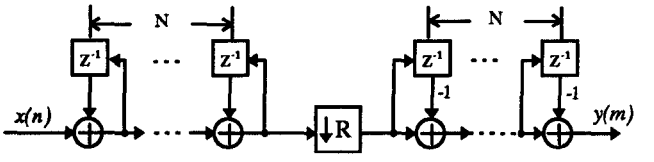

Fig. 1 A CIC decimation filter

$$H(z)=\left(\frac{1-z^{-R}}{1-z^{-1}}\right)^N \quad (1)$$

which is an N-stage sinc function. This kind of decimation filter is very efficient in these senses: 1) no multipliers; 2) no storage elements; 3) regular structure; 4) wide range of rate change; etc. Due to the droop around the cutoff frequency and aliasing within the band of interest, the choices of N and R are made to provide acceptable passband characteristics over the range from zero to the cutoff frequency. Generally speaking, the higher the first downconversion rate, f_S / R, relative to the Nyquist rate, f_N, the smaller the droop and the higher aliasing attenuation. However, this leaves more filtering to be done with a less efficient transversal or IIR decimator. Hogenauer [5] gave two tables for the design trade-off. For nth-order lowpass (or $2n$th-order bandpass) ΔΣ modulators, the compromise is to take the first downconversion rate to be four times the Nyquist rate [6]. In doing so, one has to compensate only small droop later in the low frequency stage.

The applications of CIC decimation filters seem to be in areas where high sampling rates make multipliers an uneconomical choice, such as in ΔΣ modulation data conversion. A key application could be digital IF/RF signal processing (both down and up conversion) for wireless communications (both handset and basestation).

3. POLYPHASE CIC DECIMATION FILTERS

A decimation filter at hundreds of MHz or even GHz rates is a must in the aforementioned examples. Parallel processing is a wise way to accommodate high speed and lower power consumption [4]. It also allows FPGAs to implement high speed decimation. In this section, polyphase decomposition will be used to implement parallel processing for decimation.

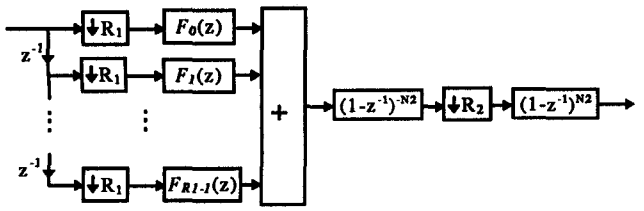

Fig. 2 Polyphase structure of the CIC decimation filter

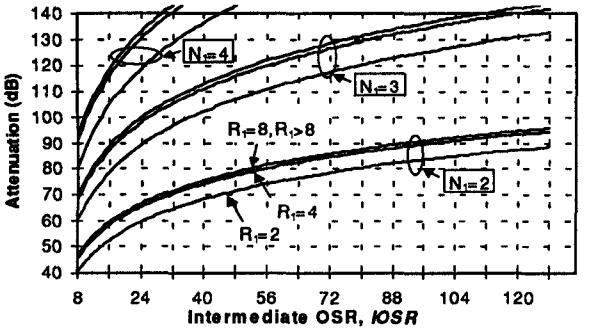

Fig. 3 Aliasing attenuation versus *IOSR*

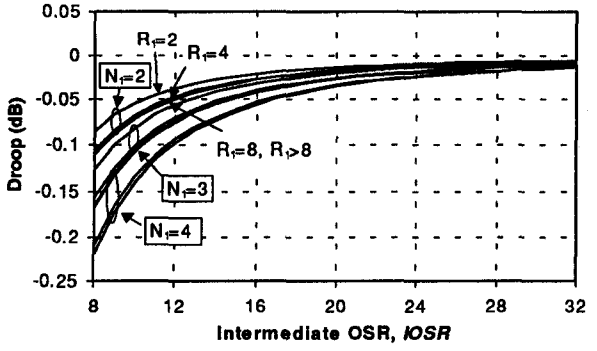

Fig. 4 Droop at cutoff frequency versus *IOSR*

Instead of using one CIC filter to decimate the high speed digital signal, here we use two (one N_1-stage and one N_2-stage). The downconversion factors for them are R_1 and R_2, respectively. Here we assume that R can be factored as $R_1 \cdot R_2$. Thus the transfer function is

$$H(z)=\left(\frac{1-z^{-R1}}{1-z^{-1}}\right)^{N1}\left(\frac{1-z^{-R}}{1-z^{-R1}}\right)^{N2}=H_1(z)H_2(z^{R1}) \quad (2)$$

Therefore

$$H_1(z)=\left(1+z^{-1}+...+z^{-(R1-1)}\right)^{N1} \quad (3a)$$

$$H_2(z)=\left(\frac{1-z^{-R2}}{1-z^{-1}}\right)^{N2} \quad (3b)$$

Performing polyphase decomposition [7] in (3a), we have

$$H_1(z)=\sum_{i=0}^{R1-1} z^{-i}F_i(z^{R1}) \quad (4)$$

TABLE 1. Polyphase components

N_1	2			3		
R_1	2	4	8	2	4	8
$F_0(z)$	(1,1)	(1,3)	(1,7)	(1,3)	(1,12,3)	(1,42,21)
$F_1(z)$	(2,0)	(2,2)	(2,6)	(3,1)	(3,12,1)	(3,46,15)
$F_2(z)$		(3,1)	(3,5)		(6,10,0)	(6,48,10)
$F_3(z)$		(4,0)	(4,4)		(10,6,0)	(10,48,6)
$F_4(z)$			(5,3)			(15,46,3)
$F_5(z)$			(6,2)			(21,42,1)
$F_6(z)$			(7,1)			(28,36,0)
$F_7(z)$			(8,0)			(36,28,0)

where $F_i(z)$ are polyphase components, operating at the rate of f_S / R_1. Thus the polyphase structure for CIC decimation filters can be built as shown in Fig. 2. $H_2(z)$ is simply a CIC decimation filter. To see how complex $H_1(z)$ is, we have to derive each polyphase component in (4) from (3a) for certain N_1 and R_1. Table 1 lists the most frequently used polyphase components. Note that the notation $(a_0, a_1, ...)$ represents a polyphase component $(a_0 + a_1 z^{-1} + ...)$. It can be seen that the polyphase components can be realized with the help of a small number of adders and shifters only.

The choice of N_1 is important for the polyphase CIC filter design. Smaller N_1 will result in larger aliasing. Look at the plot shown in Fig. 3 for the aliasing attenuation versus intermediate oversampling ratio, $IOSR = (f_S / R_1) / f_N$, one can see that N_1 can be taken to be $N_1 \leq 3$ for most cases to meet an aliasing attenuation requirement. Also note that the aliasing depends slightly on R_1. The larger the R_1, the smaller the aliasing. This figure can be used as a guideline to choose the appropriate value for N_1 and R_1.

Fig. 4 shows the droop at the cutoff frequency. Because the *IOSR* is large in a practical system, the droop is very small and can be compensated easily together with the droop introduced by the following CIC filter. For example, suppose a system needs over 70 dB aliasing attenuation. We can choose $N_1 = 2$ for $IOSR \geq 50$ and $N_1 = 3$ for $IOSR \geq 16$. The droop due to the polyphase decomposition is close to 0 dB and -0.05 dB, respectively. It is noted from Table 1 that the polyphase components are simple for the cases of $N_1 \leq 3$.

4. DESIGN ISSUES

In the design of a polyphase CIC filter, apart from the choices of N_1, N_2, R_1 and R_2 (see previous sections and [5]), there are some other issues to be clarified.

An important issue in designing a polyphase filter is to align the polyphase signals of a data converter. This can be accomplished by a commutator which can be constructed with D flip-flops controlled by different clocks. This part is critical in terms of speed. Fast D flip-flops can be implemented with dynamic circuits.

How to implement the polyphase components is another important issue. It is advantageous to get rid of multipliers in implementing these components since they still work at a high speed which is equal to f_S / R_1. For $\Delta\Sigma$ modulators, we can have simpler implementation of polyphase components. Since there are finite combinations for the polyphase components' output, a look-up table ROM can be used to store all the possible results which will be addressed by bandpass $\Delta\Sigma$ modulator's outputs. An even more efficient way to implement polyphase components may be to replace the ROM by combinational logic circuits. Since the output of a single-bit bandpass $\Delta\Sigma$ is either "1" representing +1 or "0" representing -1, we can have simple logic circuits to realize polyphase components.

4.1. Word Length in Polyphase CIC Filters

Here we consider two's complement number representation, such as $a_{0\Delta} a_1 ... a_B$, where the word length is $(B+1)$. If the word length in the input data stream is $(B_{in1}+1)$, the word length at the first CIC filter's output, $(B_{m1}+1)$, is [5]

$$B_{m1} = \lceil N_1 \log_2 R_1 \rceil + B_{in1} \tag{6}$$

where $\lceil x \rceil$ is the smallest integer not less than x. Since the output of the first polyphase CIC filter is the input of the second one's output, the input data words to the second CIC filter are $(B_{m1}+1)$ bits long. As a result, the word length at the second CIC filter's output, $(B_{m2}+1)$, is

$$B_{m2} = \lceil N_1 \log_2 R_2 \rceil + B_{m1} \tag{7}$$

Since $R_2 = R / R_1$, the above expression becomes

$$B_{m2} = \lceil N_2 \log_2 R \rceil + B_{in1} - \left(\lceil N_2 \log_2 R_1 \rceil - \lceil N_1 \log_2 R_1 \rceil \right) \tag{8}$$

Mainly due to the two-stage structure, the final word length for a polyphase CIC filter is shorter than that of Hogenauer's by $\left(\lceil N_2 \log_2 R_1 \rceil - \lceil N_1 \log_2 R_1 \rceil \right)$ bits. If, for instance, $N_1 = 2$, $N_2 = 4$ and $R_1 = 4$, we can save as many as 4 bits in the register word length. It has been proven in [5] that B_{m2} is both the upper and lower bound for each filter stage of the second CIC filter.

4.2. Truncation and Rounding

The register word length in the output of the ith phase signal, where $i = 1,2,...,(R_1 - 1)$, in Fig. 2 is

$$B_i = F_i(1) + B_{in1} \tag{9}$$

Suppose that the output word length required is $B_{out} + 1 \le B_{m2} + 1$. Since the polyphase CIC consists of two cascaded CIC decimation filters, one can retain only B_{out} bits in the output of the first CIC filter without losing accuracy. The number of lower bits discarded at the output of the first CIC filter is

$$\begin{cases} B_{m1} - B_{out} + 1, & B_{m1} > B_{out} \\ 0, & B_{m1} \le B_{out} \end{cases} \tag{10}$$

After truncation or rounding, the word length of the input data to the second CIC filter, B_{in2}, becomes $B_{in2} = MIN(B_{m1}, B_{out})$. For the truncation and rounding of the second CIC filter, see [5].

5. SOME IMPORTANT APPLICATIONS

The polyphase CIC decimation filters proposed above have many applications. These include digital quadrature demodulation, decimation for double sampling and time-interleaved $\Delta\Sigma$ modulators.

5.1. Digital Quadrature Demodulation

The ultimate goal in radio receiver design is to directly digitize the RF signal after the antenna and to digitally realize the whole radio system [1]. Fig. 5 illustrates the digital quadrature demodulation. The input signal is an IF/RF signal and the sampling rate, f_S, is set to be four times the IF center frequency. In doing so, the sine and cosine signals used to demodulate the IF signal become simple sequences of (1, 0, -1, 0, ...) and (0, 1, 0, -1, ...), respectively [9]. The data converter could be either a conventional A/D converter or a bandpass $\Delta\Sigma$ modulator. The very economical CIC decimation filters can be used to downconvert the sampling rate for I/Q channels. A good solution for a bandpass $\Delta\Sigma$ modulator is that the CIC filters downconvert I/Q signals to four times Nyquist rate. Low frequency decimators are used to further downconvert the sampling rate and general purpose DSP processors follow to process the baseband digital signals. The operating frequency in the digital demodulation is f_S which is the data converter's sampling rate, and can substantially be reduced by using the aforementioned polyphase CIC. The frequency reduction for a digital quadrature receiver is shown in Fig. 6, where the downconversion factors of 2 and 4 are achieved in Fig. 6(a) and (b); respectively.

Another advantage of the polyphase CIC filter is that it overcomes the timing misalignment in digital qudrature demodulation. The timing misalignment occurs when a frequency decimation by two is performed in each of the I and Q channels by the removal of the zero-valued samples [8]. The timing misalignment introduces undesired tones in the output's spectrum.

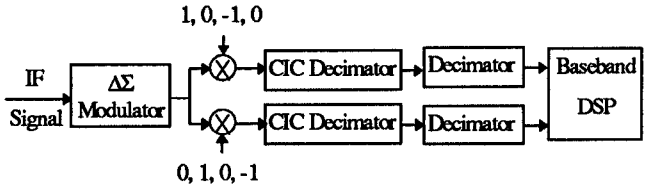

Fig. 5 Quadrature demodulation by digitizing an IF signal

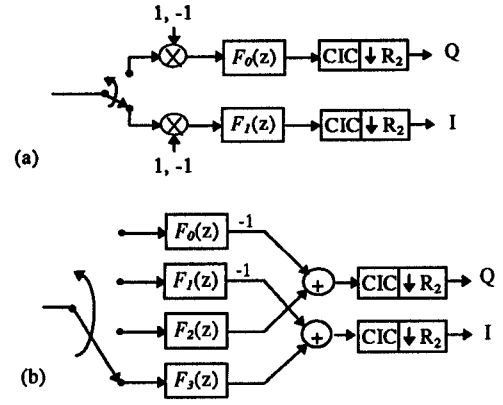

Fig. 6 Polyphase structures in digital quadrature demodulation for the cases of (a) two phases and (b) four phases

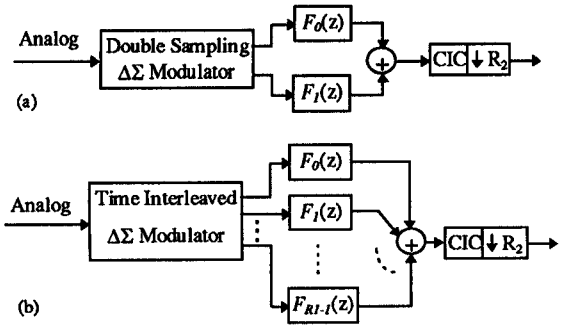

Fig. 7 Applications of the polyphase CIC decimation filter in (a) double sampling and (b) time-interleaved ΔΣ modulation

5.2. Decimation for Double Sampling and Time Interleaved ΔΣ Modulators

A practical double sampling ΔΣ modulator which is insensitive to path gain mismatch was recently proposed in [10]. The technique can increase the effective oversampling ratio by a factor of 2. The output is the interleaved version of two signals. With the polyphase CIC decimation filter, the two signals can be directly processed instead of one interleaved double-speed signal, as shown in Fig. 7(a).

The time-interleaved ΔΣ modulators were presented in [11] and were intended for very high frequency applications. The idea is to interconnect several modulators (say R_1) in a specific way to increase the effective oversampling ratio by a factor of R_1. The outputs of the R_1 modulators are interleaved to form the final output. Again, the polyphase CIC decimation filter is useful for its decimation, shown in Fig. 7(b), where the interleaving of the outputs is not needed for decimation. The advantages of doing this are to reduce the operating frequency in decimation and eliminate the hardware for interleaving.

6. CONCLUSION

In this paper, polyphase CIC decimation filters which need no multiplier have been proposed. The polyphase structures have advantages in high speed operation such as digital RF/IF signal processing and low power consumption. The important applications discussed here include digital quadrature demodulation, decimation for double sampling and time-interleaved ΔΣ modulation.

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