A Novel Self-Calibrating Scheme For Video-Rate 2-Step Flash Analog-to-Digital Converter

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Abstract

This paper presents an on-line trimming technique and an error-code self-trimming algorithm for video rate 2-step flash analog-to-digital converters. The self-calibrating scheme, combining a digital error correction process and the self-trimming algorithm, dynamically maintains the random offsets of the comparators well within ±0.6 LSB and counteracts the interstage gain error, while improving the design of a conventional 2-step A/D converter towards a higher speed, a smaller size and a lower power dissipation. The technique is applicable to subranging ADCs of up to any accuracy. Results from simulation of a 10-bit ADC are given to illustrate the superior efficiency of the scheme and the simplicity of the corresponding **circuitry.**

I. Introduction

The rapidly growing field of digital video requires high-speed, inexpensive, low-power analog-to-digital converters (ADCs). An important direction in the high-speed A/D conversion field is to use CMOS technologies with their inherently high component densities and VLSI capability, while maintaining enough speed for video-rate applications. Two-step ADCs, involving various trade-offs between speed, offsets and power dissipation, are among the best choices [l]. The major problem of high-speed ADCs is that their linearity is limited by the offset errors in the comparators. Current solutions for offset cancellation are to use offset-cancelled comparators [2][3], digital error correction [4], and digital re-mapping techniques [5][6].

In this paper, we propose an on-line technique to trim comparator thresholds and an error-code self-trimming algorithm that attempts to maintain a smooth (nearly-uniform) probability density function (PDF) at the input of a flash ADC by adapting the thresholds. It is well known that the quantization noise of a flash ADC is nearly uniformly-distributed for realistic inputs like video or radio signals. The algorithm is thus suitable for the second-stage of a 2-step ADC. The particular focus of this paper is on the self-trimming algorithm, and its interaction with conventional digital error correction to calibrate both the stages in real time.

II. Self-Trimming Scheme

Consider a stationary stochastic input signal V_{in} with a nearly-uniform PDF ρ and two adjacent thresholds x_i and x_{i+1} in a comparator bank. The i-th output code of an N-bit flash ADC is set to 1 when $x_i \le V_{in} < x_{i+1}$. The probability that digital ***codes*** fall into the i-th interval $[x_i, x_{i+1})$ can be defined as:

$$P(code = i) \approx \rho(x_{i+1} - x_i) \qquad (1)$$

as shown in Fig.1. The operation of this self-trimming scheme updates its thresholds x_i in a similar way to the LMS algorithm used in adaptive filtering [7][8]:

$$\begin{aligned} &\text{if } x_i(t-T) \le V_{in} < x_{i+1}(t-T), \\ &x_i(t) = x_i(t-T) + S;\ x_{i+1}(t) = x_{i+1}(t-T) - S. \end{aligned} \qquad (2)$$

with the end conditions: $x_0 = -\infty$ and $x_{2^N} = +\infty$. In the above equation, S and T are the adaptation step size (mV/step) and time step size, respectively. Digital codes, which control the trimming operations, are from the output of a bit-selection circuit that follows the comparator bank, i.e., only one code is used each time for the adaptation. From (2), we can see that two adjacent comparators (i-th and I+ l-th) are adapted simultaneously when the output code of the i-th comparator is 1: the lower one is trimmed up and the higher trimmed down. A leaky integrator, which tolerates the nonuniformity of the code distribution, accumulates the difference of the up and *down* trims shown in (2). The trimming process reaches equilibrium when the frequencies of the ***up*** and ***down*** trims are equal. A small deviation due to the PDF nonuniformity finally remains as the convergence error with the trimmed thresholds. The structure of this algorithm for the implementation is shown in Fig.2.

This algorithm is effective for improving the differential nonlinearity (DNL) of a flash ADC but not for the integral nonlinearity (INL). Since many re-mapping techniques [5][6] are primarily aimed at improving the INL of an ADC, this algorithm is believed to be a good complement for these mapping techniques.

III. Two-Step ADCs: Application of the Algorithm

A block diagram of a 2-step 10b ADC is shown in Fig.3. The major components of the converter are two A/D subconverters with 5-bit and 5½-bit resolution, a 5-bit D/A converter, a trimming control circuit and a fixed-gain interstage amplifier. The primary error sources present in such a 2-step ADC are gain errors and offset errors in S/H circuits and amplifiers, ADC and DAC nonlinearity and opamp settling error. The residue, which is the input signal to the second stage, is plotted versus the input V_x in Fig.4 when the two A/D subconverters and the DAC are assumed to be ideal. The lower 5-bits of such a l0b ADC are obtained by digitizing the amplified residue. The codes from the residue are nearly uniformly-distributed for inputs with any smooth PDF such as video and radio signals. Some regular signals, such as sine and square waves, will not work well.

Fig.5 shows the residue versus V_x when the first A/D subconverter has some nonlinearity, but the DAC is still ideal. When the conversion range of the second-stage (see Fig.5) is increased, the overflow or underflow of the residue due to positive or negative decision error can be encoded and thus the errors digitally corrected. This process is called *digitul error correction* [1].

The uniformly-distributed PDF of the residue shown in Fig.4 is perfect for trimming the second A/D subconverter. Unfortunately, the nonideal residue shown in Fig.5 may not be suitable for the trimming. However, if we also use the underflow and overflow information to trim the first A/D subconverter while applying digital error correction, we may expect that the resulting nonideal residue, as shown in Fig.5, is at least close to what we need to trim the second stage. The two comparators connected to the ends of the comparator bank of the second A/D subconverter with thresholds $x_{2,0}$ and $x_{2,32}$ ($x_{i,j}$ is the j- th comparator threshold of the i-th A/D subconverter hereafter) can be used to detect the underflow and the overflow for the digital error correction. The codes from these two comparators are also used to trim comparators of the first stage, i.e.,

when $x_{1,j}(t-T) \le V_x < x_{1,j+1}(t-T)$,

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$$\text{if } V_{residue} < x_{2,0},\ x_{1,j(t)} = x_{1,j}(t-T) + S$$
$$\text{if } V_{residue} < x_{2,16},\ x_{1,j+1}(t) = x_{1,j+1}(t-T) - S \quad (3)$$

With the simultaneous trimming of both the A/D subconverters, the effects of interstage-amplifier offset and ADC nonlinearity are reduced or eliminated.

The traditional design of a two-stage ADC requires a high interstage gain to attenuate input-referred nonlinearity from second-stage offsets. When offsets in the second stage are reduced to a minimum level by the trimming, the requirement for a high-gain amplifier can be greatly relaxed and so the bandwidth of the amplifier may be increased accordingly.

The interstage gain error, one of the major error sources, only affects the amplitude of the second-stage input. The error doesn't change the uniformity of the residue's PDF. Thus, the error can be automatically accounted for by the self-trimming second stage. This also has a positive impact on the bandwidth of the amplifier.

A related trimming technique is also applicable to the DAC, because its nonlinearity is also reflected in underflow and overflow of the residue. The nonlinearity of the DAC can be trimmed down by a process similar to that for the first A/D subconverter described by (3).

The combination of this self-trimming algorithm and the digital error correction technique provides an on-line calibrating scheme for the two A/D subconverters, the DAC and the interstage amplifier (Fig.3).

IV. Circuit Implementation

A conceptual diagram of the comparator and its trim circuit, which acts as a leaky switched-C integrator, is shown in Fig.6. The control signals **UP** and **D 0 WN** come from the digital control logic, and the ratio between the capacitances C_0, C_{-1} and C_{+1} determines the adaptation step size S. When the signal UP or DOWN is turned on together with the signal **clock,** charge will be added or removed from capacitor C_0. The resultant voltage on Cc, is used to cancel out the offset of the comparator.

In practice, the ***trim*** circuit is implemented in a current-mode style. The circuit is embedded into the comparator circuit as shown in Fig.7. Current is generated by the ***trim*** circuit (using a PMOS device to convert V_o to a current; see Fig.6) can be added to one side of a differential-pair latched comparator and in so doing compensate for offset errors. A small test chip has been built at AT&T Bell Labs in a 0.9μm CMOS technology, and tested to verify the trimming mechanism [9].

Research on trimming circuits for the DAC is still in progress.

With such a trimming algorithm, the switched-C offset cancellation for the second stage is no longer needed. This should allow a higher input impedance and higher speed (from simpler clocks). Moreover, lower power dissipation and lower switching noise can be expected. This self-trimming algorithm also inherently relaxes the stringent component matching requirement on device sizes, which again leads to a further reduction of power consumption by allowing the use of smaller devices.

V. Simulation Results

The self-calibrating 10b half-flash ADC shown in Fig.3, operated with a single DC supply of 5 volts, was simulated at the architecture level. The critical parts of the ADC were simulated at the transistor level. In the architecture-level simulation, comparator offsets of both the subconverters were modelled using random processes with their means evolving with time in various ways. The maximum offset was set at 100 mV for both A/D subconverters, which is more than twenty times greater than the system LSB (LSB = $5/2^{10}$ volt). The trim steps are also modelled as random processes, as the amount of charge transfer between sampling capacitors in real circuits is contaminated by noise. The means of the trim-step sizes for the two A/D subconverters were 0.1 mV and 0.025 mV, respectively. As high-speed comparators that we have designed (40 MHz in a 1.2μ m CMOS process and 100 MHz in a 0.9μm CMOS process) have a voltage resolution of better than 0.2mV, the trim-step size O.lmV is chosen as that for the first A/D subconverter in this simulation. The choice of O.lmV for the first stage *vs* 0.025mV for the second stage depends upon the ratio between the LSBs of the two A/D subconverters. The step size for the **UP** trim is made equal to be that for the D 0 W N trim. The interstage gain of 8 was chosen as a trade-off between opamp speed and the required attenuation of the input-referred convergence error. The video signal was modelled by a Gaussian process. The simulation was also performed with the digitized real video signal obtained from a 25MHz digitizer, but the results will be reported in [9] due to the page limit here.

The improvement of the system performance was separately measured in terms of differential (DNL) and integral (INL) nonlinearity for the two stages. The DNL and INL are defined as follows:

$$DNL(i) = x_{i+1} - x_i - 1LSB;\ for\ \ i = 0,\ldots,2^N - 3$$
$$DNL(i) = O;\ for\ i = 2^N - 2 \quad (4)$$

$$INL(i) = \sum_{j=1}^{i-1} DNL(j) - best\ linear\ fitting;\ for\ i = 1,\ldots,2^N - 2$$
$$INL(i) = 0;\ for\ i = 0. \quad (5)$$

where i and x_i are respectively the code number and the threshold voltage between codes $i+1$ and i, as defined above. Fig.8(a) shows the improved DNL of the first A/D subconverter after the system converged during about 3×10^6 iterations. One out of every 10,000 output codes is included in the calculation. In the figure, the DNL is described by an interval rather than a specific value due to the nature of the stochastic control. To verify further that most of the calibrated thresholds remain closely around their equilibrium states, we also calculated the probability distributions of DNLs versus LSB. The figure clearly shows that the DNL of the first stage is well within ±0.18 LSB with a calculated probability density (normalized) shown in the RHS figure: the probability that the DNL is greater than ±0.18 LSB is negligible (< 0.01%). In Fig.9(a), the INL of the first A/D subconverter is plotted in a similar way versus ***code.*** The maximum INL is also well within ±0.17 LSB, as expected.

The ***second*** stage contributes more nonlinearity to the entire system, as shown in Figs.8(b) and 9(b). The maximum DNL, with a corresponding probability of about 0.03%, is less than 0.60 LSB. The maximum INL, shown in Fig.9(b), is less than 0.80 LSB.

The DNLs of the comparators at both the two stages are almost symmetric about the code-axis, except those of the first and last comparators as shown in Figure 8(b). This happens because we force underflow or overflow to happen with a certain probability by ratioing the step sizes used to increment and decrement the end thresholds. For example, by using

$$\text{if } V_{residue} < x_{2,0}(t-T),\quad x_{2,0}(t) = x_{2,0}(t-T) - 15S \qquad (6)$$

we keep underflow happening about $\frac{1}{32\times15}(\approx 0.21\%)$ of the time and hold the threshold $x_{2,0}$ at the edge of the PDF. Underflow values are also used, to adjust $x_{2,1}$ to avoid propagating systematic DNL, so that the update rule for $x_{2,1}$ is modified from (2) to:

$$\text{if } V_{residue} < x_{2,1}(t-T),\quad x_{2,1}(t) = x_{2,1}(t-T) - S \qquad (7)$$

Similarly, the case of overflow is handled in a similar way.

Other circuit prototypes that we have designed so far can avoid this DC offset but their complexity for the implementation thus increases accordingly. A comparative study of different circuit prototypes for the self-calibrating ADC will be reported elsewhere.

VI. Conclusions

An on-line trimming technique and a self-trimming algorithm for 2-step 10b ADCs utilizing the concept of a discrete sign-data LMS algorithm has been described. A proposed trimming circuit is used as a leaky SC integrator for the self-trimming algorithm. The interaction between the self-trimming algorithm and conventional digital error correction provides an on-line self-calibrating scheme, which is applicable to subranging ADCs of up to any accuracy. The scheme dynamically maintained the DNLs of both the stages well below 0.18 LSB and 0.60 LSB, respectively, by adaptively trimming the comparators of both the stages of the ADC simultaneously, while automatically counteracting the interstage gain error. The trimming process inherently relaxes the stringent component matching requirement for device sizes, and thus the circuit is expected to work with a smaller size at a lower power dissipation. It also reduces the requirement of a high interstage gain which is used to attenuate the input-referred nonlinearity from the second stage. The nonlinearity of the DAC can also be reduced by trimming.

A detailed mathematical analysis of the self-trimming algorithm and the simulation on real video signal will be reported in [9].

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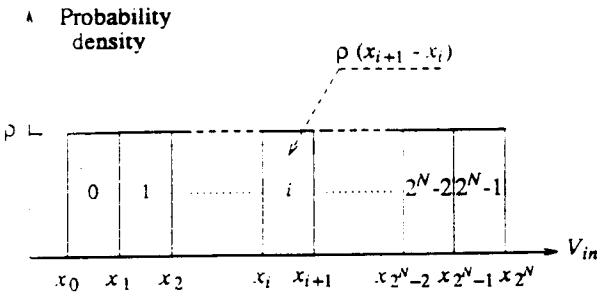

Fig.1 The distribution of input signal V_{in} and the output codes.

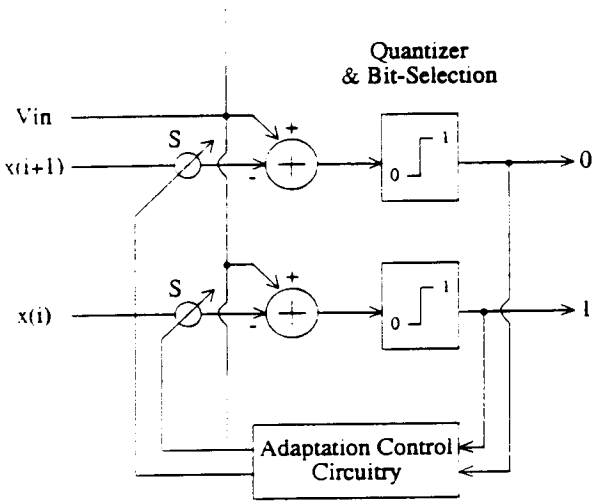

Fig.2 An adaptive trimming scheme for the second stage of a two-step flash A/D converter (when $x(i) < Vin < x(i+1)$).

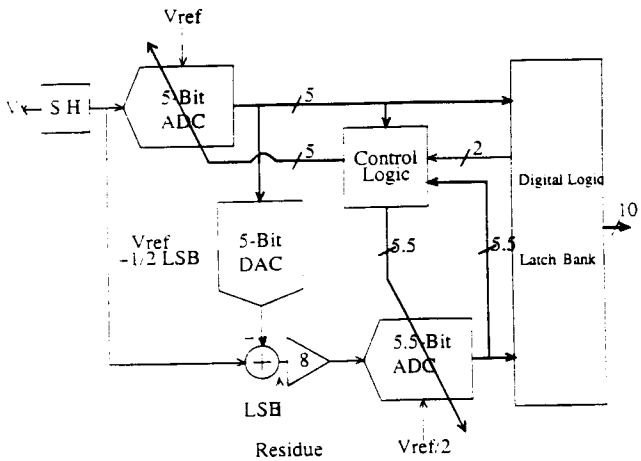

Figure 3. Block diagram of a 10-bit 2-step flash A/D converter with a self-calibrating scheme.

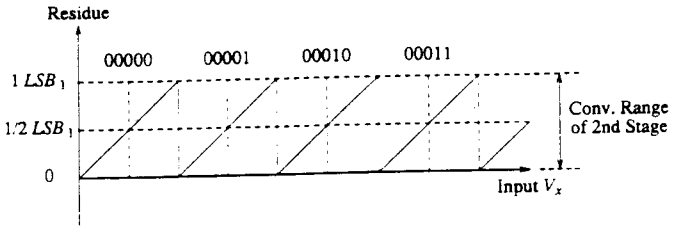

Fig.4 Residue vs. input for ideal A/D subconverter and DAC.
LSB_1 ($=V_{Ref}/2^5$) is the LSB of the first stage.

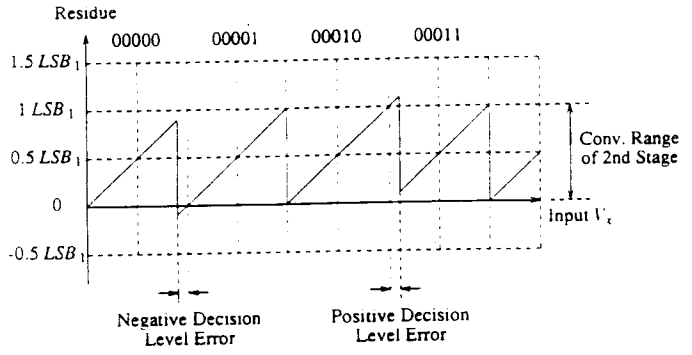

Fig.5 Residue vs. input for nonideal A/D subconverter and ideal DAC.
LSB_1 is defined as in Fig.4.

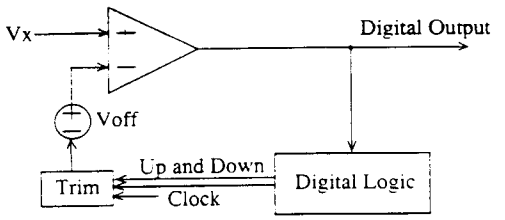

Figure 6(a). Block diagram of a single comparator and its control

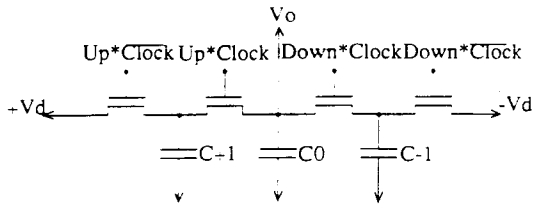

Figure 6(b). The conceptual diagram of the trimming circuit

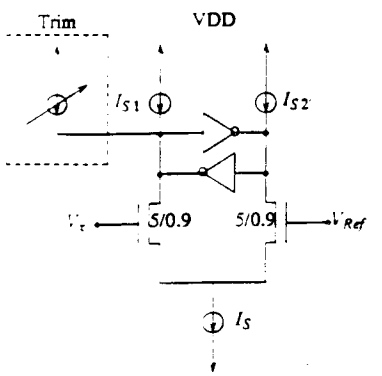

Fig.7 A latched comparator with offset trimming.

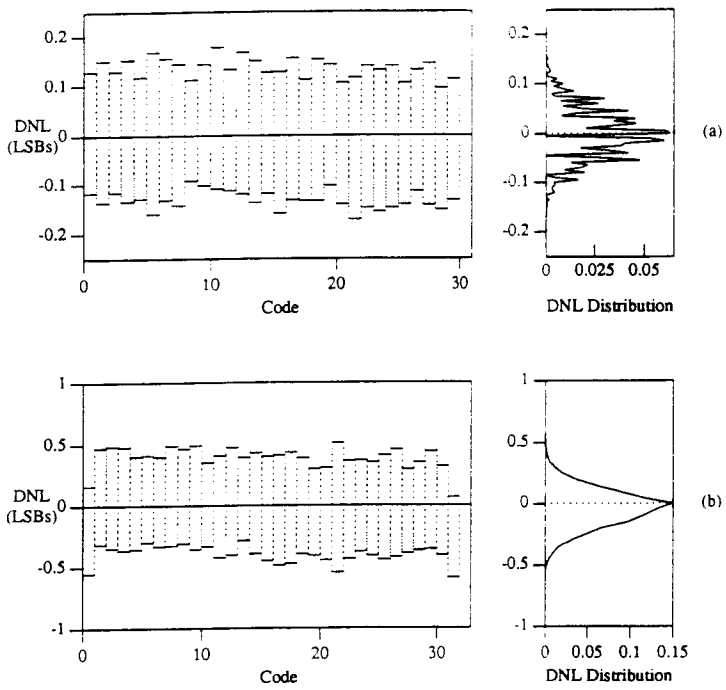

Fig.8 Differential nonlinearity (DNL) and distribution. Note that the DNL varies with time and the maximum initial DNL was ±20 LSB.
(a). Improved DNL of the first subconverter versus output code.
(b). Improved DNL of the second subconverter versus output code.

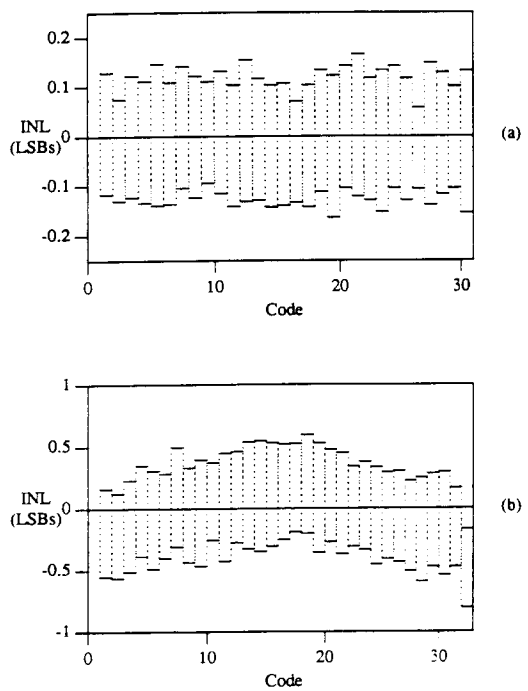

Fig.9 (a). Improved INL of the first subconverter versus output code.
(b). Improved INL of the second subconverter versus output code.