Mixed Analog-Digital Design Considerations in Deep Submicron CMOS Technologies

By

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A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of Doctor of Philosophy.

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The undersigned recommend to the Faculty of Graduate Studies and Research the acceptance of the thesis

"Mixed Analog-Digital Design Considerations in Deep Submicron CMOS Technologies"

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Abstract

Higher speed and higher density are the main thrusts of CMOS technology and are achieved by device miniaturization. In deep submicron geometries, the supply voltage is scaled down to prevent reliability hazards such as oxide breakdown and hot carrier effects and also to reduce energy per operation of digital circuits. Lowering the supply voltage directly reduces the signal swing, which in turn makes the design of high-speed wide dynamic range mixed-signal SC circuits a challenge. It is also desirable to implement SC circuits in a standard digital CMOS process, where double-poly capacitors are not available, because the driving forces behind the CMOS technologies are DRAMs and microprocessors which do not require linear capacitors.

This thesis demonstrates that analog circuit design can track projected digital technology until at least the year 2010. It addresses the design of low-voltage and high-speed SC circuits and also explores the feasibility of using MOSFET capacitors in a linear SC circuit. The thesis describes an experimental 1 V CMOS process implemented as a subset of a 0.5 μm dual n^+/p^+ poly gate process using natural MOSFETs. A 1 V experimental SC sigma-delta modulator is presented—the lowest supply voltage reported so far for SC ΣΔ modulators. Also described is a high-speed fourth-order SC bandpass ΣΔ modulator and a novel fourth-order double-sampled SC bandpass ΣΔ modulator together with their experimental results. Finally, a fourth-order bandpass SC ΣΔ modulator designed in a digital CMOS process using pMOSFET capacitors is described.

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List of Abbreviations

A/D	Analog-to-Digital
ASIC	Application Specific Integrated Circuit
BiCMOS	Bipolar and Complementary Metal Oxide Semiconductor
CE	Constant Electric Field
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CV	Constant Voltage
DC	Direct Current
DR	Dynamic Range
DRAM	Dynamic Random Access Memory
FE	Forward Euler
HD_k	k^{th} harmonic distortion
IF	Intermediate Frequency
LDI	Lossless Discrete Integrator
LDD	Lightly Doped Drain
LT	Low Temperature
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NTF	Noise Transfer Function
nMOSFET	n-channel Metal Oxide Semiconductor Field Effect Transistor
opamp	operational amplifier
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier

pMOSFET	p-channel Metal Oxide Semiconductor Field Effect Transistor
QCV	Quasi-Constant Voltage
SC	Switched-Capacitor
SCE	Short-Channel Effect
SI	Switched-Current
SNR	Signal to Noise Ratio
SNDR	Signal to Noise+Distortion Ratio
STF	Signal Transfer Function
STG	Series Transmission Gate
TG	Transmission Gate
TTL	Transistor-Transistor Logic
UGBW	Unity-gain Bandwidth
VLSI	Very Large Scale Integration
ΣΔ	Sigma-Delta

List of Symbols

$\lvert\ \rvert$	Absolute value
A	opamp DC gain
C_{gb}	Gate-bulk capacitance of MOSFET
C_{gs}	Gate-source capacitance of MOSFET
C_{ox}	Specific gate capacitance of MOSFET
E_c	Conduction band edge
E_g	Silicon bandgap energy
E_v	Valence band edge
e	Quantization noise
f	Frequency in Hz
f_0	Center frequency
f_s	Sampling frequency
g_{ds}	Drain-source conductance
g_m	MOSFET transconductance
$H(s)$	s-domain transfer function
$H(z)$	z-domain transfer function
I_{ds}	Drain current
i_i	Input current
i_o	Output current
i_{off}	MOSFET subthreshold off-current
k	CMOS technology scaling factor
k	Boltzman’s constant

L	MOSFET channel length
$m(\omega)$	Magnitude error frequency response
N_A	Acceptor impurity density
n	Subthreshold slope factor
n_0	Quantization noise in signal band
$\hat{Q}$	Fixed charge density
R_{on}	MOSFET drain-source on-resistance
r_j	MOSFET junction depth
S	Subthreshold swing factor
$S\|_y^x$	Sensitivity of x to variation in y
T	Clock period
T	Temperature
t_D	Delay time
t_{ox}	Gate oxide thickness
V_{BE}	Base-Emitter voltage
V_{DD}	Power supply voltage
V_{FB}	Flat-band voltage
V_{icm}	Input common-mode voltage
V_{ocm}	Output common-mode voltage
V_{on}	MOSFET gate over-drive voltage (on-voltage)
V_t	MOSFET threshold voltage
V_{tn}	nMOSFET threshold voltage
V_{tp}	pMOSFET threshold voltage
$\overline{v_n}$	RMS noise voltage

v_D	Drain voltage
v_{id}	Differential input voltage
v_{in}	Negative input voltage
v_{ip}	Positive input voltage
v_{od}	Differential output voltage
v_{on}	Negative output voltage
v_{op}	Positive output voltage
v_S	Source voltage
W	MOSFET channel width
z^{-1}	Sampled-data representation of delay ($z^{-1} = e^{-j\omega T}$)
α	Velocity saturation index
α_1	First-order voltage coefficient of capacitance
α_2	Second-order voltage coefficient of capacitance
β	MOSFET transconductance parameter ($\beta = \mu C_{ox} W/2L$)
β	Feedback factor
ε_{ox}	Oxide dielectric constant
ε_{si}	Silicon dielectric constant
ϕ_B	Bulk potential
ϕ_F	Fermi potential
ϕ_{ms}	Metal-silicon work function difference
ϕ_n	Clock phase n
ϕ_t	Thermal voltage
γ	Body effect coefficient
μ	Mobility

μ_n	Electron mobility
μ_p	Hole mobility
$\theta(\omega)$	Phase error frequency response
ω_u	Unity-gain bandwidth
ω_0	Cut-off frequency $(-3dB)$

Chapter 1

Introduction

1.1 Motivation

Higher speed and higher density are the main benefits of CMOS VLSI technology and are achieved by shrinking the feature size of the MOSFET devices. In the past, Constant Voltage (CV) scaling has been used for CMOS (down to 0.5 μm) to achieve higher performance and to maintain supply voltage compatibility. However, as MOSFET miniaturization reaches to deep submicron sizes (0.5 μm and below), supply voltage scaling based on Quasi-Constant Voltage (QCV) scaling must be adopted to assure reliability [Kakumu90]. Hot carrier effects and gate oxide breakdown are the two important reliability factors determining how high power supply voltage can be. The Semiconductor Industry Association (SIA) roadmap (Table 1.1) predicts a supply voltage of 0.9 V for semiconductors by the year 2010 [SIA94].

Year	1995	1998	2001	2004	2007	2010
Feature size (μm)	0.35	0.25	0.18	0.13	0.1	0.07
Power supply voltage (V)	3.3	2.5	1.8	1.5	1.2	0.9

Table 1.1: SIA semiconductor technology roadmap

The move toward lower supply voltages is also fueled by low-power battery powered portable devices [Thomas93]. An ideal power supply for a battery powered system is a single-cell (1.2 V - 0.9 V) off-the-shelf battery.

Integrated circuits are moving increasingly into the mixed-signal world where more parts of a system are implemented on a single chip. Performance and density of digital circuits are expected to follow the famous Moore's law—achieving a 2X increase in circuit density and a slower rate of (1.4-1.2)X increase in circuit speed every three years. Energy per operation in digital circuits ($E \sim CV^2$) is also reduced due to supply voltage scaling in deep submicron CMOS. However, lowering the supply voltage directly reduces the signal swing in analog circuits, which in turn makes the design of wide dynamic range mixed-signal circuits a challenge. This raises the following question:

- ***Will mixed-signal supply voltage follow the digital supply voltage down to 1 V?***

In deep submicron CMOS ($L < 0.5$ μm), the charge carriers' velocity will be saturated at the pinch-off point in the channel and as a result the classical quadratic saturation current becomes $I_{dsat} \sim (v_{GS} - V_t)^{\alpha}$, where α = 1.3 to 1.4 instead of 2 [Hu94]. Therefore, 1.4X circuit speed improvement every generation will slow down to about 1.2X, leading to another question:

- ***What are the circuit techniques to maintain a high dynamic range at high speed?***

Analog circuits are usually implemented using Switched-Capacitor (SC) techniques because of their high circuit accuracy. Traditionally, SC circuits are implemented in analog CMOS processes where linear double poly capacitors are available. However, the driving forces behind the CMOS technologies are DRAMs and microprocessors which do not require a double-poly process. The next question is:

- ***Can linear SC circuits be implemented in a standard digital CMOS process?***

These questions form the core of the research conducted in this thesis.

1.2 Thesis Objectives

This thesis is concerned with the three key issues mentioned above, namely: low voltage, high speed, and the implementation of linear SC circuits in a digital CMOS process. Through analysis and some preliminary experimental circuits it will be shown that SC mixed-signal circuits will scale down to 1 V.

Low voltage: To demonstrate the feasibility of 1 V mixed-signal circuits, low-threshold

MOSFET transistors are required. A 1 V CMOS process technology is developed as a subset of a 0.5 μm n^+/p^+ dual poly gate CMOS process. In this process, natural threshold voltage MOSFETs are optimized to have a V_t of about 200 mV. A first-order voice-band SC ΣΔ modulator is implemented in this process and operates at 1 V power supply.

High speed: Low-voltage operation is known to compromise speed unless the technology shrink is in proper relation to the supply voltage. Two new high-speed bandpass ΣΔ modulators are implemented in a 3 V 0.5 μm CMOS process to verify their performance and functionality.

Linear SC design in a digital CMOS process: MOSFET capacitors biased in strong inversion or accumulation regimes can be used to replace linear capacitors. A telescopic opamp with different input and output common mode voltages is shown to be suitable for this purpose. Also described is the design of a fourth-order SC bandpass ΣΔ modulator using pMOSFET transistors, biased in strong inversion, as linear capacitors.

The benchmark circuits are chosen to be ΣΔ modulators for the following two reasons. First, a ΣΔ modulator is a typical mixed-signal circuit with enough complexity to test the technology and to demonstrate the achievable performances. It contains important analog cells such as opamps, comparators and switches as well as some digital gates including inverters, NORs, and a D-type flip-flop. Second, ΣΔ modulators are widely used as precision Analog-to-Digital (A/D) converters and are becoming popular in A/D conversion of narrow-band signals at Intermediate Frequencies (IF) in radio receiver circuitry.

1.3 Contributions

Contributions of this work include:

- Proposed and verified suitability of low-V_t natural MOSFETs for 1 V mixed analog/ digital applications.
- Compared Switched Capacitor (SC) and Switched Current (SI) analog techniques for low-voltage applications.
- Analyzed low-voltage SC circuits using low-V_t MOSFETs.

- Proposed low-leakage series transmission gate and composite switches.
- Demonstrated a technique for exploiting the short-channel effects to obtain low-voltage switches.
- Implemented a high-speed architecture for bandpass ΣΔ modulator.
- Developed a novel double-sampled bandpass ΣΔ modulator.
- Designed a fourth-order SC bandpass ΣΔ modulator in a standard digital CMOS process.

1.4 Thesis Outline

Chapter 1 provides an introduction.

Chapter 2 starts with an examination of CMOS scaling in deep submicron geometries which require supply voltage scaling down to $1\ \mathrm{V}$. Theoretical limits on low-voltage digital and analog CMOS due to circuit topology are discussed and some recent work in this area is reviewed. Oversampling and noise-shaping are then briefly overviewed and a simple mapping of lowpass ΣΔ to bandpass ΣΔ [Jantzi] is described. High-speed SC bandpass ΣΔ modulator techniques are also presented. Next, the Switched-Current (SI) analog circuit technique [Hughes89] is introduced and methods of implementing SC circuits in a digital CMOS process are discussed. Finally, a comparative study of SC and SI for low-voltage applications is presented. It is concluded that the SC technique is preferred in low-voltage circuits from a dynamic range point of view.

In **Chapter 3,** low-voltage SC circuit design using low-V_t MOSFETs is considered. First, two methods of achieving low-V_t MOSFETs in current CMOS processes are proposed. The impact of subthreshold leakage current on the accuracy of the SC circuit is then analyzed. Methods of reducing the subthreshold leakage through analog switches are discussed next and two new switch topologies (series transmission gate and composite switch) addressing this problem are presented. Finally, two experimental circuits, a $2.25\ \mathrm{V}$ ΣΔ modulator using short-channel MOSFETs and a $1\ \mathrm{V}$ ΣΔ modulator using low-V_t natural MOSFET are discussed.

Chapter 4 begins by examining motivations for a high-speed bandpass ΣΔ modulator. A

high-speed fourth-order SC bandpass ΣΔ modulator is discussed, followed by presentation of a double-sampled SC bandpass ΣΔ modulator. Fully differential circuit implementations of both modulators in a 3 V 0.5 μm analog CMOS process are described and measured results are presented.

Chapter 5 describes a SC circuit technique employing MOSFET capacitors biased in strong inversion as linear capacitors. Distortion caused by capacitor non-linearity in a SC amplifier is analyzed. Then, the design of a fourth-order bandpass ΣΔ modulator using a pMOSFET transistor as a linear capacitor is described.

Chapter 6 draws the thesis conclusions and proposes future work.

Appendices which provide some additional information on MOSFET equations used in this thesis and measured characteristics of natural MOSFETs are also included.

Chapter 2

Impacts of CMOS Scaling on Performance of Mixed-Signal Circuits

2.1 Introduction

The scaling of CMOS technology in the deep submicron regime is expected to continue providing faster and denser devices. In section 2.2, CMOS scaling is reviewed along with the fact that, for device reliability, the supply voltage is being scaled down in deep submicron technologies. The power supply voltage of 0.1 μm CMOS technology is expected to be about 1 V [Davari95]. Along with the power supply, the threshold voltage of MOSFETs must be scaled down to achieve high-speed circuits. Limits on supply voltage scaling for mixed-signal circuits are considered in section 2.3; some current research in the area of low-voltage digital and analog circuits is also presented. The impact of reducing the supply voltage on power dissipation of digital and analog circuits is discussed next. In section 2.4, ΣΔ modulators, which are the benchmark circuits in this thesis, are introduced and high-speed bandpass SC ΣΔ modulators reported in the literature are discussed. Most advanced CMOS processes are developed to support memory and digital circuits. Thus, mixed-signal circuits that are realizable in a standard digital CMOS process are desired. Analog SI and SC circuit techniques that allow mixed-signal circuits to be implemented in a digital CMOS process are discussed in section 2.5. Finally, a comparative study of SC and SI sampled-data analog circuit techniques is presented in section 2.6. It will be seen that SC has advantages over SI for low-voltage design.

2.2 CMOS Scaling

The scaling of CMOS technology is achieved by reducing the dimensions of MOSFET transistors by a factor of k ($k > 1$). The original Constant Electric-field (CE) scaling law proposed by Dennard [Dennard74] involved supply voltage scaling as well as scaling all the device dimensions to preserve the same electric-field in the scaled-down device. A constant electric-field in the substrate is obtained by increasing device-well doping concentrations in the smaller devices. The CE scaling scheme improves the device density by k^2, reduces the gate delay by k, and lowers power dissipation by k^2 thus maintaining a constant power density.

Drawbacks of CE scaling are the departure from standard power supply voltage, problems with MOSFET threshold voltage scaling, and degradation in analog signal swing. Therefore, in the past (down to 0.5 μm technology) a Constant Voltage (CV) scaling rule has been used for CMOS to maintain a supply voltage of 5 V and to achieve higher circuit performance; gate delay is reduced by k^2 in a CV scaling. However, in CV scaling the higher electric field causes a reliability hazard due to hot carriers and gate oxide breakdown. A higher electric field in deep submicron devices also brings about carrier velocity saturation, which causes speed improvement to become linearly proportional to k (similar to CE scaling). Another drawback of CV scaling is an increase in power dissipation density which is proportional to k^3.

A compromise between CV and CE scaling schemes is a general scaling theory called Quasi-Constant Voltage (QCV) scaling. In a QCV scaling, power supply voltage is reduced at a slower rate of approximately $\sqrt{k}$. In Table 2.1, various scaling schemes and their effects on MOSFET device characteristics are summarized.

Studies of CE, CV, and QCV scaling for mixed-signal circuits in high-micron [Wong83] and submicron [Sano88] CMOS technologies have shown that QCV scaling is close to an optimum scaling scheme.

2.2.1 CMOS Scaling in the Next Decade

Recently, Davari published a guideline for CMOS scaling in the next decade for digital circuits [Davari95]. A summary of this guideline is produced in Table 2.2. Two different

Parameters	CE	CV	QCV
Lateral dimensions (L)	$1/k$	$1/k$	$1/k$
Gate oxide thickness (t_{ox})	$1/k$	$1/k$	$1/\sqrt{k}$
Doping concentration	k	k^2	$k^{1.5}$
Supply voltage (V)	$1/k$	1	$1/(\sqrt{k})$
Electric field	1	k	1
Current (I)	$1/k$	k	$1/k$
Area (A)	$1/k^2$	$1/k^2$	$1/k^2$
Capacitance ($C=A\varepsilon/t_{ox}$)	$1/k$	$1/k$	$1/k^{1.5}$
Gate delay (VC/I)	$1/k$	$1/k^2$	$1/k$
Power dissipation (VI)	$1/k^2$	k	$1/k^{1.5}$
Power density (VI/A)	1	k^3	$\sqrt{k}$
Energy dissipation (CV^2)	$1/k^3$	$1/k$	$k^{2.5}$

Table 2.1: CMOS scaling schemes

power supply voltages are recommended for each generation of deep submicron technology: one for high-performance (HP) circuits and another one for low-power (LP) circuits.

Year	*1995*	*1998*	*2001*	*2004*
Supply voltage (HP/LP) V	*3.3/2.5*	*2.5/1.5*	*1.5/1.0*	*1.2/1.0*
Channel length (μm)	*0.35*	*0.25*	*0.18*	*0.13*
Oxide thickness (nm)	*9*	*6*	*3.5*	*2.5*

Table 2.2: A guideline for CMOS scaling

This guideline is in agreement with the SIA technology roadmap for semiconductors presented in Chapter 1. By the year 2004, the power supply voltage is predicted to be scaled down to 1.2 V for high-performance circuits and 1 V for low power applications.

Supply voltage scaling in CMOS, undertaken to maintain reliability, causes severe speed performance degradation unless the MOSFET threshold voltage (V_t) is scaled down.

Circuit speed suffers because it is proportional to transconductance (g_m) and for a fully turned- on MOSFET (i.e., $v_{GS} = V_{DD}$) the transconductance is $g_m \sim V_{DD} - V_t$.

2.2.2 V_t Scaling Issues

A MOSFET transistor biased below threshold voltage ($v_{GS} \leq V_t$) operates in the weak inversion mode where drain current is exponentially dependent on the value of $v_{GS} - V_t$ (Appendix A). The subthreshold off-current (for $v_{GS} = 0$) is given by the following simplified equation:

$$i_{off} = I_{D0}\frac{W}{L}10^{-V_t/S}, \qquad (2\text{-}1)$$

where S is the subthreshold swing and is given by

$$S = n\frac{kT}{q}ln(10) \qquad (2\text{-}2)$$

and typically $n \approx 1.4$.

Non-Scalability of Subthreshold Swing

As can be seen from (2-2), subthreshold swing does not scale with technology scaling. Therefore, the main limitation of V_t scaling is due to the non-scalability of S.

At room temperature, S has a typical value of 80 mV/decade for bulk CMOS, and increases to about 100 mV/decade at $85°C$. Reducing the threshold voltage of MOSFETs by 100 mV increases the subthreshold off-current by an order of magnitude. Higher off-current increases the standby power dissipation in digital circuits and limits the accuracy of the analog SC circuits.

Digital circuits: In digital CMOS circuits the total power consumption expression is

$$ɔ = p_{0\to 1}fC_LV_{DD}^2 + i_{off}V_{DD} + i_{sc}V_{DD}, \qquad (2\text{-}3)$$

where $p_{0\to 1}$ is the activity factor, f is the clock frequency, C_L is the load capacitance, V_{DD} is the supply voltage, and i_{sc} is the short circuit current during each input transition when both nMOSFET and pMOSFET are temporarily on.

Lowering the V_t increases the off-current and the second term in the above equation will

rise. However, low-V_t MOSFETs allow operation at a lower V_{DD} without sacrificing speed performance. A reduced V_{DD} decreases the dynamic power consumption, the first term in (2-3).

Several studies [Liu93] [Burr91] have shown that a significant power saving is achieved by operating at very low supply voltages (as low as 200 mV) using low-V_t MOSFETs, while preserving circuit speed.

Analog circuits: Analog switches in SC and SI circuits must exhibit a low on-resistance when closed and very low leakage current when opened. At a low supply voltage, low-V_t MOSFET are suitable as switches due to their low on-resistance. However, low-V_t switches are leaky and limit the precision of the analog circuits. In Chapter 3, the impact of leakage through analog switches is analyzed and some solutions are proposed.

A sharper subthreshold slope (i.e., a lower value of S) is obtained by reducing n, or T, or both in (2-2). The lowest possible value for n is achieved in a CMOS on Silicon-on-Insulator (SOI) process where $n = 1$. The corresponding value of S is 57.5 mV/decade at room temperature. Low-Temperature (LT) CMOS is another method of scaling the subthreshold swing. Operation at liquid nitrogen temperature (77 K) reduces S by a factor of four to about 14.5 mV/decade.

Both SOI and LT-CMOS furnish a better V_t scaling and are promising technologies for very low-voltage deep sub-0.1 μm CMOS processes.

Threshold Voltage Fluctuation

Another limitation of V_t scaling is based on the fundamental variability of the threshold voltage due to process variations. Fluctuation in V_t is mainly due to random dopant and channel length variations. For a normally distributed threshold voltage, the standard deviation due to random dopant concentration variation is

$$\delta V_t = \frac{q}{2C_{ox}}\sqrt{\frac{\pi N_A}{2}}(WL)^{-3/8}(X_D)^{1/4}, \qquad (2\text{-}4)$$

where N_A is the doping density, L and W are the channel length and width of the transistor, and X_D is the depletion width [Keyes75].

Recent studies based on measurements [Mizuno93] and simulations [Nishinohra92] [Wong93] show that V_t variation due to dopant fluctuation is proportional to $1/\sqrt{L}$, in agreement with (2-4), and increases as channel length is reduced. In [Nishinohra92], 2-D and 3-D simulations indicate that $\delta(\Delta V_t)$ is expected to increase from 10 mV, for 1 μm technology, to about 30 mV for a 0.1 μm technology.

Temperature variation also changes the V_t by approximately 1.25 mV/°C [Chen90]. For an industrial temperature range of –50°C to 85°C, the total threshold shift due to temperature alone is about 170 mV.

In low-V_t processes, threshold voltage changes due to process variations and temperature have a big impact on speed and standby power dissipation. For instance speed performance variation (based on quadratic equation formulae given in Appendix A) due to a ±100 mV change in V_t is about ±2.5 % in a 5 V process with V_t = 0.8 V, and rises to ±12 % in a 1 V process with V_t = 0.2 V. Assuming i_{DS} = 1 μA at $v_{GS} = V_t$ and S = 100 mV/decade, the highest off-current in the above example would be 100 fA for the 5 V high-V_t and 10 nA for the 1 V low-V_t processes, respectively. Such a large impact on speed and standby power dissipation due to threshold variation in a low-V_t scenario is intolerable and circuit techniques to address this problem are discussed briefly here.

Multi-threshold voltage: A process with multiple threshold voltage transistors offers circuit design flexibility at the cost of additional threshold adjust masks and an implants. Low-V_t transistors can be used for circuit speed and high-V_t transistors can be used to reduce the leakage current [Shinichiro93].

Back-bias V_t adjusting: Threshold voltage can be held constant by adjusting the substrate voltage. Figure 2.1 shows negative feedback circuitry which generates a substrate voltage to keep V_{tp} equal to a constant V_{ref} [Shoji92] [Bazarjani95d]. The amplifier in this circuit operates with supply voltages of V_P and V_{DD} where $V_P > V_{DD}$ is the positive supply (generated by a charge-pumped circuit) to keep source/drain and bulk junctions reverse biased at all times.

A self-substrate-biasing circuit technique is also reported in [Kobayashi94] to reduce the

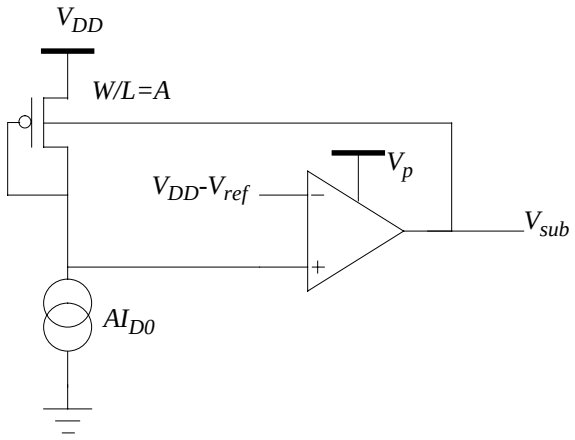


Figure 2.1: A negative feedback V_t adjust circuit

V_t fluctuation. In [Kuroda96], a back-bias feedback circuit that adjusts V_t to 0.1 V in active mode and 0.5 V in the standby mode is discussed. A complete study of V_t adjusting circuits in SOI through back-bias along with the charge pump circuitry is under investigation [Soreefan96].

Summary

Supply and threshold voltages of future deep submicron CMOS technologies are being scaled down. Reducing the threshold voltage increases the off-current due to non-scalability of subthreshold swing, S, limiting the minimum V_t.

2.3 Low-Voltage Mixed-Signal Design

Low-voltage micropower circuit techniques were developed in the late 1960s and early 1970s for electronic wristwatches. These circuits had to operate from a single cell 1.35 V mercury or 1.5 V silver oxide battery. The operating frequencies of these circuits were typically a few kHz and their total power consumption was below 1 μW. Other low-power applications include calculators, hearing aid devices, and pacemakers. In all these systems, the required speed performance of the circuit is low, typically less than 1 MHz.

The technology of choice for low-power applications has been CMOS due to its very low static power dissipation. Techniques to build low threshold voltage MOSFETs with $V_t \sim 0.5 - 0.8$ V were developed in the late 1960s [Nagane69][Leuenberger69] and

methods of adjusting the threshold voltage by doping implants were successfully demonstrated by Swanson [Swanson72].

In this section, limitations to low-voltage digital and analog designs due to circuit topology are discussed and some recent research in the area of low-voltage digital and analog circuits is presented. Finally, the impact of supply voltage scaling on power consumption of digital and analog circuits is considered.

2.3.1 Limits on Digital CMOS Supply Voltage Scaling

A lower limit on the supply voltage of digital circuits is set by the requirement that the voltage gain of a logic gate must be greater than unity. This condition is necessary to obtain regeneration of logic levels at the output of each gate.

In [Swanson72], MOSFET equations in weak inversion are derived and low-voltage operation of a CMOS inverter circuit is analyzed. Voltage gain of the CMOS inverter at mid-rail is found to be: $(V_{DD}/2)(q/(nkT))$. Thus, the minimum required supply voltage for digital CMOS is

$$V_{DD}\big|_{min} > \frac{2nkT}{q}. \qquad (2\text{-}5)$$

This is the theoretical lower bound for the supply voltage of a static CMOS inverter circuit, about $50 - 70$ mV at room temperature. Some experimental circuits that have demonstrated the validity of the above limit include: a 100 mV 11-stage ring oscillator [Swanson74], a 7-stage ring oscillator operating at 75 mV at room temperature and 27 mV at 77 $°K$ [Burr95].

The present supply voltage of 3.3 V for CMOS is a factor of 47 larger than the theoretical limit of 70 mV found in (2-5). Therefore, a large margin for supply voltage reduction exists for CMOS.

In CMOS logic, a certain energy ($CV^2/2$) is stored on the gate capacitance to represent logic 1. This stored energy must be greater than the thermal noise in that capacitor. The mean thermal noise energy in a capacitor is $kT/2$ and in [Stein77], it is shown that for an error rate of 10^{-19} the minimum energy required per operation is $165kT$. Considering this energy requirement and the minimum supply voltage of (2-5), a logic operation

involves only 118 electrons.

At this point, it would be interesting to see what are the minimum required supply voltage and logic swing for a bipolar circuit. A similar study for a Current Mode Logic (CML) gate, Figure 2.2, shows that exceeding unity gain requires the logic swing to be [Gray93]

$$V_{Swing} > \frac{2kT}{q}. \qquad (2\text{-}6)$$

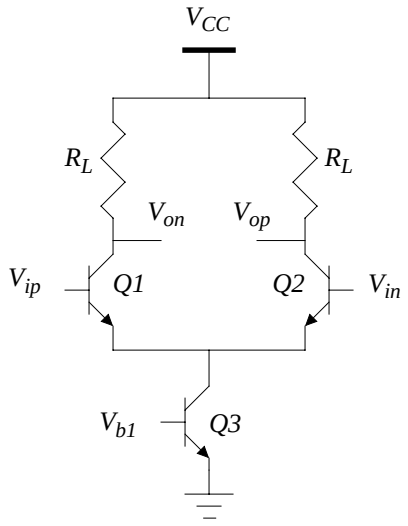


Figure 2.2: A basic CML inverter-buffer gate

At room temperature, the lower bound of logic swing for bipolar circuits is about 50 mV.

The lower limit of the power supply voltage for this CML gate is determined by the voltage required to turn on the input transistors Q1 and Q2 which is

$$V_{CC}\big|_{min} = V_{BE} + V_{Swing} + V_{CE}. \qquad (2\text{-}7)$$

Assuming a turn-on V_{BE} of 0.75 V, a 50 mV logic swing, and a minimum V_{CE} of 0.2 V, the minimum required supply voltage for the CML gate is about 1 V.

Existing 3 V CML gates, with a logic swing of 200 mV, operate close to the limits of 1 V power supply (higher by a factor of 3) and 50 mV logic swing (higher by a factor of 4).

Thus, there is a very narrow margin for supply voltage reduction of bipolar CML gates.

2.3.2 Limits on Analog CMOS Supply Voltage Scaling

This section is an investigation into the lower limit of the supply voltage for an opamp, analog switch, and current mirror—the three basic building blocks commonly used in analog SC and SI circuits.

Operational Transconductance Amplifier

Consider a simple single-stage fully differential opamp circuit, as shown in Figure 2.3. The minimum input common-mode voltage required for the proper operation of this

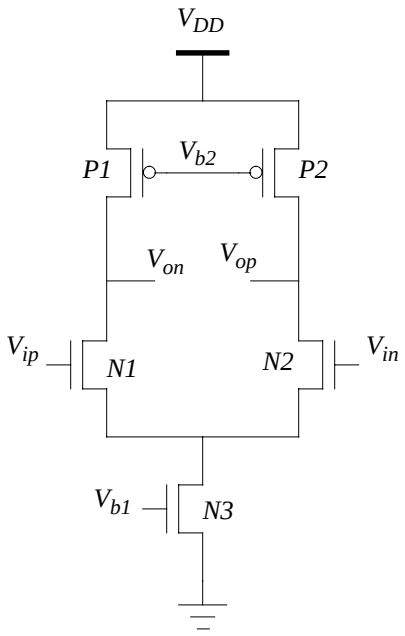


Figure 2.3: A fully differential CMOS Opamp

amplifier is determined by the voltage needed to turn on the input differential pair MOSFETs, transistors N1 and N2, as given by

$$V_{icm}\big|_{min} = V_{tn1} + V_{on1} + v_{DS3}. \qquad (2\text{-}8)$$

Here, V_{icm} is the input common-mode voltage, V_{tn1} is the threshold voltage of the transistor M1, v_{DS3} is the drain-source voltage of the transistor N3, and V_{on1} is the gate to source overdrive voltage of the transistor N1 which is defined as

$$V_{on} = v_{GS} - V_t. \qquad (2\text{-}9)$$

The minimum v_{DS3} required to keep the transistor M3 in saturation is

$$v_{DS3}\Big|_{min} = V_{on3} = v_{GS3} - V_{t3}\,. \qquad (2\text{-}10)$$

If equal threshold voltage V_t and overdrive voltage V_{on} is assumed for all the transistors and also assumed that $V_{DD} > V_{icm}$ (i.e., charge-pump techniques are not used), from equation (2-8) the lower bound on the supply voltage of the opamp is

$$V_{DD}\Big|_{min} = V_t + 2V_{on}. \qquad (2\text{-}11)$$

The minimum required drain-source saturation voltage depends on the MOSFET mode of operation. If the device is in weak inversion, the minimum saturation voltage required is about $(4-6)kT/q$ [Vittoz94], which is $100-150$ mV at room temperature. However, the minimum drain-source saturation voltage of MOSFETs operating in strong inversion is about 200 mV.

In a typical 0.5 μm CMOS process, with a threshold voltage of 0.6 V, and assuming an overdrive voltage of 0.2 V, the minimum supply voltage of this opamp is 1 V. In this calculation, we ignored V_t variations due to process fluctuation, temperature changes and back-bias voltage as well as constraints on input and output common-mode levels.

In a low-V_t process, the minimum supply voltage of the opamp (Figure 2.3) may be determined by the drain-source saturation voltage (or V_{on}) and the required output voltage swing $V_{out(swing)}$. Assuming equal gate to source overdrive voltage for all the transistors, the minimum supply voltage is

$$V_{DD}\Big|_{min} = 3V_{on} + V_{out(swing)}\,. \qquad (2\text{-}12)$$

For $V_{on} = 0.2$ V and an output voltage swing of 0.4 V, the minimum power supply voltage is 1 V.

Analog Switch

An analog switch must have a full rail-to-rail signal handling capability with a low on-resistance. An nMOSFET transistor used as a switch operates in triode mode with on-resistance of approximately

$$R_{on} = \frac{1}{\mu C_{ox}\frac{W}{L}(v_{GS} - V_{tn})} . \qquad (2\text{-}13)$$

A parallel nMOSFET and pMOSFET switch (transmission gate) has a rail-to-rail signal swing capability if the supply voltage is

$$V_{DD} = V_{tn,e} + V_{tp,e} + 2V_{on}. \qquad (2\text{-}14)$$

The effective threshold voltages, $V_{tn,e}$, and $V_{tp,e}$ are given by

$$V_{te} = V_{t0}(Max) + \Delta V_t(T) + \Delta V_t(v_{SB}) . \qquad (2\text{-}15)$$

$V_t(Max)$ is the 3σ upper value of threshold voltage due to process variations, $\Delta V_t(T)$ and $\Delta V_t(v_{SB})$ are the threshold voltage changes due to temperature, and the back bias respectively and are given by

$$\Delta V_t(T) = a(25 - T) \qquad (2\text{-}16)$$

$$\Delta V_t(v_{SB}) = \gamma(\sqrt{2\Phi_B + v_{SB}} - \sqrt{2\Phi_B}) . \qquad (2\text{-}17)$$

Here, T is temperature in degrees Celsius, and "*a*" is the slope of threshold voltage as a function of temperature, which is about $1-2$ mV$/°C$. Other parameters are the body effect coefficient $\gamma \approx 0.5$, the bulk potential Φ_B, and the source to bulk voltage v_{SB}.

The on-conductance of a transmission gate switch as a function of signal level is shown in Figure 2.4 for three different values of power supply voltages [Vittoz93]. In this figure the

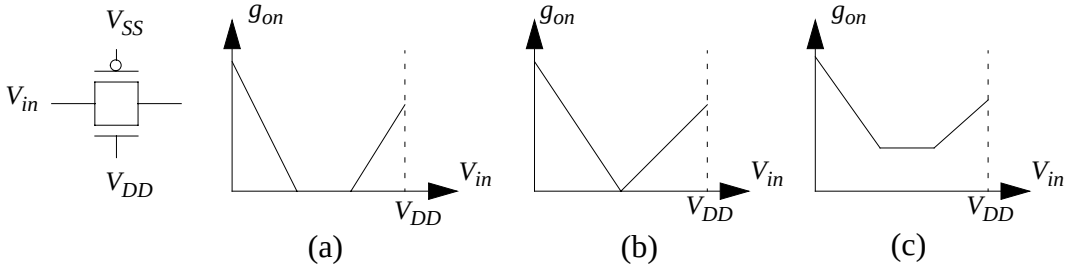


Figure 2.4: Complementary transmission gate switch on-conductance for (a) $V_{DD}<2V_t$, (b) $V_{DD}=2V_t$, and (c) $V_{DD}>2V_t$

threshold voltages of nMOSFET and pMOSFET are assumed to be equal to V_t.

In a 0.5 μm process with effective threshold voltages of 0.8 V, a supply voltage of 2 V is required to turn the transmission gate on with a minimum overdrive of 0.2 V at mid-rail.

Current mirror

A current mirror circuit is a current gain cell that provides a weighted output copy of an input current. This circuit forms the foundation of SI signal processing and is also widely used to provide bias currents in such blocks as opamps and comparators. A simple current mirror circuit is shown in Figure 2.5. The voltage V_B generates a current I_B in the transistor P which is fed to the diode-connected transistor $N1$. Since transistors $N2$ and $N1$ have the same gate and source potential, their drain-source currents are related by

$$\frac{I_2}{I_1} = \frac{(W/L)_{N2}}{(W/L)_{N1}}. \qquad (2\text{-}18)$$

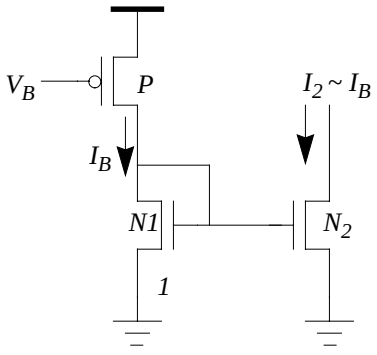


Figure 2.5: A simple current mirror cell

If $N1$ and $N2$ are identical transistors, I_2 will mirror I_B. For accurate operation, all the transistors in the circuit must be in the saturation regime. Transistor $N1$ is diode connected and when it is turned on it will be in saturation with a gate (or drain) to source voltage of $V_t + V_{on}$. Assuming the same overdrive voltage (V_{on}) for all the MOSFETs, transistor P requires a drain to source voltage of at least V_{on} to be in saturation. Thus, the minimum required supply voltage for proper operation of the simple current mirror is

$$V_{DD} > V_t + 2V_{on}, \qquad (2\text{-}19)$$

which is identical to the minimum supply voltage expression obtained for a simple opamp (2-11). Comparison of (2-11), (2-19) and (2-14) shows that switches are the bottleneck for low-voltage SC and SI operation.

2.3.3 Previous Work on Low-Voltage Digital Circuits

A low-voltage digital design using standard CMOS technology, by A. Chandrakasan at Berkeley University, is described first. Then, a theoretical analysis by Dake Liu at Linkoping University, showing power savings achieved by supply voltage and threshold voltage down-scaling, is discussed. Finally, an experimental encoder-decoder system operating at 200 mV, by Jim Burr at Stanford University, is presented.

Berkeley

Power optimization at different levels of technology, circuit style, architecture, and supply voltage scaling is considered in [Chandrakasan92]. The most efficient logic family was found to be CPL (Complementary Pass-transistor Logic) if low threshold nMOSFETs are available. Logic gates must be designed for the lowest acceptable speed to save unnecessary energy loss.

In a 2 μm CMOS technology, a power supply of 1.5 V is found to be the optimum for a large variety of cases. At such a low voltage ($V_{DD} = 2V_t$), circuit speed may become unacceptably low for some applications. In such cases, techniques such as parallel architecture and pipelining can be used to obtain lower latency and higher throughput rates.

Linkoping

An extensive study of the impacts of supply voltage and threshold voltage scaling is reported in [Liu93]. Reducing the supply voltage decreases the power consumption in CMOS logic ($P \propto fCV^2$). However, speed performance $T \propto (V_{DD})/(V_{DD} - V_t)^2$ is degraded unless the threshold voltage is scaled down.

In a 0.25 μm CMOS technology it is shown that a factor of 40 reduction in power dissipation is possible, without any speed loss, by reducing the supply voltage from 3 V to 0.48 V and properly optimizing the MOSFETs threshold voltages from 0.7 V to $V_{tn} = 0.1$ V and $V_{tp} = -0.01$ V.

Stanford

Low-power research at Stanford University [Burr91] focuses on the use of near zero threshold voltage ($\sim$100 mV) MOSFETs and selecting a power supply voltage of $V_{DD} = 3V_t$. The threshold voltage is fine-tuned by applying a back-bias potential.

Low threshold voltage devices allow reduced power supply voltage, which in turn decreases AC power dissipation quadratically. However, DC power consumption, due to the subthreshold leakage, increases exponentially. The minimum total power dissipation is obtained at a supply voltage where the AC component of the power dissipation and the DC power dissipation are equal. In a 2 μm CMOS technology, 200 mV is shown to be the optimum supply voltage for digital circuits with a logic depth of 10 and an activity ratio of 0.1. An experimental CMOS Encoder/Decoder circuit is demonstrated in [Burr94] to operate at 200 mV supply voltage.

2.3.4 Previous Work on Low-Voltage Analog Circuits

Work on low-voltage analog circuits started in bipolar technology in the 1970s. Some reported 1V circuits in bipolar technology include: a bandgap voltage reference [Vittoz77], operational amplifiers [Widlar78] [Huijsing85], an active lowpass filter [Tanimoto91], and an analog current mode multiplier cell [Chan95].

Low-voltage analog circuits in CMOS (the focus of this work) started in the late 1970s [Vittoz77] and early 1980s [Vittoz80] [Krummen82]. Low-voltage analog circuits are implemented using Switched-Capacitor (SC), active-RC, and Switched-Current (SI) techniques. This section starts by describing a 1 V ΣΔ A/D converter using an active-RC technique. A 1.2 V ΣΔ converter implemented with the SI technique is then discussed. Finally, three papers dealing with low-voltage SC filters are presented.

2.3.4.1 Low-Voltage Active-RC Circuits

A 1 V second-order ΣΔ modulator, implemented in a 0.5 μm multi-threshold voltage CMOS technology, is reported in [Matsuya94]. Integrators in the ΣΔ modulator are implemented using an active-RC technique, as shown in Figure 2.6. For an oversampling ratio of 16, this modulator has a SNDR of 51 dB and a dynamic range of 58 dB. The modulator operates at a clock frequency of 6.14 MHz (signal bandwidth of 192 kHz)

and consumes 1.56 mW at a 1 V power supply voltage.

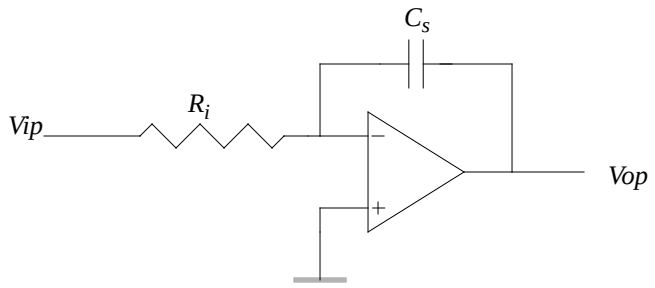


Figure 2.6: An active-RC integrator

Since subthreshold leakage current through low-V_t analog switches was the main source of concern in this design, SC implementation was ruled out. In Chapter 3 of this thesis, the impact of leakage current through analog switches on the accuracy of SC circuits are discussed and methods of reducing the subthreshold leakage are also presented.

A drawback of integrated active-RC circuits is inaccuracy in the RC time constant, because monolithic resistors and capacitors have a tolerance of more than ±15 % and do not track each other. For lowpass ΣΔ modulators, variations in the RC time constant causes a gain variation and is not critical.

2.3.4.2 Low-Voltage Switched-Current Circuits

Recently [Tan95], a low-voltage second-order SI ΣΔ modulator was reported which operates at 1.2 V. The circuit, however, is not a true 1.2 V part because the switches operate from a higher external supply voltage.

The circuit is implemented in a 0.8 μm digital CMOS process using a fully differential SI memory cell with a common-mode feed forward circuit. This modulator is clocked at 1 MHz and consumes 0.78 mW. The measured SNDR and SNR for an oversampling ratio of 64 are 55 dB and 51 dB respectively. Ideally, this modulator should achieve a SNDR of more than 80 dB. The low performance of this SI circuit is attributed (by the authors of the original paper) to circuit noise generated by the first current copier cell.

A review of SI technique is provided in section 2.5. In section 2.6 it will be shown that SC has some advantages over SI for low-voltage applications.

2.3.4.3 Low-Voltage Switched-Capacitor Circuits

In CMOS, SC is the dominant technique for implementing analog circuits due to its high circuit accuracy and low distortion even at low supply voltages [Castello91]. For low-voltage applications, the most critical component in a SC circuit (and a SI circuit) is the transmission gate switch, which requires a gate voltage of at least $2V_t$ for proper full swing signal handling. In SC circuits, few switches usually require rail-to-rail signal swing. For instance, in the non-inverting SC integrator of Figure 2.7 only the input switch (S1) needs to be implemented with a transmission gate, an nMOSFET and an pMOSFET in parallel. All the other switches are connected to analog ground $V_{ag} \approx V_{DD}/2$ and thus can simply be nMOSFET transistors.

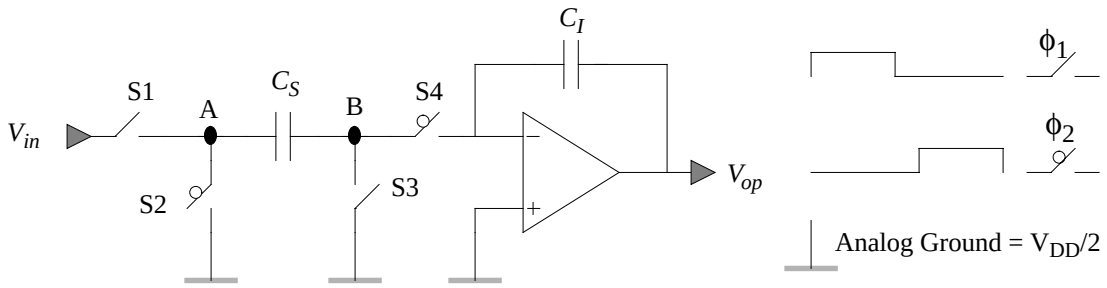


Figure 2.7: A non-inverting SC integrator and its associated 2-phase non-overlapping clock

In general, to achieve full signal transmission through a MOSFET switch with acceptable on-resistance, either the gate voltage must be increased (e.g., clock voltage multiplication) or the threshold voltage of MOSFETs must be reduced. A third solution would be to eliminate the need for switch $S1$. In the following section, the above methods of low-voltage SC design are described.

(I) Clock Voltage Multiplication

If the supply voltage is less than $2V_t$, the MOSFET switches will not be able to conduct when biased at the mid-rail. Clock voltage boosting is an effective way of increasing the conductance of the MOSFET switches. This is the most commonly used technique in low-voltage SC circuits [Krummen83] [Callias89] [Castello91] [Wayne92] [Grilo96] [Au96].

A biquadratic SC lowpass filter operating at 1.5 V is reported in [Castello91] for

telephony applications. This filter uses a fully differential architecture and is fabricated in a 0.8 μm BiCMOS technology. The clock frequency is 447 kHz and the measured THD is −70 dB for a 1.5 Vpp signal.

This technique requires extra circuitry for voltage multiplication, may need an off-chip capacitor, and is noisy. Another drawback of voltage boosting is that in deep submicron modern processes, the higher electric field of clock voltage is a reliability hazard and is not acceptable.

(II) Low-V_t MOSFETs

Reducing the threshold voltage of MOSFETs will reduce the on-resistance of the switches. In [Adachi90], a lower threshold voltage nMOSFET ($V_t = 0.2$ V) is fabricated by adding an extra mask for threshold adjust implant to a double-poly 2 μm CMOS process. A 7th- order Chebyshev SC lowpass telephony filter, implemented in this process, operates at 1.4 V and consumes 0.49 mW. This filter is clocked at 111 kHz and has a cutoff frequency of 3 kHz. The in-band noise for an input signal with a 1 Vpp signal is measured to be −67 dBm. This performance is comparable to the SC filters operating at 5 V.

This method may require process modification. However, in multi-threshold processes [Sun92] [Mutoh93], low-V_t MOSFETs are available at no extra cost. A low-cost method of fabricating low-V_t devices in a dual poly gate process is also discussed in Chapter 3. An advantage of this approach (i.e., the low-V_t MOSFET switch) is compatibility with the future of CMOS technology and low-power digital design [Liu93][Burr94] because power supply scaling is forcing V_t down-scaling.

(III) Switched-Opamp Circuits

In a SC circuit most switches are connected to analog (or virtual) ground. By selecting an analog ground which is very close to V_{SS}, nMOSFETs that conduct well can be used as switches. The input switch that requires full signal swing, switch $S1$ in Figure 2.7, can be replaced with a switched-opamp as shown in Figure 2.8.

A second-order lowpass filter implemented using a switched-opamp is described in [Crols94] and operates at 1.5 V while consuming 110 μW. This biquadratic filter is

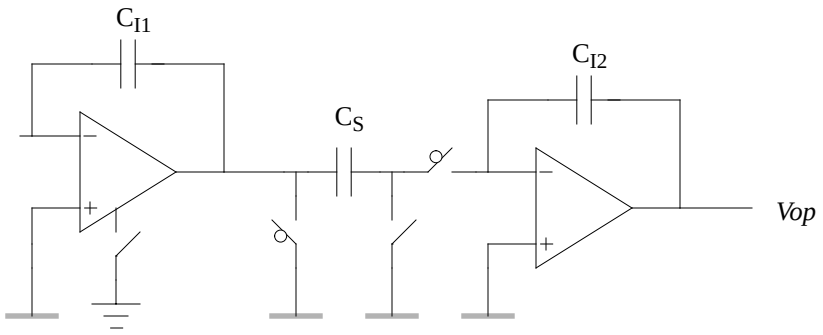


Figure 2.8: A switched-opamp SC integrator

clocked at 115 kHz and has a cutoff frequency of 1.5 kHz. For an output swing of 0.55 Vpp, the total harmonic distortion is measured to be −64 dB. The dynamic range of this filter is about 69 dB.

In a SC circuit, the very first input switch is not driven by an integrator and therefore can not be replaced with a switched-opamp. One solution is to implement the first stage of the circuit using an active-RC technique. This causes a gain error, which may be acceptable, while all the loop time constants are determined by SC topologies.

2.3.5 Impact of Voltage Scaling on Power Dissipation of Mixed-Signal Circuits

Power dissipation in a circuit must be studied in relation to other performance parameters of the circuit. For instance, in digital circuits there is a trade-off between power dissipation and speed of the circuit. In general, one is interested in reducing power consumption while not sacrificing speed. This means reducing the energy consumption of the circuit. In analog circuits, power minimization must be considered along with the speed and dynamic range of the circuit. In this section, the effects of supply voltage scaling on energy dissipation of digital circuits and power dissipation of analog circuits (for a fixed speed and dynamic range) are investigated.

Power Dissipation in Digital CMOS

In general, power dissipation is caused by two types of current: a dynamic current and a static current. A CMOS inverter, Figure 2.9, is used to illustrate various components of the power dissipation in static CMOS logic.

The static power dissipation is caused by MOSFET subthreshold leakage and leakage

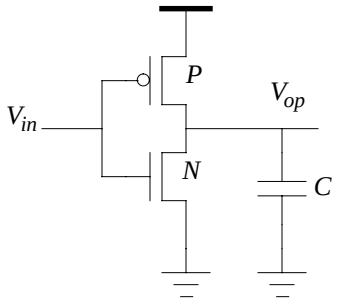


Figure 2.9: CMOS inverter

currents through reverse-biased junctions (I_{leak}). When switching, charging and discharging of the load capacitor (C) is the main source of power dissipation which is quadratically proportional to the supply voltage. During each input transition, there is also a short circuit (crowbar) current (I_{sc}) flowing directly from the power supply to ground when both nMOSFET and pMOSFET are temporarily on ($V_{tn} < V_{in} < V_{DD} - V_{tp}$). The total power consumption is

$$P = I_{leak}V_{DD} + fCV_{DD}^2 + I_{sc}V_{DD}. \qquad (2\text{-}20)$$

Dynamic power dissipation fCV_{DD}^2 is usually the dominant term in (2-20) [Burr91]. Energy dissipation is a measure of the power-delay product, which is

$$E = CV_{DD}^2. \qquad (2\text{-}21)$$

Supply voltage scaling reduces the energy dissipation in digital CMOS circuits quadratically.

Power Dissipation in Analog SC Circuits

The SC integrator shown in Figure 2.7 is considered for the study of power dissipation in analog SC circuits.

Just as for digital circuits, there are two types of power dissipation: dynamic and static. Leakage currents, DC bias currents in bias circuitry, and opamp bias currents for class A operation will all contribute to static power dissipation.

$$P_{static} = I_{leak}V_{DD} + (I_{bias} + I_A)V_{DD} \qquad (2\text{-}22)$$

Dynamic power is dissipated by the clock generator, charging and discharging MOSFET switches, as well as by amplifiers charging load capacitors (C_S and C_I). The dynamic power dissipated in clock drivers due to the gate capacitance of MOSFET switches is

$$P_{sw} = f_{clock} C_{sw} V_{DD}^2. \quad (2\text{-}23)$$

The average power dissipated in driving the load capacitors is given by the following equation [Castello85]:

$$P_C = \frac{2}{\pi} V_i V_{DD} C_s f_{clock} \quad (2\text{-}24)$$

Here, V_i is the peak amplitude of a sinusoidal signal and f_{clock} is the clock frequency. In analog circuits an important figure of merit is dynamic range (DR), which is a measure of circuit accuracy and is given by

$$DR = \frac{Signal(rms)}{noise} = \frac{V_{i,rms}}{\sqrt{kT/C_s}}. \quad (2\text{-}25)$$

$V_{i,rms}$ is the RMS value of the input sinusoidal signal, $k = 1.38 \times 10^{-23}$(J/K) is the Boltzman constant, and T is the temperature in degrees Kelvin. If we assume that the input is a sinusoidal signal and can swing between supply rails, the RMS value of the input is

$$V_{i,rms} = \frac{V_{DD}}{2\sqrt{2}}. \quad (2\text{-}26)$$

Equations (2-24), (2-25), and (2-26) can be combined to describe power dissipation in the sampling capacitor as a function of dynamic range and clock frequency. The resulting equation is

$$P_C = \frac{DR^2}{2\pi}(kT) f_{clock}. \quad (2\text{-}27)$$

This equation shows that for a given dynamic range the power dissipated in driving the load capacitor is independent of the power supply voltage.

Thus, in the limit, when DC power dissipation and power dissipated due to the switches are negligible compared to AC power dissipation in driving the load capacitors, reducing the power supply will not change the power dissipation in the analog circuitry.

In the above analysis, limitation on the unity gain bandwidth (ω_u) was not included. A more realistic approach is to relate power dissipation to DR and ω_u. Power dissipation in driving the load capacitor is

$$P = V_{DD} I. \quad (2\text{-}28)$$

The speed of a SC circuit is determined by the unity gain bandwidth of the opamp which is

$$\omega_u = \frac{g_m}{C}. \quad (2\text{-}29)$$

Here, g_m is the transconductance of the opamp which has the following relation with the quiescent current:

$$I = g_m \frac{V_{on}}{2}. \quad (2\text{-}30)$$

Combining equations (2-25), (2-26), (2-28), (2-29) and (2-30), the power dissipation can be expressed in terms of dynamic range, speed, and supply voltage as

$$P \propto DR^2 kT \omega_u \left(\frac{V_{on}}{V_{DD}} \right). \quad (2\text{-}31)$$

Thus, reducing the supply voltage, if accompanied by an increase in load capacitance to compensate for dynamic range loss, will increase the total power dissipation in analog circuits. Scaling V_{on} with the supply voltage would give constant power dissipation but would require process scaling to correct for the reduced transistor f_t, which is inversely proportional to channel length squared, $f_t \propto V_{on} / L^2$.

If supply voltage scaling does not require increasing the load capacitor (and consequently increasing the quiescent current), power dissipation will be reduced linearly with supply voltage down-scaling. This happens when the value of the capacitor is determined by other considerations such as stability or matching, and is higher than the required value due to

kT/C noise.

Summary

Limits to low-voltage digital CMOS circuits indicate that there is a large margin for supply voltage down scaling. A review of the literature in the area of low-voltage circuits suggests that digital circuits using low-V_t MOSFETs achieve a great saving in power dissipation. In analog SC circuits, if the process is fixed lowering the supply voltage will increase the power dissipation in driving the load capacitance. On the other hand, technology scaling allows V_{on} to be scaled down along with the power supply without sacrificing device f_t. In this case, power dissipation for a given dynamic range and unity gain bandwidth will remain unchanged.

2.4 Oversampled Sigma-Delta Modulator Overview

Oversampled ΣΔ modulation is a noise shaping technique that converts an analog input signal into a simple digital code (typically 1-bit) at a sampling frequency which is much higher than the Nyquist rate. A block diagram of a general n-bit ΣΔ modulator comprising a loop filter, an n-bit A/D, and an n-bit D/A in a negative feedback loop is shown in Figure 2.10.

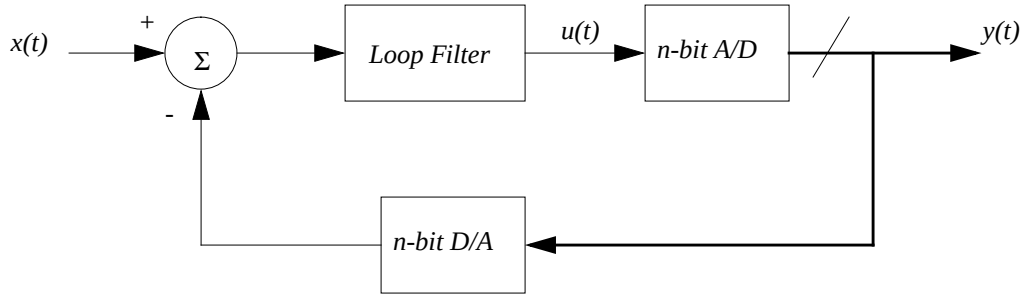


Figure 2.10: A block diagram of a ΣΔ modulator

The loop filter shapes the quantization noise out of the band of interest. If a lowpass filter is placed in the loop, the quantization noise will be highpass filtered and if a bandpass filter is chosen as loop filter, the quantization noise will be band-reject filtered. In a sigma-delta A/D converter, the out of band quantization noise is removed by a digital filter that also performs decimation.

ΣΔ is becoming the method of choice for high-precision low- or medium-speed A/D converters. This is because compared to other techniques, such as flash and pipelined A/D, the analog circuitry in a ΣΔ modulator is simple and relatively insensitive to circuit imperfection and component mismatch. Also, due to the oversampling, the antialiasing filter at the input of a ΣΔ A/D converter has relaxed requirements compared to that of a Nyquist rate A/D converter. However, ΣΔ modulators require a large digital signal processing unit for the decimation filter. Both simplicity of analog circuits and extensive use of digital circuits in ΣΔ modulators are highly compatible with scaled-down CMOS technologies.

In Figure 2.10, if the transfer function of the loop filter is denoted as $H(z)$ and the n-bit A/D (multilevel quantizer) is modeled as an additive noise $Q(z)$, the equivalent linear feedback system of Figure 2.11 is obtained.

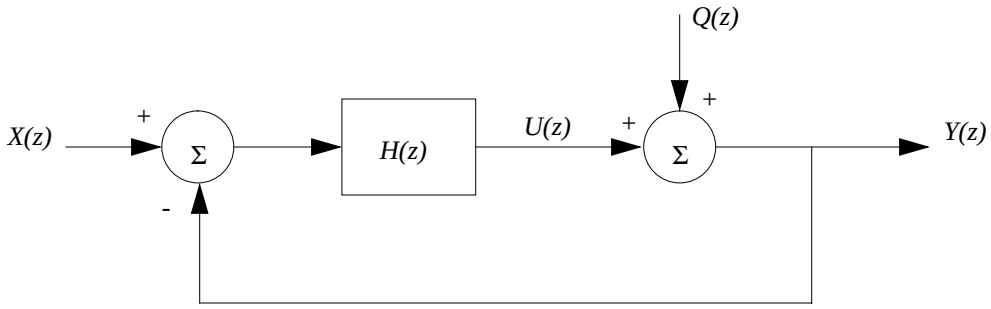


Figure 2.11: Equivalent linear system of Figure 2.10

The expression for the output z-transform in terms of the signal transfer function $F_X(z)$ and noise transfer function $F_Q(z)$ is

$$Y(z) = F_X(z)X(z) + F_Q(z)Q(z) \quad . \qquad (2\text{-}32)$$

The signal transfer function and the noise transfer function are respectively

$$F_X(z) = \frac{H(z)}{1 + H(z)} \qquad (2\text{-}33)$$

$$F_Q(z) = \frac{1}{1 + H(z)} \quad . \qquad (2\text{-}34)$$

2.4.1 Lowpass Sigma-Delta Modulators

A simple first-order ΣΔ modulator is obtained by letting the loop filter be a discrete-time integrator and also allowing the quantizer to have only two levels of $\pm\Delta/2$. The *z*-domain transfer function of a unity delay integrator is

$$H(z) = \frac{z^{-1}}{1-z^{-1}}. \qquad (2\text{-}35)$$

Substituting the above $H(z)$ into equations (2-33) and (2-34) will give the corresponding signal transfer function and noise transfer function, as follows:

$$F_X(z) = z^{-1} \qquad (2\text{-}36)$$

$$F_Q(z) = 1-z^{-1}. \qquad (2\text{-}37)$$

The signal transfer function is simply a unit delay and the noise transfer function is a first-order differentiator which behaves like a highpass filter. Since F_Q has a zero at DC, the quantization noise is reduced at low frequencies and is pushed to high frequencies.

If the quantization error is assumed to be white noise with a mean square value of $\Delta^2/12$, the quantization noise in the signal band $) < f < f_E$ is approximately [Candy92]

$$n_0^2 = \frac{\Delta^2}{12}\frac{\pi^2}{3}\left(\frac{1}{OSR}\right)^3, \qquad (2\text{-}38)$$

where OSR is the oversampling ratio defined as the ratio of the sampling frequency f_s to the Nyquist rate of the signal $2f_B$.

Increasing the OSR by a factor of 2 reduces the quantization noise, in the first-order ΣΔ modulator, by 9 dB which adds 1.5 bits to the resolution.

A second-order noise shaping is achieved by allowing a double differentiator noise transfer function as defined by

$$F_Q(z) = (1-z^{-1})^2. \qquad (2\text{-}39)$$

This noise transfer function has a double zero at DC. The corresponding single loop filter

transfer function is obtained by substituting (2-39) into (2-34) and doing some simple algebra. The second-order ΣΔ modulator loop filter transfer function is

$$H(z) = \frac{z^{-1}(2 - z^{-1})}{(1 - z^{-1})^2} \ . \qquad (2\text{-}40)$$

The in-band power of quantization noise at the output of a second-order ΣΔ modulator is [Candy92]

$$n_0^2 = \frac{\Delta^2}{12}\frac{\pi^4}{5}\left(\frac{1}{OSR}\right)^5 \ . \qquad (2\text{-}41)$$

Doubling the OSR reduces the quantization noise by $15\ \text{dB}$, adding 2.5 bits to the resolution of a second-order ΣΔ modulator.

2.4.2 Bandpass Sigma-Delta Modulators

The basic principle of noise shaping can be extended by placing the quantization noise nulls at an arbitrary center frequency f_0. Then, the quantization noise will be pushed away from the signal band (BW) at the desired center frequency.

A simple way of designing bandpass ΣΔ modulators is to perform a lowpass to bandpass transformation. One such transformation in the discrete-time domain is achieved by the following change of variable,

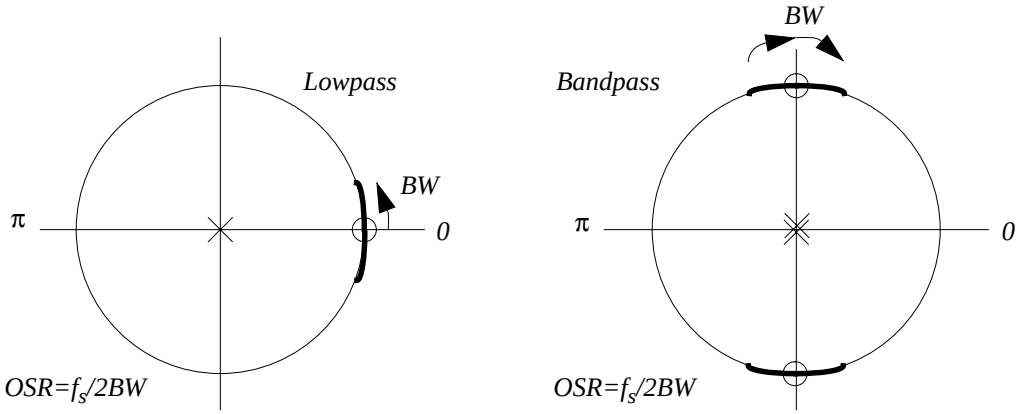
$$z^{-1} \rightarrow -z^{-2} . \qquad (2\text{-}42)$$

This transformation maps the zeros of the lowpass prototype from DC to $\pm f_s/4$. Therefore, noise in the resulting bandpass modulator is suppressed around the $f_s/4$ and the $3f_s/4$ frequencies. The stability and SNR characteristics of this bandpass modulator will be identical to that of the lowpass prototype [Jantzi].

In the following, the above transformation, equation (2-42), is applied to a first-order lowpass ΣΔ modulator H_{lp1}. The resulting bandpass modulator, H_{bp2}, is a second-order modulator as expected from (2-42).

$$H_{lp1} = \frac{-z^{-1}}{1 - z^{-1}} \rightarrow H_{bp2} = \frac{z^{-2}}{1 + z^{-2}} \qquad (2\text{-}43)$$

The above mapping is illustrated in Figure 2.12.



(a) (b)

Figure 2.12: Pole/zero placement of (a) a first-order lowpass ΣΔ and (b) a second-order bandpass ΣΔ derived by $z^{-1} \rightarrow -z^{-2}$ transformation

For a bandpass ΣΔ modulator with center frequency f_0 located at $f_s/4$, the oversampling ratio is simply $2f_0/BW$.

The second-order ΣΔ modulator represented by (2-40) can also be transformed to a fourth-order bandpass ΣΔ modulator as follows:

$$H_{lp2}(z) = \frac{-z^{-1}(2 - z^{-1})}{(1 - z^{-1})^2} \rightarrow H_{bp4}(z) = \frac{z^{-2}(2 + z^{-2})}{(1 + z^{-2})^2} \qquad (2\text{-}44)$$

The stability of this fourth-order bandpass ΣΔ modulator H_{bp4} is assured due to the stability of the second-order lowpass prototype H_{lp2}.

2.4.3 High-Speed SC Bandpass Sigma-Delta Modulator

Bandpass ΣΔ modulators allow A/D conversion to be performed on narrow-band signals at IF (Intermediate Frequency) frequencies. These A/Ds are useful in some communication systems, such as AM radio, digital radio, and in high speed modems. Digitizing the analog signal at a high IF and processing the signal in the digital domain is desirable due to the

robustness of digital circuits.

High-speed analog signal processing will be dominated by continuous-time Gm-C [Shoaei94] or LC based circuits. These circuits typically require tuning circuitry which is non-trivial. Recently, a high-speed bipolar sampled-data bandpass ΣΔ modulator has been reported [Varelas96]. Here, we focus on high-speed SC implementation of bandpass ΣΔ modulator using standard CMOS processes.

In the following, monolithic bandpass ΣΔ modulators reported in refereed publications are discussed and their performances summarized.

The first reported monolithic bandpass ΣΔ modulator was a fourth-order SC circuit with optimally placed zeros for noise transfer function [Jantzi92]. This modulator was implemented in a 3 μm, ±5 V, double-poly analog CMOS process. It operated at a 1.82 MHz clock and achieved a 63 dB SNDR for signals at 455 kHz IF with a 10 kHz bandwidth.

Another fourth-order SC bandpass ΣΔ modulator operating at a 7.2 MHz clock frequency was reported in [Longo93]. This modulator has a transfer function similar to H_{bp4} in equation (2-44) and is implemented in a 1 μm double-poly CMOS technology. The resonators are built using two SC delay cells in a negative feedback loop. Over a 30 kHz bandwidth centered at 1.8 MHz, the measured SNDR is 75 dB. This modulator operates at 5 V and consumes 40 mW.

A high-speed second-order SC ΣΔ modulator operating at a clock frequency of 42.8 MHz was described by Singor and Snelgrove in [Singor94]. This modulator was implemented in a 0.8 μm, double-poly BiCMOS technology. The transfer function of this modulator is identical to H_{bp2} in equation (2-43) and the resonator is implemented using LDI and FE SC integrators. A performance of 55 dB SNDR was achieved in a 200 kHz bandwidth centered at 10.7 MHz, while dissipating 60 mW from a 5 V power supply.

In [Song95], a hardware efficient fourth-order bandpass SC ΣΔ is described which requires two opamps instead of four. The two opamps consume 0.8 mW from a 3.3 V power supply. This modulator is based on a 2-path system and is designed in a 2 μm CMOS technology. The circuit is clocked at 8 MHz and the measured SNDR is 56 dB in

a 30 kHz bandwidth.

A 6th-order two stage (4-2) bandpass ΣΔ modulator is reported in [Hairapet96]. This modulator uses a pseudo-two-path SC resonator with one opamp. A dynamic range of 72 dB is achieved for this bandpass A/D converter over a bandwidth of 200 kHz and an IF frequency of 3.25 MHz. This modulator is implemented in a 0.8 μm CMOS technology and consumes 7 mW from a 3 V supply.

In [Norman96], a 160 MHz fourth-order bandpass ΣΔ modulator in a 0.8 μm BiCMOS technology is reported. A dynamic range of 84 dB is achieved for a signal bandwidth of 2.5 MHz centered at 5 MHz in a medical ultrasound application. The architecture of this modulator is based on a SC integrator.

Summary

Oversampled sigma-delta converters are compatible with VLSI technology due to their architecture which contains simple analog circuitry followed by a complex digital signal processing unit. A narrow-band signal at IF can be digitized using a bandpass ΣΔ modulator. A simple transformation from lowpass to bandpass is achieved by a $z^{-1} \rightarrow -z^{-2}$ change of variable.

2.5 Analog Circuit Design in a Standard Digital CMOS Process

As CMOS VLSI technology advances to finer geometries, more analog functions of a mixed-signal chip find economic solutions in the digital domain. Advantages of digital circuits over analog include noise immunity, programmability, efficient scaling with technology, availability of excellent automated design tools, and a systematic test strategy. The boundary between digital and analog circuits is moving toward minimizing the amount of analog circuitry. However, interfacing with the physical world requires analog circuits at least for implementing A/D and D/A converters.

A cost effective implementation of mainly digital mixed-signal circuits requires the analog circuits to be implemented in a standard digital CMOS process.

In CMOS, analog circuits are usually implemented using SC techniques due to their high circuit accuracy. SC circuits are traditionally implemented in CMOS processes where

linear double-poly capacitors are available. Since a standard digital CMOS process does not offer a second layer of polysilicon, therefore, the double-poly option requires a process change to the mainstream digital CMOS technologies. In a predominantly digital mixed-signal chip, the extra cost associated with the special double-poly process option may not be justifiable.

To address this problem, a new sampled-data analog signal processing technique, called Switched-Current (SI) was proposed by Hughes [Hughes89]. This technique requires only MOSFET transistors in a dynamic current circuit configuration to perform analog signal processing. Thus, it is compatible with baseline digital CMOS technologies. However, reported performance results for SI circuits indicate poor accuracy due to settling error and charge injection. In a recent publication [Nedved95], 11 bits of resolution is measured over the voice-band for a $5\ \mathrm{V}$ $\Sigma\Delta$ modulator operating at $1.024\ \mathrm{MHz}$. For the same modulator, SC circuits have achieved 14 bits.

In section 2.5.1, the SI technique is described and in section 2.5.2, two high performance memory cells are discussed. Different techniques for implementing linear SC circuits in a single-poly digital CMOS process are presented in section 2.5.3.

2.5.1 SI Circuit Technique

Signal processing in the analog sampled-data domain requires four operations on the signals, namely: summation, inversion, scaling, and delay [Fiez90]. SC technique uses MOSFET transistors and floating capacitors as basic components to realize these operations.

A simple weighted current mirror, Figure 2.13, does the inversion, summation, and scaling operations. The output current i_o is given by

$$i_o(n) = -A[i_1(n) + i_2(n)] \quad , \qquad (2\text{-}45)$$

where A is the aspect ratio (W/L) of N_2 with respect to the aspect ratio of N_1.

A delay operation is achieved by adding a switch to a simple current mirror to isolate the gates of the MOSFETs N_1 and N_2 as shown in Figure 2.14.

This current sample-and-hold circuit is called a first generation memory cell [Hughes89]

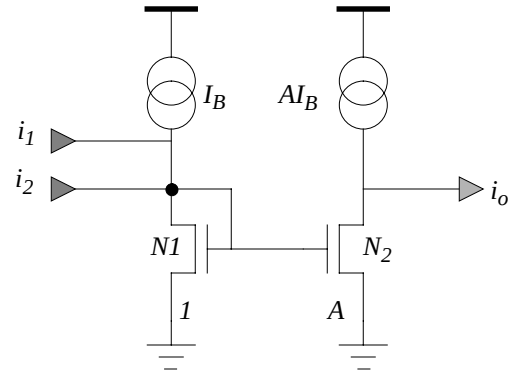


Figure 2.13: A weighted current mirror

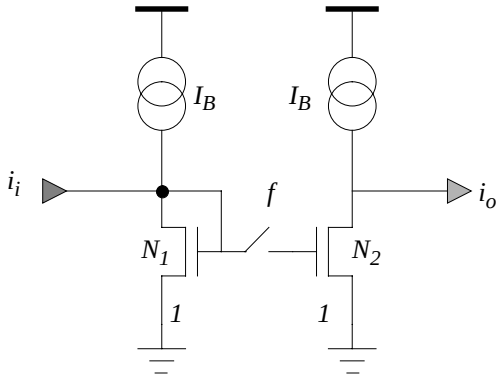


Figure 2.14: A first generation memory cell

and performs a half-delay operation. The transfer function $H(z)$ of this circuit is

$$H(z) = \frac{i_o(z)}{i_i(z)} = -z^{-1/2} \quad . \qquad (2\text{-}46)$$

A non-inverting damped integrator is realized using a full delay cell (two half-delay cells in cascade) in a feedback loop as shown in Figure 2.15 along with its corresponding 2-phase non-overlapping clock.

The transfer function of this integrator is

$$H(z) = \frac{Az^{-1}}{1 - Bz^{-1}} , \qquad (2\text{-}47)$$

which corresponds to the Forward Euler transformation ($s \rightarrow 1/T[(1 - z^{-1})/z^{-1}]$) of

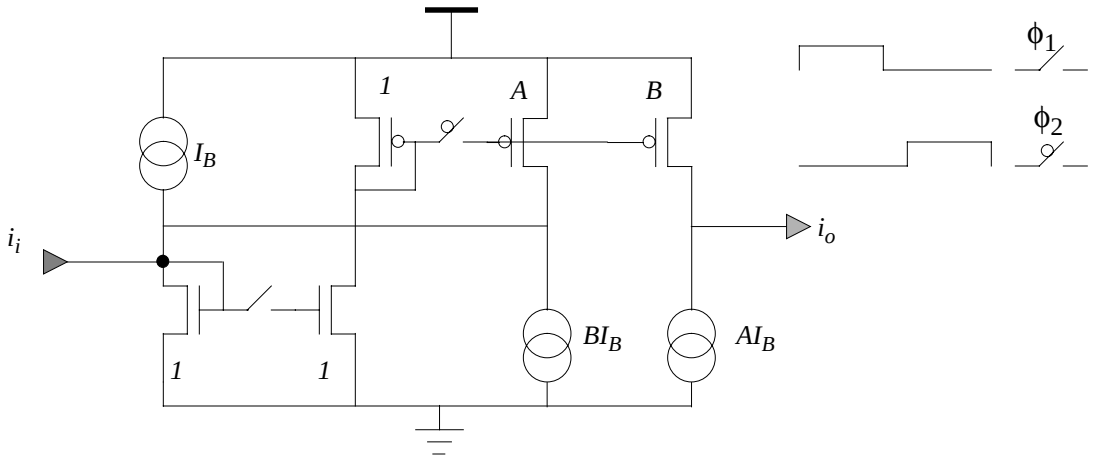


Figure 2.15: First generation SI integrator

the following continuous time integrator.

$$H(s) = \frac{a_0}{1 + \frac{s}{\omega_0}} \qquad (2\text{-}48)$$

a_0 is the DC gain and ω_0 is the cut-off frequency.

The sampled data integrator of (2-47) corresponds to the continuous time integrator of (2-48) with a phase shift ($e^{(-j\omega T)/2}$) [Battersby93] and

$$a_0 = \frac{A}{1-B} \qquad \omega_0 = \frac{2}{T}\left(\frac{1-B}{1+B}\right). \qquad (2\text{-}49)$$

The sensitivity of x with respect to variation in y is defined as

$$S\Big|_y^x = \left(\frac{y}{x}\right)\frac{\partial x}{\partial y}. \qquad (2\text{-}50)$$

The sensitivity of the cut-off frequency and DC gain with respect to variation in B is found to be:

$$S\Big|_B^{a_0} = \frac{B}{1-B} \qquad S\Big|_B^{\omega_0} = \frac{2B}{1-B^2} \qquad (2\text{-}51)$$

Thus, the performance of this integrator with a low damping factor ($B \to 1$) is very sensitive to variation in the coefficient B which is determined by transistor matching.

The second generation memory cell [Hughes90], shown in Figure 2.16, solves the MOSFET mismatch problem by utilizing the same transistor for sampling the signal as well as holding it.

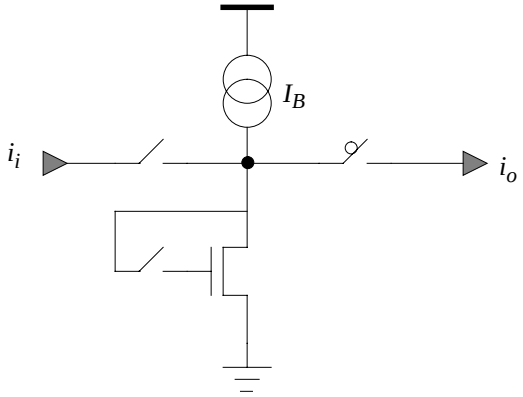


Figure 2.16: Second generation SI memory cell

A lossless non-inverting integrator circuit constructed using a second generation SI

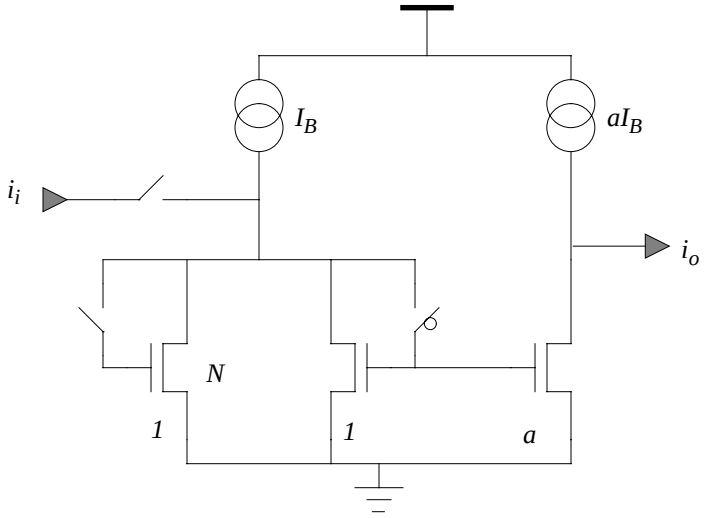


Figure 2.17: A second generation non-inverting lossless integrator

memory cell is shown in Figure 2.17. The transfer function of this circuit is

$$H(z) = \frac{\alpha z^{-1}}{1 - z^{-1}} . \qquad (2\text{-}52)$$

A damped non-inverting integrator is obtained by adding feedback to the lossless

integrator as shown in Figure 2.18.

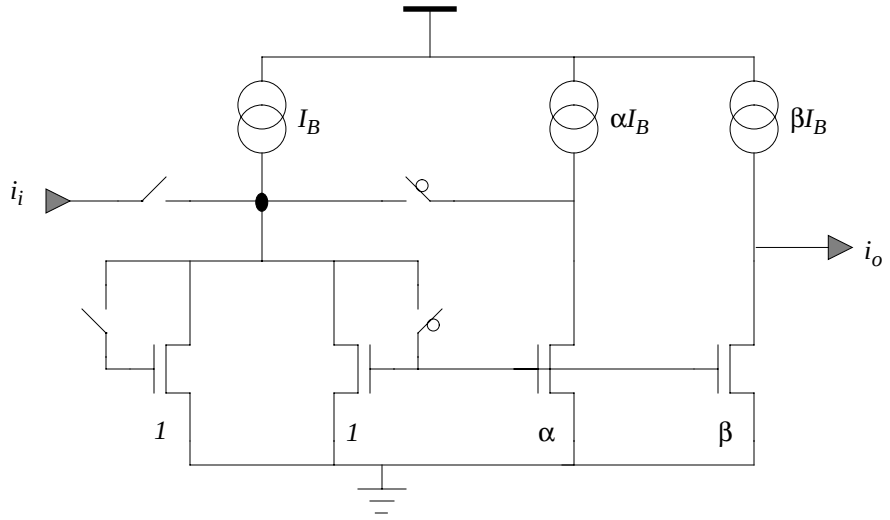


Figure 2.18: Second generation damped integrator

The transfer function of the above damped integrator is

$$H(z) = \frac{Az^{-1}}{1 - Bz^{-1}} \qquad (2\text{-}53)$$

where

$$A = \frac{\beta}{1+\alpha} \qquad B = \frac{1}{1+\alpha}. \qquad (2\text{-}54)$$

Cut-off and DC gain sensitivity with respect to α and β are

$$S\big|_B^{a_0} = 1 \qquad S\big|_B^{\omega_0} = 0 \qquad (2\text{-}55)$$

$$S\big|_B^{a_0} = -1 \qquad S\big|_B^{\omega_0} = \frac{2}{2+\alpha}. \qquad (2\text{-}56)$$

Both ω_0 and α_0 exhibit low sensitivity to variations in α and β.

2.5.2 High Performance Memory Cells

An ideal SI memory cell must exhibit infinite input conductance g_i during the sampling phase and infinite output resistance r_o during the hold phase. However, the simple memory cell in Figure 2.16 has a finite input impedance g_m and output resistance $1/g_{ds}$.

The accuracy of a SI circuit is proportional to $g_i r_o = g_m / g_{ds}$. There are many circuit techniques proposed to improve the accuracy of SI circuits. Here, two prominent methods, regulated cascode [Toumazou90] and S^2I [Hughes93] are discussed.

Regulated Cascode Memory Cell

The regulated cascode memory cell, illustrated in Figure 2.19, is based on a regulated cascode current mirror [Sackinger87] that improves the output conductance of the memory cell by a factor which is higher than that of simple cascoding.

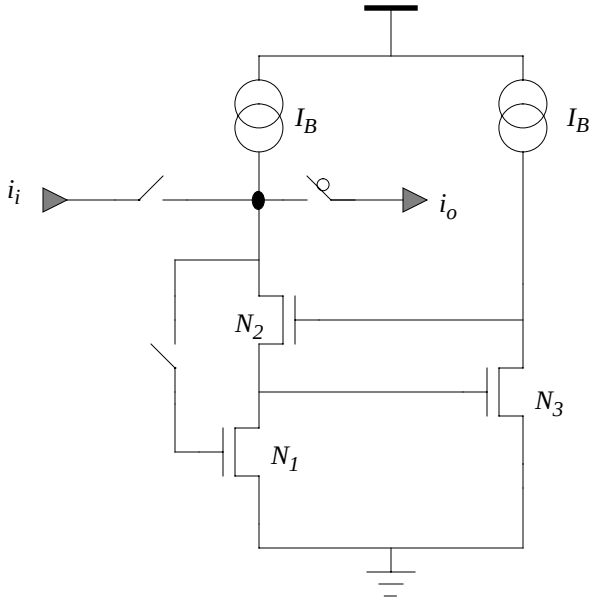


Figure 2.19: Regulated cascode memory cell

This cell operates as follows. During the sampling phase the voltage on the gate of $N1$ reaches v_{GS1} to maintain a drain current of $I_B + i_i$. In the hold phase, the gate of $N1$ is isolated and the sampled current is fed to the output. The negative feedback loop formed by transistors $N2$ and $N3$ keeps the voltage v_{DS1} constant at a value of v_{GS3}.

The input and output conductance of this circuit are

$$g_i = g_{m1} \qquad r_o = \frac{g_{m2} g_{m3}}{g_{ds1} g_{ds2} g_{ds3}}. \tag{2-57}$$

Compared to a simple current copier, the value of $g_i r_o$ for a regulated cascode is higher

by a factor of $(g_{m2}g_{m3})/(g_{ds2}g_{ds3})$.

S²I Memory Cell

A two-step memory cell, called S²I cell, and its associated clock waveforms are shown in Figure 2.20.

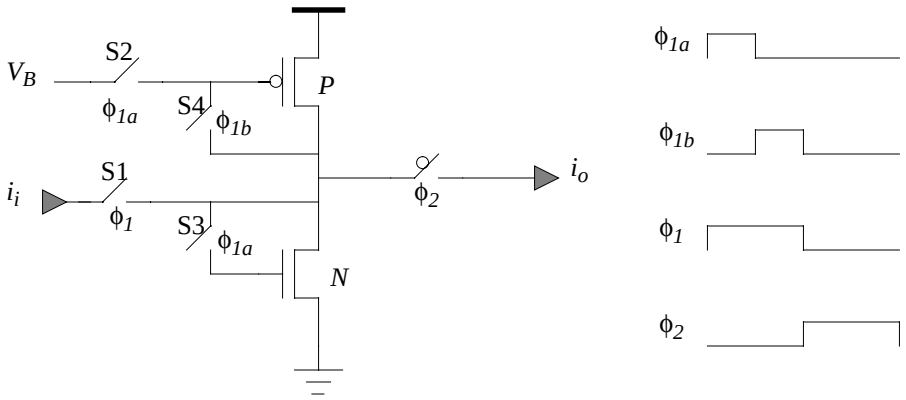


Figure 2.20: S²I memory cell

On phase ϕ_{1a}, the coarse memory transistor N is diode connected and the input current is sampled. The bias current is provided by transistor P during this phase. During ϕ_{1b}, the gate of N is opened and its drain-source current will be sustained (parasitic C_{gs} holds the gate to source voltage). Circuit non-idealities and charge injection from sampling switch $S1$ cause the stored current in N to be different than the input current. The fine memory transistor P is now diode connected and will sample the difference between the actual input current i_i and the stored current i_{ds1}. This difference is the error current caused during the coarse sampling phase. On phase ϕ_2, the stored current (in N) is subtracted from the error current (in P) and provides an error free output current i_o.

2.5.3 Linear SC Circuit Techniques in a Digital CMOS Process

As previously discussed, implementation of the linear SC circuits requires linear floating capacitors. In standard digital CMOS processes, where a linear double-poly capacitor is not available, parasitic poly-to-metal or metal-to-metal capacitors may be used as linear capacitors. The parasitic capacitance per unit area is typically low (0.05 fF/μm²) compared to that of a poly-poly capacitor, which is 1 fF/μm². The penalty of using parasitic capacitances is the increase in silicon real estate (by a factor of almost 20) that

may not be acceptable if the total capacitance used in the circuit is large.

Another type of capacitor available in CMOS processes is the MOSFET gate capacitor, which is the one exploited in SI circuits. The capacitance per unit area of a MOSFET gate capacitor is typically higher (by a factor of $1.5 – 2.5$) than the capacitance per unit area of a poly-poly capacitor. However, MOSFET gate capacitance exhibits a non-linear behavior as shown in Figure 2.21.

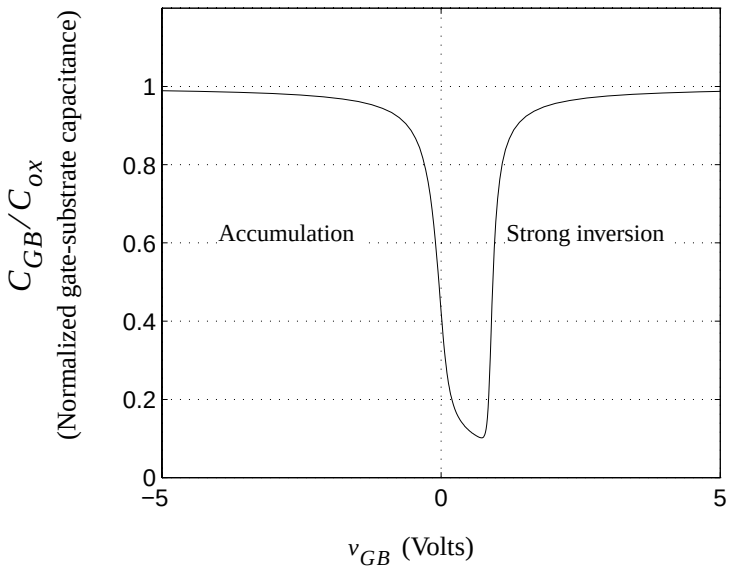


Figure 2.21: nMOSFET CV plot

Reported research in the area of employing MOSFET gate capacitance to realize a linear SC circuit is reviewed in the following section.

Weakly Non-linear MOSFETs

As can be seen from the CV characteristics of an nMOSFET shown in Figure 2.21, a relatively linear capacitor is achieved by operating the MOSFET in strong inversion ($v_{GS} > V_t$) or accumulation ($v_{GS} < 0$) regimes. Techniques to bias the MOSFETs in strong inversion or accumulation to reduce distortion in the SC filter design were first reported in [Montoro88].

A theoretical analysis of the harmonic distortion caused by the weakly non-linear MOSFET capacitors biased in strong inversion or accumulation is described in [Behr92]. It is shown that distortions due to these capacitors are technology independent. The

voltage coefficient α (called V_{cc} in [Behr92]) for gate MOSFET capacitor is derived from

$$\alpha = \frac{1}{C_g}\left|\frac{dC_g}{dv_{GB}}\right|, \qquad (2\text{-}58)$$

where C_g is the gate capacitance and v_{GB} is the gate to bulk voltage. For a MOSFET gate capacitor biased at $v_{GB} = V_R$, the voltage coefficients in strong inversion and in the accumulation region are given respectively by

$$\alpha|_{str} = \frac{2\phi_t}{(V_R - V_t)^2} \qquad (2\text{-}59)$$

$$\alpha|_{acc} = \frac{2\phi_t}{(V_R - V_{FB})^2}. \qquad (2\text{-}60)$$

Here, ϕ_t is the thermal voltage and V_{FB} is the flat band voltage. A voltage capacitance coefficient of 17 kppm/V is obtained for a MOSFET with a V_t of 0.8 V, biased 2.5 V in strong inversion.

A simple damped integrator circuit is used to test MOSFET capacitors. Measured THD results are in good agreement with computed results showing that approximately –40 dB THD is achievable using a 3 V signal swing.

In another study [Schneider94], an explicit formula is derived for the harmonic distortion in SC circuits with a weakly non-linear capacitor. It is shown that harmonic distortions as low as –40 dB to –60 dB can be obtained in SC filters using MOSFETs biased in strong inversion or accumulation as linear capacitors. A single-ended discrete SC biquad filter is implemented, using a Motorola P5N40 transistor as capacitor, to verify the theoretical analysis.

SC Circuits as Linear Charge Processors

In [Bermudez92], the basic operation of a SC circuit is considered as a charge mirror cell composed of capacitors and an opamp. The charge processing is linear and is independent of the non-linearity of the capacitors involved.

A charge mirror is shown in Figure 2.22. A charge q_A injected at the inverting terminal of the opamp will appear on capacitor C_A with the following relationship between charge and voltage:

$$q_A = C_{A0} f_A(v) v \,. \qquad (2\text{-}61)$$

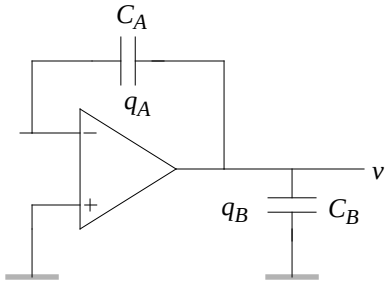


Figure 2.22: A charge mirror cell

A non-linear capacitor C_X is described by [Lee85]

$$C_X = C_{X0} f_X(v) \,. \qquad (2\text{-}62)$$

The parameter C_{X0} is the capacitance at zero voltage and is proportional to the area of the capacitor.

The charge on capacitor C_B, in Figure 2.22, is

$$q_B = C_{B0} f_B(v) \,. \qquad (2\text{-}63)$$

If capacitors C_A and C_B have the same non-linearity function, then

$$\frac{q_B}{q_A} = \frac{C_{B0}}{C_{A0}} = \frac{area(C_B)}{area(C_A)} \,. \qquad (2\text{-}64)$$

This is a linear charge mirror and the gain is defined by the area ratio.

A typical SC building block which performs summation, scaling and delay operation on two charge signals is shown in Figure 2.23.

In the charge domain, the operation is linear from input to output. If the external signals are in the voltage domain, a linear input V/Q and output Q/V converters are required.

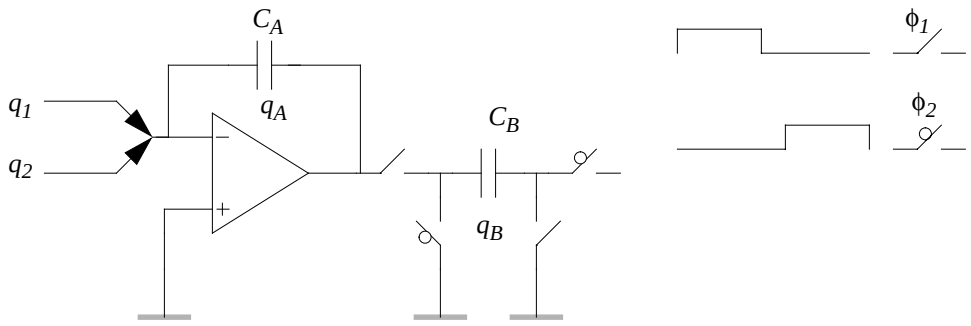


Figure 2.23: A SC building block

This means any capacitor connected to either inputs or output (voltage) must be a linear capacitor.

A High-Linearity MOSFET SC Branch

A high-linearity SC circuit branch using MOSFET capacitors, proposed in [Yoshizawa95], is shown in Figure 2.24. In this circuit, MOSFETs are biased in a weakly non-linear region (accumulation) and the non-linearity effects are canceled to a first-order, because the two capacitors are connected in series and back-to-back.

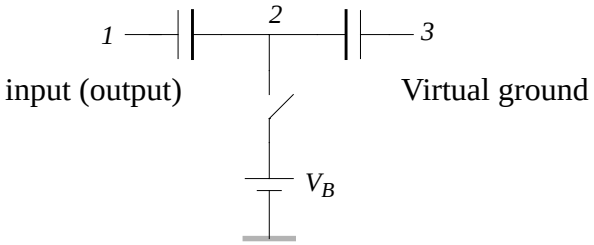


Figure 2.24: The MOSFET SC branch

This MOSFET capacitor branch can be used in a SC circuit as shown in Figure 2.25. An expression similar to (2-61) is used for the weakly non-linear capacitors C_A and C_B and it is assumed that $C_{A0} = C_{B0} = C$. If $V_{in}/2 \ll V_B$, it can be shown that the charge delivered by the SC branch during ϕ_2 is

$$\Delta q = \frac{C}{2}\left[f(V_B) + \left.\frac{df}{dv}\right|_{V_B} \right] V_{in}(n) \ . \qquad (2\text{-}65)$$

Since V_B is a constant voltage, the term in the bracket is a constant. Therefore, the effective capacitance term is a constant and Δq charge is a linear function of the $V_{in}(n)$ voltage.

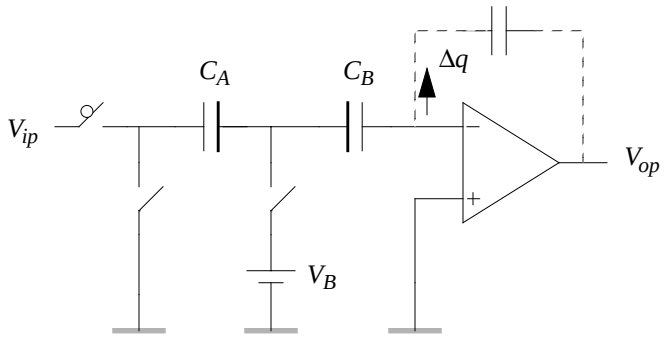


Figure 2.25: A SC circuit using the MOSFET SC branch

An experimental SC amplifier with a gain of 10 was implemented using pMOS capacitors in accumulation to verify the linearity of the above SC branch [Yoshizawa96]. For V_B = 1.5 V and a 400 mVpp input signal at 1 kHz, the largest harmonic was 72 dB below the fundamental of the input signal.

Summary

Sampled-analog circuits can be realized in standard digital CMOS process using SI or SC circuit techniques. In SC design, linear capacitors can be achieved using parasitic poly-to-metal or metal-to-metal capacitors or using MOSFET gate capacitors biased in strong inversion or accumulation regimes.

2.6 A Comparative Study of SC and SI for Low-Voltage Applications

Supply voltage down-scaling was shown to be essential in future deep submicron VLSI circuits to prevent problems caused by breakdown voltage, hot electron effects, and power dissipation. A reduced supply voltage decreases the voltage signal swing which in turn makes the design of high-speed wide dynamic range SC circuits a challenge. In SI circuits, the signal is in the current domain and this originally led some researchers to believe that the SI technique is more suitable for low-voltage analog design [Hughes90a] [Fiez90] [Battersby91]. Further research [Crawley92] [Temes93] [Bazarjani93] indicated that SI

would not benefit from supply voltage scaling. In this section, limits to low-voltage SC and SI are explored and it will be shown that SI exhibits no clear advantage over SC for low-voltage analog function. In fact, analysis of dynamic range (for a given supply voltage) indicates that SC circuits achieve a higher dynamic range than SI circuits.

A SC circuit consists of capacitors, opamps, and switches and a SI circuit comprises current mirrors and analog switches. In section 2.3, limits to low-voltage operation of the opamp, switch, and current mirror were investigated. A transmission gate switch requires a supply voltage of greater than $2V_t + 2V_{on}$. Both opamp and current mirror need a supply voltage of greater than $V_t + 2V_{on}$. Therefore, the minimum supply voltages required for proper operation of either SC circuits or SI circuits are the same.

An important performance parameter for low-voltage operation is the maximum achievable circuit dynamic range as defined by (2-25). For dynamic range comparison, the SC integrator circuit shown in Figure 2.7 and the SI integrator circuit shown in Figure 2.17 are considered.

The maximum output voltage swing in the SC integrator is determined by the linear voltage swing at the output of the opamp. For a two-stage opamp, as shown in Figure 2.26, the maximum output voltage swing is

$$V_{swing(opamp)} = V_{DD} - 2V_{on}, \qquad (2\text{-}66)$$

where V_{on} is the minimum v_{DS} voltage needed to keep the output transistors $N4$ and $P3$ in the opamp (Figure 2.26) in saturation. The noise in a SC circuit is limited by kT/C and the circuit dynamic range is

$$DR|_{SC} = \frac{V_{DD} - 2V_{on}}{\sqrt{(8kT)/C_S}}. \qquad (2\text{-}67)$$

In the SI circuit, during the sampling phase the minimum voltage on the gate of N is $V_t + V_{on}$ and the maximum voltage on the gate of N can rise to $V_{DD} - V_{on}$, to keep P in saturation. The voltage signal swing on the gate of N is

$$V_{swing(SI)} = V_{DD} - V_t - 2V_{on}. \qquad (2\text{-}68)$$

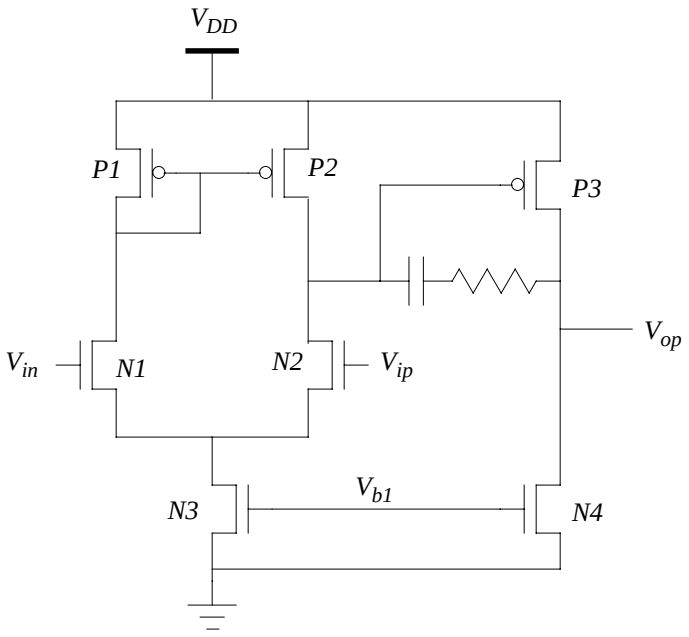


Figure 2.26: A two-stage pole-splitting opamp

The minimum stored voltage on the gate capacitance of the nMOSFET transistor $N1$ must be greater than the thermal noise kT/C_g, where C_g is the gate capacitance of $N1$. The dynamic range of the SI integrator is

$$DR|_{SI} = \frac{V_{DD} - V_t - 2V_{on}}{\sqrt{(8kT)/C_g}}. \qquad (2\text{-}69)$$

For example, assuming $C_s = C_g$, $V_t = 0.6$ V, $V_{DD} = 1.6$ V, and $V_{on} = 0.2$ V the DR of the SC integrator is 6 dB larger than the DR of the SI integrator.

2.7 Summary

In this chapter, CMOS scaling in deep submicron technologies was reviewed and it was mentioned that supply voltage has started to scale down due to reliability issues. Along with the supply voltage, threshold voltage must be scaled down to achieve high speed circuits. Threshold voltage scaling issues due to non-scalability of subthreshold swing were discussed. Limits to digital and analog supply voltage scaling were discussed and it was shown that a large margin for supply voltage reduction exists for digital CMOS. Dynamic power consumption in CMOS logic is reduced quadratically with supply voltage

reduction factor. A first-order analysis showed that for a given dynamic range and speed, power consumption of an analog circuit is independent of the supply voltage. Research in the area of low-voltage digital and analog circuits was presented.

Then, ΣΔ modulators, which are the benchmark circuits in this thesis, were introduced and reported high-speed bandpass SC ΣΔ modulators were reviewed.

Finally, analog circuit techniques that allow mixed-signal circuit to be implemented in a standard digital CMOS process were presented.

Chapter 3

Low-Voltage SC Design with Low-V_t MOSFETs

In Chapter 2, CMOS scaling was reviewed and it was discussed that in deep submicron technologies the supply voltage is scaling down to assure device reliability. In conjunction with supply voltage, MOSFET threshold voltage must be reduced to attain high-speed circuits. However, lowering the threshold voltage of MOSFET transistors will increase the subthreshold off-current which raises the standby power dissipation in digital circuitry and limits the accuracy of analog SC circuits. It was discussed that scaling the supply voltage along with the threshold voltage reduces the total power dissipation in digital CMOS. Low-voltage analog SC circuit techniques using low-V_t MOSFETs are investigated in this chapter.

Low-V_t MOSFETs are available in advanced 0.1 μm CMOS technologies. This chapter starts by presenting two different methods of achieving low-V_t MOSFETs in the current CMOS processes; the first scheme may involves a process change, and the second method uses circuit techniques. Accuracy degradation in SC circuits due to the subthreshold leakage current of low-V_t MOSFET transmission gate switch is analyzed next. Then, methods for reducing the subthreshold leakage in analog switches are discussed and two new switch topologies, the series transmission gate and composite switch [Bazarjani94b], addressing this problem are proposed. Finally, the design and measured results for two low-voltage SC ΣΔ modulators are presented. The first design is a 2.25 V second-order ΣΔ modulator designed in a 0.8 μm BiCMOS technology using short-channel (0.6 μm) MOSFET switches. This modulator operates at a 2.5 MHz clock rate and achieves 92 dB

SNDR over the C-message weighted telephony bandwidth (60 Hz – 5 kHz). The second design is a 1 V first-order ΣΔ modulator implemented in a 0.5 μm CMOS process using low-V_t natural MOSFETs. This modulator is clocked at 1 MHz and has 54 dB dynamic range for an oversampling of 128 (voice band 4 kHz) and consumes about 100 μW.

3.1 A Low-V_t Process

As channel lengths of MOSFET transistors are shrunk to 0.5 μm and below, buried-channel pMOSFET devices with strong short-channel effects (SCEs) must be replaced with surface channel devices. SCE is a combination of several 2-D phenomena in short channel MOSFETs and is expressed as V_t roll-off due to channel shortening [Tsividis87].

Fabrication of surface-channel MOSFETs requires a dual poly gate process technology where n^+-poly is used for nMOSFETs and p^+-poly is used for pMOSFETs. In such technologies, the natural threshold voltages of the transistors are set by the well implants and are given by [Chen90],

$$V_t = V_{FB} + 2\phi_F + \sqrt{2q\varepsilon_{si}N_W(2\phi_F)}/C_{ox} \qquad (3\text{-}1)$$

where V_{FB} is the flat-band voltage, ϕ_F is the bulk Fermi potential, N_W is the device well doping concentration, and C_{ox} is the gate specific capacitance. V_{FB} and ϕ_F are related to process parameters and physical constants by

$$V_{FB} = \phi_{MS} - \frac{\hat{Q}}{C_{ox}} \qquad (3\text{-}2)$$

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_W}{n_i}\right), \qquad (3\text{-}3)$$

where $\hat{Q}$ is the fixed charge density and ϕ_{MS} is the gate-to-substrate workfunction. In an n^+/p^+ dual poly gate CMOS technology, the threshold voltages of the natural MOSFETs are symmetric. This is due to the symmetrical gate-to-substrate workfunction of the MOSFETs, as shown in Figure 3.1.

The ϕ_{MS} for nMOSFETs and pMOSFETs are

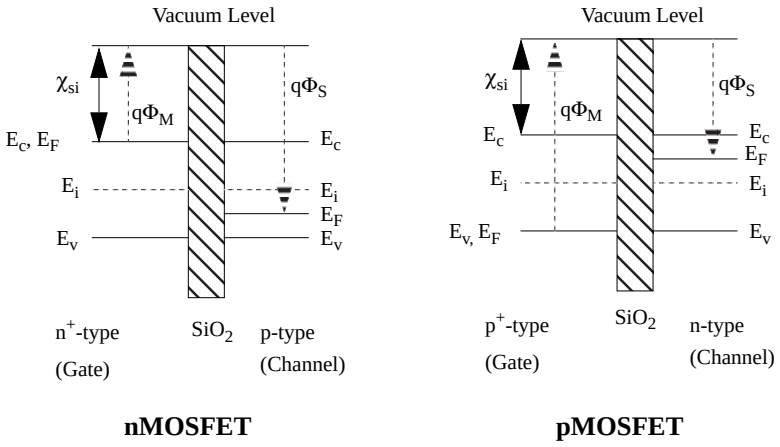


Figure 3.1: Gate-substrate workfunction of nMOSFET and pMOSFET in an n+/p+ dual poly gate CMOS process

$$\phi_{MS}\big|_{nMOSFET} = -\left(\frac{E_g}{2q} + \phi_F\right) \qquad (3\text{-}4)$$

$$\phi_{MS}\big|_{pMOSFET} = \left(\frac{E_g}{2q} + \phi_F\right). \qquad (3\text{-}5)$$

Here, E_g is the bandgap energy which is about 1.124 eV at room temperature and q is the charge of an electron that is 1.602×10^{-19} C.

Example 3.1: Assuming a fixed charge density of 2×10^{10} q/cm^3 and device well dopings of 4×10^{16} q/cm^3, the natural threshold voltage of MOSFETs in a typical 0.5 μm CMOS technology with gate oxide thickness of 12 nm is found to be $V_t = 220$ mV.

In some dual n^+/p^+ poly gate processes [Sun92], it is possible to mask out the threshold adjust implant and obtain the low-V_t natural MOSFETs. In the next section, device characteristics of an experimental 1 V CMOS process [Bazarjani95b] are described.

Experimental Natural MOSFETs

Natural threshold voltage CMOS transistors have been fabricated using a 0.5 μm CMOS process. This process does not require any threshold adjust implant (for natural MOSFETs). For 1 V operation, this process can be further simplified by eliminating the steps required for hot-carrier reduction i.e., Lightly-Doped-Drain (LDD).

The threshold voltages of 0.5 μm channel length nMOSFET and pMOSFET devices are measured to be 202 mV and 197 mV respectively. Figure 3.2 and Figure 3.3 show the I_D and G_m versus gate voltage for a 20 μm / 0.5 μm nMOSFET and a 20 μm / 0.5 μm pMOSFET biased at V_{DS} = 0.1 V respectively.

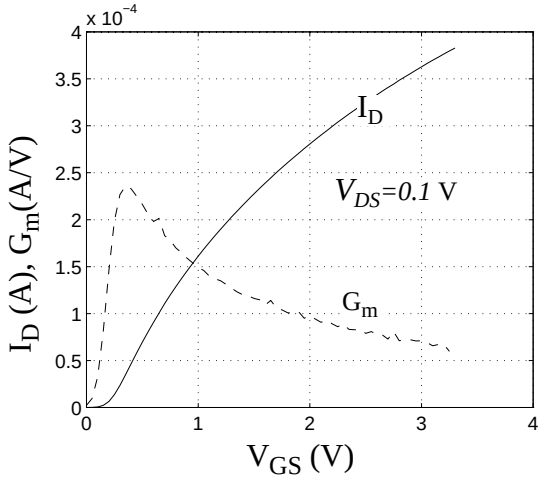


Figure 3.2: Measured I_D (A) and G_m (A/V) versus V_{GS} (V) for "natural" nMOSFET

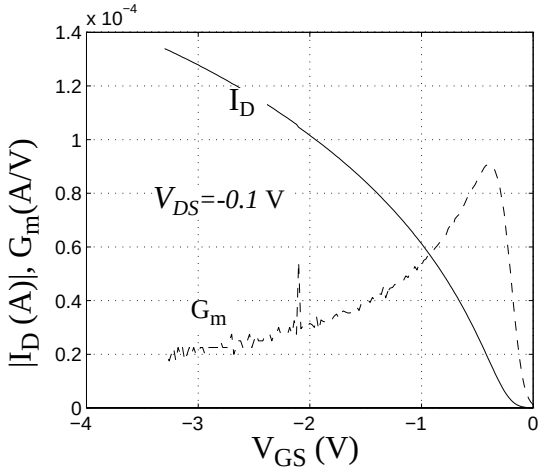


Figure 3.3: Measured $|I_D$ (A)| and G_m (A/V) versus V_{GS} (V) for "natural" pMOSFET

Subthreshold slopes are measured to be 78 mV/decade as illustrated in Figure 3.4.

Summary

Low-V_t natural threshold voltage MOSFETs can be fabricated as a by-product of a dual

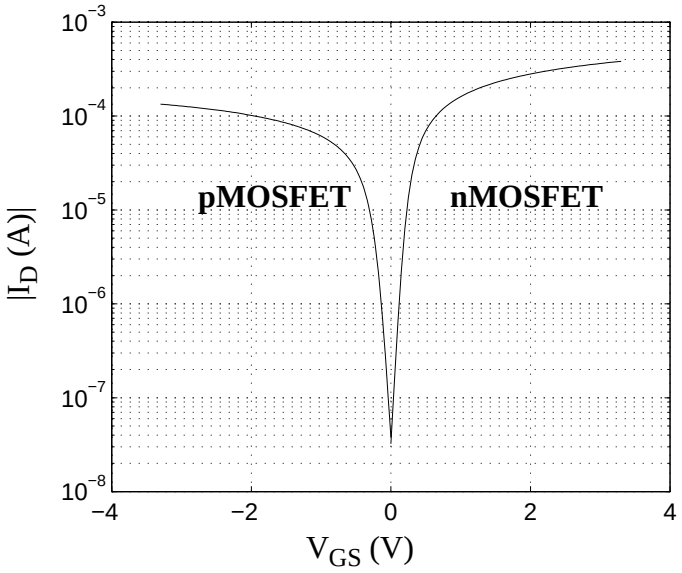


Figure 3.4: Measured subthreshold characteristics of natural nMOSFET and pMOSFET

poly gate CMOS process where the threshold voltage is set by a well implant. The natural MOSFET is obtained by selectively shielding the threshold adjust implant or removing the steps for threshold adjust for the whole wafer. Measured results, for a 0.5 μm technology, indicate that typical values for V_t and S are about 200 mV and 80 mV/decade respectively. These low-V_t natural MOSFETs are suitable for low-voltage ($V_{DD} \sim 1$ V) mixed-signal design. In a dual-V_t process, the low-V_t transistors can be used to achieve higher speed in digital circuits. In Chapter 5, application of a low-V_t MOSFET to the design of a high-swing linear MOSFET capacitor will be discussed.

3.2 Circuit Technique for V_t Reduction

If a low-V_t process is not available, circuit techniques must be used to reduce the threshold voltage. In this section, methods of reducing the threshold voltage by 100 mV to 200 mV are discussed.

(I) Low-Vt Short-Channel Devices: Taking advantage of SCEs

As the channel length of a MOSFET transistor is made smaller than a critical value (L_{min}), several 2-D phenomena known as short channel effects (SCEs) will occur. The onset of SCEs is empirically given [Brews80] by

$$L_{min} = 8.8[r_j t_{ox}(W_S + W_D)^2]^{1/3}. \quad (3\text{-}6)$$

Normally, process engineers select the minimum feature size of the technology (L_0) to be slightly greater than L_{min}. One of the characteristics of short channel devices is that threshold voltage rolls off quickly as channel length is reduced below L_{min}. Figure 3.5 illustrates the threshold voltage as a function of channel length, for a generic 1.5 μm CMOS technology, based on the charge-sharing model approximation formula [Tsividis87] given by

$$V_t(L) = V_{t0}\left(1 - \frac{\alpha_1}{L}\sqrt{\frac{2\varepsilon_{si}\phi_B}{qN_A}}\right). \quad (3\text{-}7)$$

Here, V_{t0} is the long channel threshold voltage, L is the channel length, ϕ_B is the surface potential at the onset of strong inversion which is approximately $2\phi_F$, and α_1 is a fitting parameter.

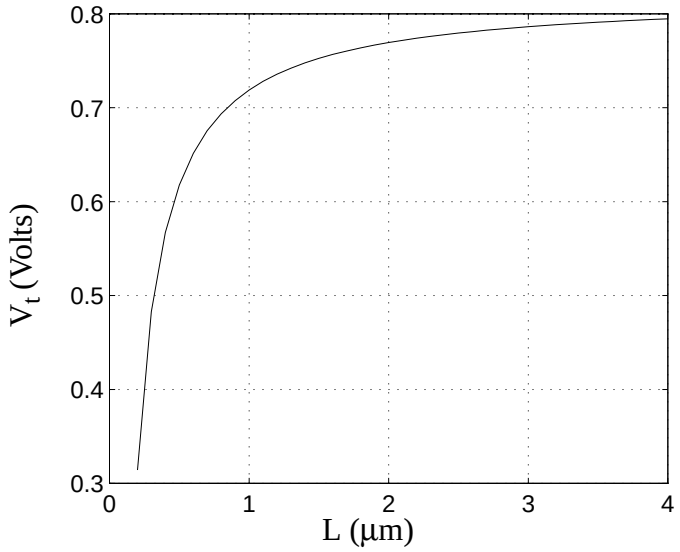


Figure 3.5: Threshold voltage as a function of channel length

MOSFET transistors with channel lengths shorter than the minimum feature size of a given technology (called “short-channel MOSFETs” hereafter), have lower threshold voltages due to SCE. These short-channel MOSFETs can be used as efficient analog

switches [Bazarjani94a] due to higher V_{on} (as a result of lower V_t), higher aspect ratio(W/L) for the same width, and lower charge injection (based on channel length reduction). However, undesirable SCEs, such as increased subthreshold conduction and punchthrough current, set a limit to the minimum channel length acceptable for the short-channel devices. Subthreshold conduction has been discussed before (section 2.2.2); in the following punchthrough is briefly discussed.

Short-channel MOSFETs are susceptible to barrier lowering that results in an unwanted current flow from drain to source. This phenomenon is affected by L and v_{DS}. Figure 3.6a shows a turned-off nMOSFET switch which is not affected by punchthrough. For $v_{DS} = 0$, the peak potential barrier is lowered if the channel length is not larger than the sum of the two depletion region widths (source and drain to substrate), as shown in Figure 3.6b. The barrier is lowered further for $v_{DS} > 0$ (Figure 3.6c) because field lines penetrate from drain to source [Troutman79]. The resulting punchthrough current has a two dimensional nature and no analytical model predicting it exists. Two dimensional computer simulation and experiments show that punchthrough current decreases as v_{DS} is lowered or negative bulk to source voltage is applied. In section 3.3, it will be shown that in a SC circuit all of the "off" switches have both back bias and a maximum v_{DS} lower than $V_{DD}/2$, which helps in reducing punchthrough current.

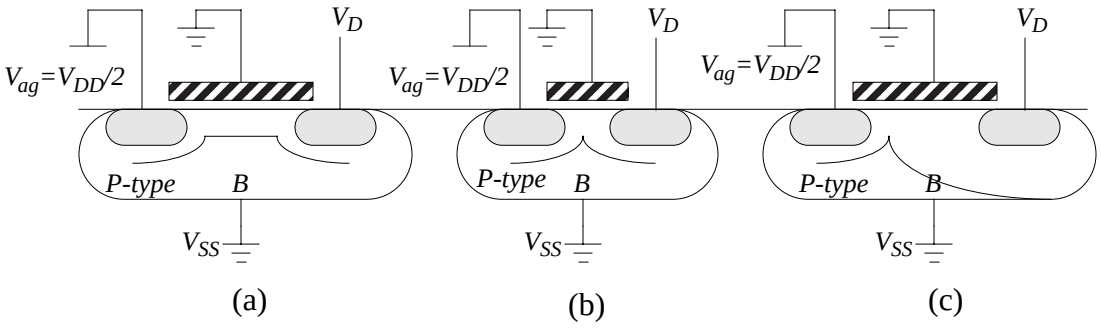


Figure 3.6: Turned-off nMOSFET switch exhibiting (a) no punchthrough, (b) punchthrough due to short channel length, and (c) punchthrough due to large drain to source potential

Channel length variation due to process fluctuation must be carefully considered for short-channel MOSFETs. A drawn channel length (L_0) can vary by "ΔL" due to error in

lithography and etching. For channel lengths below the minimum feature size in a given technology, this variation might be larger. Thus, the optimum channel length must be selected such that devices with the absolute minimum channel length obtained on silicon have acceptable subthreshold and punchthrough currents.

(II) Substrate Forward Biasing

The threshold voltage of MOSFETs is a function of source to substrate voltage, owing to the body effect and is given by

$$V_t = V_{t0} + \gamma(\sqrt{\phi_B + v_{SB}} - \sqrt{\phi_B}), \qquad (3\text{-}8)$$

where γ is the body effect coefficient defined as

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}. \qquad (3\text{-}9)$$

Application of a negative v_{SB} in nMOSFET (i.e. forward biasing the well potential with respect to source) will reduce the threshold voltage. However, junction forward bias current limits the maximum forward biasing to about $0.4\ \text{V}$.

Example 3.2: Assuming a γ of $0.5\ \text{V}^{1/2}$ and $\phi_B = 0.8\ \text{V}$, a forward bias voltage of $0.4\ \text{V}$ reduces the threshold voltage by about $130\ \text{mV}$.

Summary

In a CMOS process with a normal V_t, lower threshold voltage MOSFETs are obtained using short-channel MOSFETs or by forward biasing the well.

3.3 Low-V_t Transmission Gate Design for SC Circuits

In SC circuits, analog switches are implemented with MOSFET transistors having the following two distinct modes of operation.

"On" State:

In this case, MOSFETs operate in strong inversion-triode mode with a non-linear signal dependent on-conductance of approximately

$$g_{on} = 2\beta(v_{GS} - V_t), \qquad (3\text{-}10)$$

where $\beta = (1/2)(\mu C_{ox} W/L)$.

"Off" State:

A turned-off MOSFET transistor ($v_G = 0$) operates in the weak inversion regime and it can be modelled as a current source with the following value:

$$i_{off} = I_{D0}\frac{W}{L}10^{\frac{-(v_S + V_t)}{S}}. \qquad (3\text{-}11)$$

Here, S is the subthreshold swing (the gate voltage change needed to reduce the leakage current by one decade), and I_{D0} is the value of the drain current when the gate to source voltage of a unit transistor ($W/L = 1$) is set to V_t and is given by

$$I_{D0} = \mu C_{ox}\phi_t^2. \qquad (3\text{-}12)$$

An analog switch has several requirements, the most important ones being: low on-resistance, full signal swing handling, and low off-current.

A low on-resistance switch is obtained by using low-V_t MOSFETs. Rail-to-rail signal swing handling is achieved by using a full transmission gate (TG) switch also known as a complementary switch—an nMOSFET and a pMOSFET in parallel. Here, we focus on the behavior of the "off" switches in the context of stray-insensitive SC circuits.

Consider a stray-insensitive non-inverting SC integrator and its corresponding two-phase non-overlapping clock, as shown in Figure 3.7.

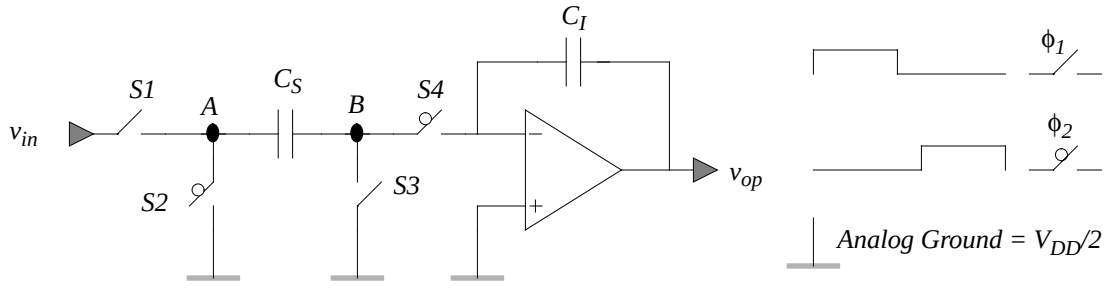


Figure 3.7: A non-inverting SC integrator

All the "off" switches have the following properties:

- At least one side of any "off" switch is connected to analog ground, either directly or through another switch. This is a critical property used in the development of a non-leaky switch as described later.
- The maximum drain to source voltage across an "off" switch is less than $V_{DD}/2$ and is given by

$$\left|v_{DS}\right|_{max} = max\left\{\left|(V_{DD}/2) - v_{in}\right|_{min}\right|, \left|\left|v_{in}\right|_{max} - (V_{DD}/2)\right|\right\} . \qquad (3\text{-}13)$$

Note that during off-state, the drain to source voltages of MOSFET switches $S3$ and $S4$ are almost zero. If the signal swing is limited to $V_{on} < v_{in} < V_{DD} - V_{on}$, the maximum drain to source voltage of switches $S1$ and $S2$ will be

$$\left|v_{DS}\right|_{max} = \frac{V_{DD}}{2} - V_{on}. \qquad (3\text{-}14)$$

- There is a negative back bias (bulk to source voltage for nMOSFET) on all the switches. Again, assuming the signal swing is reduced by V_{on} from each supply rail, the minimum back bias voltage on MOSFET switches $S1$ and $S2$ is

$$v_{SB} = V_{on}. \qquad (3\text{-}15)$$

Switches $S3$ and $S4$ have a back bias of $V_{DD}/2$.

The effects of low-V_t leaky MOSFET switches on the precision of analog SC circuits will be examined in the context of the non-inverting integrator illustrated in Figure 3.7. In this circuit, we assume that switch $S1$ is implemented with a full transmission gate and all the other switches are simply nMOSFET transistors. In the following, error voltages on nodes A and B due to finite on-resistance and off-current are analyzed for different periods of a complete clock cycle.

(I) During ϕ_1

The equivalent circuit of the non-inverting SC integrator (Figure 3.7) during ϕ_1 is shown in Figure 3.8.

The leakage i_{off2} is the off-current through the nMOSFET switch $S2$ and is calculated

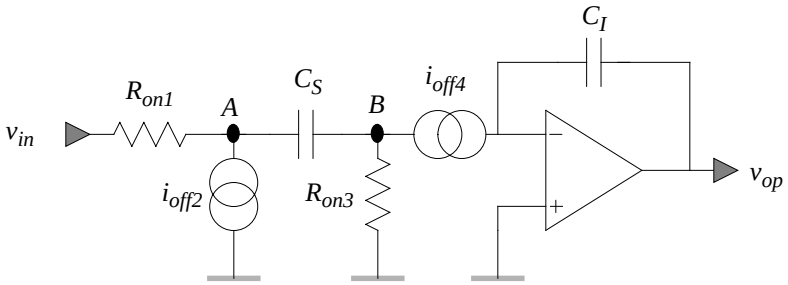


Figure 3.8: Equivalent circuit of Figure 3.7 during ϕ_1

from (3-11) to be:

$$i_{off2} = I_{D0}\frac{W}{L}10^{-\left(\frac{v_{in}+V_{tn}}{S}\right)} \qquad (3\text{-}16)$$

This off-current is largest for a signal level closest to V_{SS} and causes an error voltage (Δv_1) in the transmission of signal from v_{in} to V_A given by

$$\Delta v_1 = R_{on1} i_{off2}, \qquad (3\text{-}17)$$

where $R_{on1} = 1/g_{on1}$ is the effective on-resistance of the complementary MOSFET switch $S1$. The on-conductance g_{on1} is obtained from (3-10) as follows:

$$g_{on1} = g_{on1}\big|_{nMOSFET} + g_{on1}\big|_{pMOSFET} \qquad (3\text{-}18)$$

$$g_{on1}\big|_{nMOSFET} = 2\beta_n(V_{DD} - v_{in} - V_{tn}) \qquad v_{in} < V_{DD} - V_{tn} \qquad (3\text{-}19)$$

$$g_{on1}\big|_{pMOSFET} = 2\beta_p(v_{in} - V_{tp}) \qquad v_{in} > V_{tp} \qquad (3\text{-}20)$$

The error voltage (Δv_1) is a non-linear function of the input signal and causes offset and gain errors as well as distortion at the end of the cycle at the output. This error voltage is proportional to R_{on1} and i_{off2}. R_{on1} reaches a maximum at about mid-rail (assuming $\beta_n = \beta_p$) and i_{off2} rises as the signal gets closer to V_{SS}. Since Δv_1 is exponentially proportional to i_{off2}, the maximum value of Δv_1 occurs when i_{off2} reaches its maximum value, i.e $v_{in} = V_{SS}$. Assuming nMOSFETs used in $S1$ and $S2$ have the same W/L, the maximum error voltage is

$$\Delta v_1\Big|_{max} = \frac{\phi_t^2}{V_{DD} - V_t} 10^{-\frac{V_t}{S}}, \qquad (3\text{-}21)$$

where ϕ_t is the thermal voltage (kT/q = 25 mV @ room temperature). This error voltage is independent of device size and is determined solely by the process technology parameters and the thermal voltage. For example, in a 1 V process with a threshold voltage of 200 mV and a subthreshold swing of 100 mV/decade the maximum error voltage Δv_1 is about 7.8 μV.

A required dynamic range implies an upper limit on the error voltage, and from (3-21) one can find the minimum required threshold voltage. In the same way, for a given dynamic range and R_{on} the maximum tolerable i_{off} can be found. For example, a 100 dB *SNR* with a power supply of 1 V, and an on-resistance of 10 kΩ requires an off-current of less than 1 nA.

Switch $S4$ is biased at mid-rail (analog ground and virtual ground); thus, ideally there is no potential across this switch and leakage off-current through it is zero. However, due to non-idealities (finite opamp gain, etc.) there will be some voltage across switch $S4$. Since this switch is biased at mid-rail, the subthreshold leakage is reduced by two different actions; threshold increase due to body effect, and negative gate to source voltage. The subthreshold leakage current will be

$$i_{off4} = I_{D0}\frac{W}{L} 10^{-\left(\frac{V_{DD}/2 + V_t}{S}\right)}. \qquad (3\text{-}22)$$

For some typical values W/L = 10, I_{D0} = 100 nA, and V_{DD} = 1 V, a device with V_t = 180 mV and S = 90 mV/decade will have a leakage off-current of about 0.1 pA, which is very small and comparable to junction leakage.

Non-Overlapping Period:

The equivalent circuit of the SC integrator during the non-overlapping period is shown in Figure 3.9. As discussed in the previous section, the leakage off-currents through $S3$ and $S4$ are negligible.

In this circuit, C_T and C_B are the parasitic capacitances from the top and bottom plate of

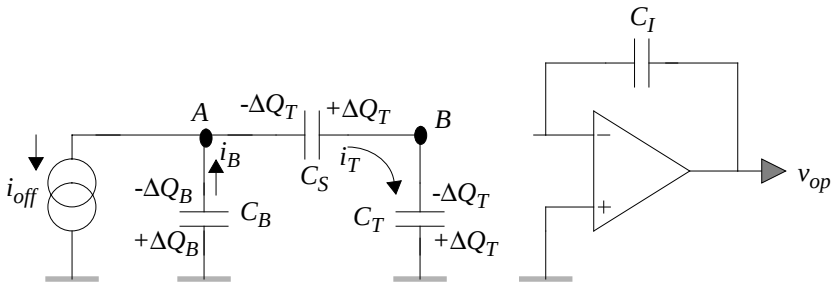


Figure 3.9: Equivalent circuit of Figure 3.7 during non-overlapping period

capacitor C_S to ground. The sum of leakage currents through $S1$ and $S2$ is called i_{off}, which is provided by i_T and i_B.

These leakage currents cause a change in charge across each capacitor as shown in the above figure. The error charge ΔQ_B across C_B causes no net error at the output (this is a stray insensitive configuration), because during ϕ_2 node A is shorted to analog ground and ΔQ_B is dumped to ground. The error charges ΔQ_T on capacitors C_S and C_T have different polarities (during ϕ_2) and as such cause no net error at the output.

During ϕ_2:

During ϕ_2 the SC integrator has an equivalent circuit as shown in Figure 3.10. At steady state, node B will be at the virtual ground potential (similar to the negative input of the opamp). Thus, leakage i_{off3} would be negligible. However, at the beginning of ϕ_2, the voltage at node B is changed suddenly from analog ground to $-v_{in}$. This can cause switch $S3$ to become leaky (for v_{in} close to V_{DD} the source of $S3$ will fall to V_{SS} resulting in $v_{GS} = 0$). Any charge lost by $S3$ will cause an error voltage (Δv_2) at the output given by

$$\Delta v_2 = \frac{1}{C_S}\int_0^{\delta t} i_{off3}\,dt, \qquad (3\text{-}23)$$

where δt is the time taken for the opamp to force V_B back to virtual ground.

For example if $C = 1$ pF and $\delta t = 5$ ns, an average leakage current i_{off} of 1 nA causes an error voltage of $\Delta V_2 = 5$ μV.

Another source of error during this phase is due to leakage current i_{off1}. Ideally, at the end

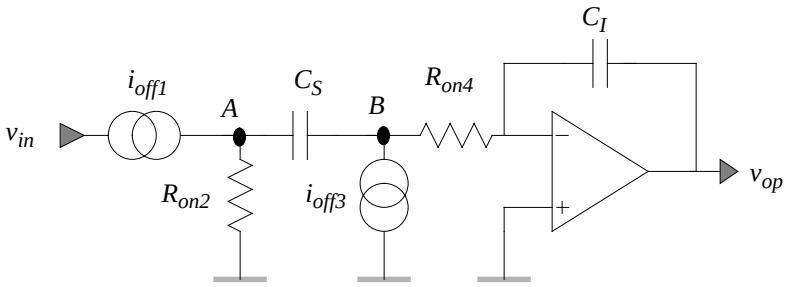


Figure 3.10: Equivalent circuit of Figure 3.7 during ϕ_2

of ϕ_2 node A must be at the analog ground potential. Leakage current i_{off1} and on-resistance R_{on2} cause an error voltage on node A which is given by

$$\Delta v_3 = i_{off1} R_{on2} \qquad (3\text{-}24)$$

Assuming the input voltage is close to V_{SS} and nMOSFET transistors in $S1$ and $S2$ have the same W/L, the error voltage is

$$\Delta v_3 = \frac{\phi_t^2}{(V_{DD}/2)-V_t} 10^{-\frac{V_t + v_{in}}{S}} . \qquad (3\text{-}25)$$

Again, maximum error occurs for v_{in} close to V_{SS} or V_{DD}. The maximum error caused during this phase (ϕ_2) is larger than the maximum error caused during ϕ_1, (3-21), because of the higher on-resistance in (3-24).

Summary

Low-V_t MOSFETs are leaky and limit the accuracy of SC circuits. The error caused during sampling is process dependent. For a 1 V process with a threshold voltage of 100 mV and a subthreshold swing of 100 mV, the sampling error is 156 μV which limits the accuracy to about 76 dB.

3.4 Series Transmission Gate and Composite Switch

As described in the previous section, subthreshold off-current through analog switches implemented with low threshold voltage MOSFETs introduces errors in SC circuits and reduces the dynamic range of the analog circuit.

A method of reducing the off-current is by limiting the signal swing. If the signal swing is reduced by ΔV from each rail, the subthreshold off-current (3-11) will be reduced by $\Delta V/S$ decades. Notice that for a $\Delta V = 200$ mV (which may be required for drain-source saturation voltage in the amplifier) and $S = 90$ mV/decade, the off-current is reduced by more than 100 times.

Measurements of i_{DS} vs. v_{GS} for a $W/L = 20\mu m/0.5\mu m$ nMOSFET with a threshold voltage of 130 mV are shown in Figure 3.11 for two different values of $v_{SB} = 0$ and 0.2 V. The drain to source voltage is set to 0.1 V in both measurements. Note that the

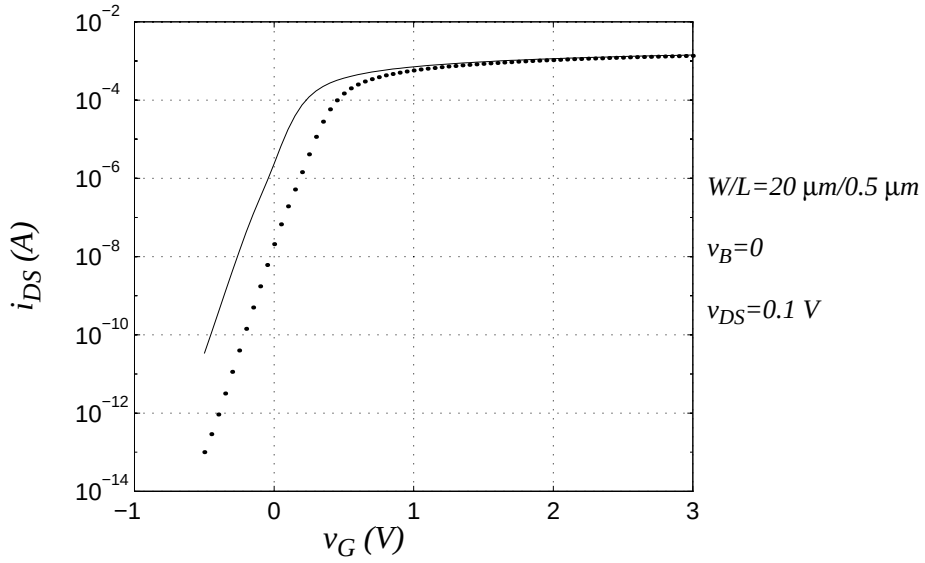


Figure 3.11: Measured i_{DS} vs. v_G for an nMOSFET with V_t=*130* mV and v_S=*0* (solid line) and v_S=*0.2* V (dotted line)

leakage off-current (i_{DS} at $V_G = 0$) is reduced from 2.38 μAto 20 nA by applying a negative gate-to-source voltage of 200 mV (i.e., limiting the signal swing).

Another way of reducing the subthreshold off-current is by adjusting V_t through back bias. A major problem with low-V_t MOSFET transistors is the threshold voltage variation due to processing errors (about ±100 mV) [Mizuno94] and temperature fluctuation (about −1.25 mV/°C). These can have a compounding effect and increase the off-current drastically. A technique of setting the V_t to a constant value, by adjusting the substrate

voltage, has been discussed in section 2.2.2.

In low-voltage design we can not afford to limit the signal swing by more than $150 – 200$ mV, the minimum required drain-to-source saturation voltage in the amplifier. If the threshold voltage is very low, limiting the signal swing may not decrease the off-current enough and other techniques ought to be exploited.

3.4.1 Series Transmission Gate Switch

In section 3.3, it was shown that in a stray insensitive SC circuit "off" switches have one side connected to analog/virtual ground (either directly or through another switch). An nMOSFET switch during the off-phase is shown in Figure 3.12a.

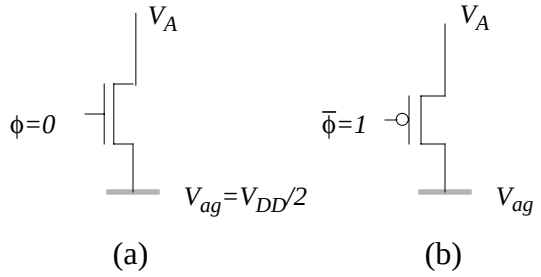


Figure 3.12: Turned-off (a) nMOSFET and (b) pMOSFET switches

For a $V_A > V_{DD}/2$ the subthreshold leakage off-current through the nMOSFET switch is low because of the negative gate to source voltage and an increase in V_t due to back bias. The i_{off} current is,

$$i_{off} = I_{D0}\frac{W}{L}10^{-P} \qquad (3\text{-}26)$$

where

$$P = \frac{V_{DD}/2 + V_t}{S}. \qquad (3\text{-}27)$$

However, as voltage V_A drops below $V_{DD}/2$, subthreshold leakage increases exponentially and reaches a maximum for $V_A = V_{SS}$. In this case the exponent ($P = V_t/S$) is small for low-V_t devices and results in a large off-current.

A turned-off pMOSFET switch (Figure 3.12b) has the opposite behavior; the off-current is

low for V_A below $V_{DD}/2$ and the largest off-current flows for $V_A = V_{DD}$.

A very low leakage switch (with one side tied to analog ground), is obtained by a series transmission gate switch as shown in Figure 3.13. The maximum subthreshold leakage off-current through this switch is similar to an nMOSFET switch with $V_A = V_{DD}/2$, as analyzed previously.

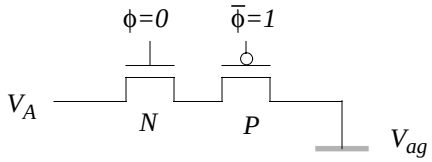


Figure 3.13: A series transmission gate switch

Figure 3.14 illustrates the simulated subthreshold leakage current through an nMOSFET and a series transmission gate (STG) switch. Threshold voltages of MOSFETs are set to 110 mV and transistor sizes are $(W/L)_p = 2(W/L)_n = 10$.

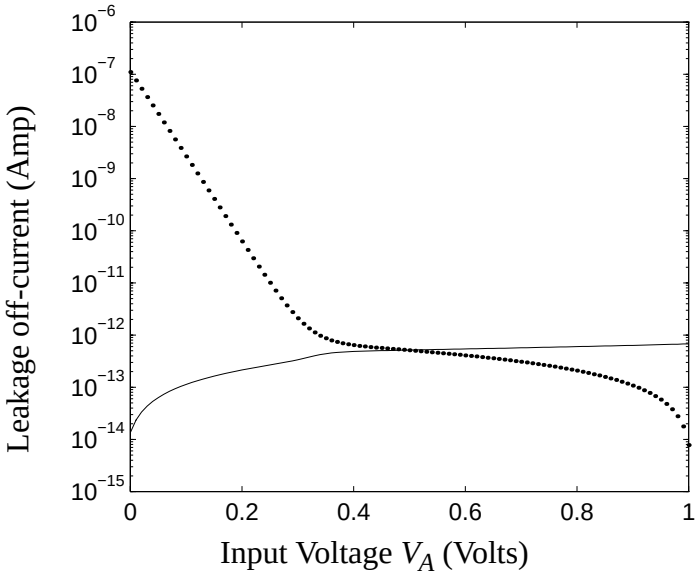


Figure 3.14: Leakage off-current through an nMOSFET switch (dotted line) and a STG switch (solid line) versus input voltage

The leakage off-current through the STG switch is very low (~1 pA) while a low-V_t nMOSFET has a relatively high leakage off-current (~0.1 μA) for low input voltages.

The on-conductance of the series transmission gate switch is

$$g_{on} = \frac{2\beta_n(V_{DD} - V_{tn} - V_{in})\beta_p(V_{in} - V_{tp})}{\beta_n(V_{DD} - V_{tn} - V_{in}) + \beta_p(V_{in} - V_{tp})} . \qquad (3\text{-}28)$$

For $\beta_n = \beta_p$ and $V_{tn} = V_{tp} = V_t$, the maximum on-conductance for a STG occurs at $V_{DD}/2$. This is exactly where all the switches to analog ground are operating. The maximum on-conductance of a series transmission gate is

$$g_{on(max)}\Big|_{STG} = \beta\left(\frac{V_{DD}}{2} - V_t\right), \qquad (3\text{-}29)$$

which is lower than the on-conductance of a simple nMOSFET by a factor of *2*. Simulation for on-conductance, Figure 3.15, confirms the validity of the above analysis.

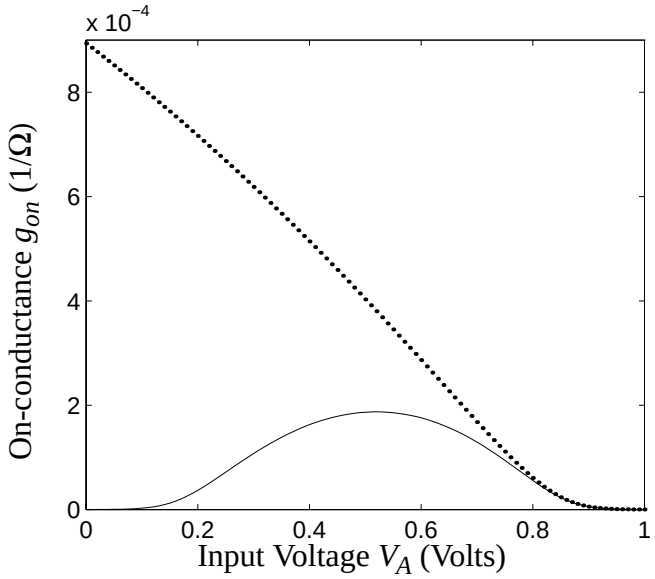


Figure 3.15: On-conductance of the nMOSFET (dotted-line) and STG switch (solid-line) versus input signal

A drawback of the series transmission gate switch is the limited input signal swing. This switch cannot conduct signals that are within a V_t of the supply rails. In the next section, a solution to this problem is presented.

3.4.2 Composite Switch

In a multi-threshold process, the high-V_t (threshold adjusted) transistors can be used in a

parallel transmission gate (TG) configuration along with the series transmission gate switch to handle rail-to-rail switch capability. The composite switch is shown in Figure 3.16 (the V_t adjusted MOSFETs are shown with bold lines in the channels).

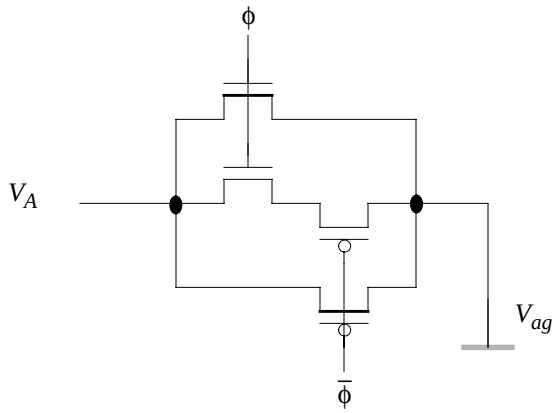


Figure 3.16: A composite switch

The simulated on-conductance of the composite switch is shown in Figure 3.17. In this

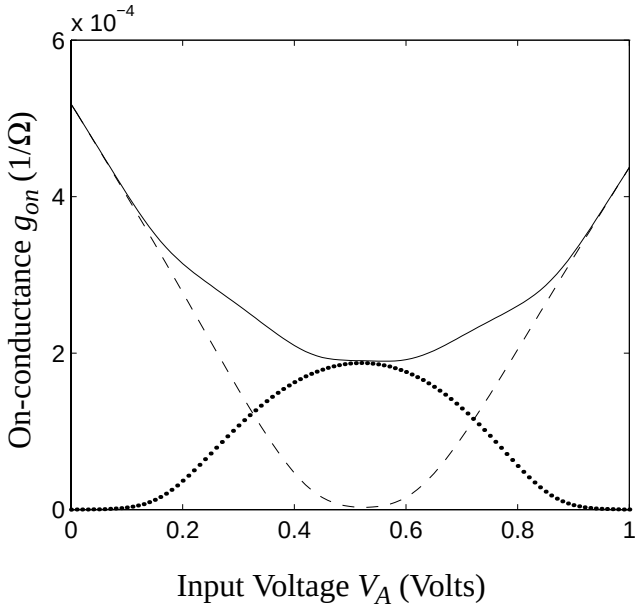


Figure 3.17: Simulated on-conductance for high-V_t TG switch (dashed-line), low-Vt series transmission gate switch (dotted-line), and the composite switch (solid-line) versus input signal

configuration, the high-V_t parallel transmission gate conducts well when the signal is

close to the rails, and the low-V_t series transmission gate conducts well when the signal is at mid-rail. The on-conductance and leakage through this composite switch is simulated along with simple high-V_t and low-V_t parallel transmission gates and all three are illustrated in Figure 3.18 and Figure 3.19.

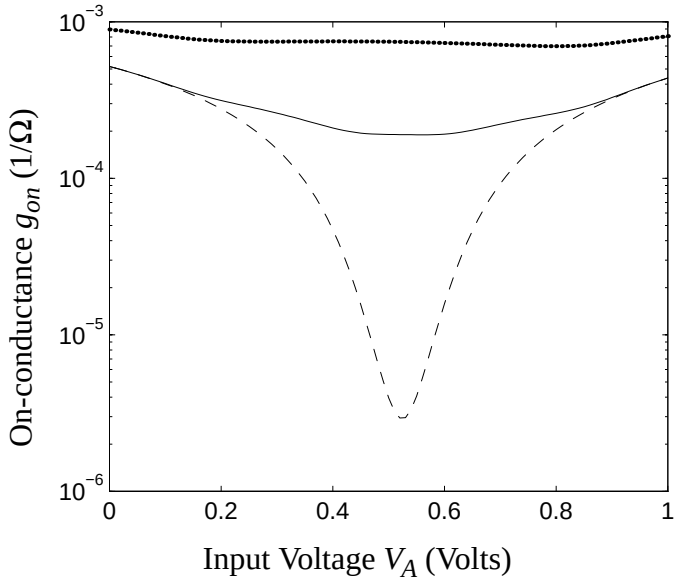


Figure 3.18: On-conductance for high-V_t TG switch (dashed-line), low-V_t TG switch (dotted-line), and the composite switch (solid-line) versus input signal

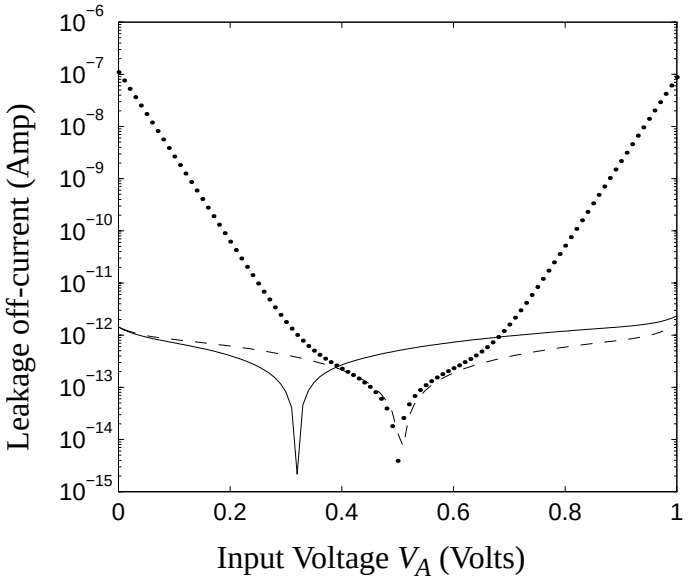


Figure 3.19: Leakage current for high-V_t TG switch (dashed-line), low-V_t TG switch (dotted-line), and the composite switch (solid-line) versus input signal

Summary

Subthreshold off-current through MOSFET switches is reduced by (1) limiting the signal swing, (2) adjusting the V_t by back bias, and (3) using low-leakage series transmission gate and composite switch.

3.5 A 2.25 V Second-Order Sigma-Delta Modulator

This 2.25 V modulator is based on an existing 3.3 V SC oversampled double integration sigma-delta modulator [Howlett93] in BATMOS, Northern Telecom's 0.8 µm BiCMOS process [Hadaway91]. The 3.3 V design operates at 2 MHz and achieves 94 dB SNDR for an oversampling ratio of 256. Simulations indicated that the characteristic of the amplifier and comparator blocks used in this modulator are not significantly degraded at 2.25 V. The modulator performance was limited by the increase in switch resistance at 2.25 V. This has been remedied by using short-channel MOSFET switches. At 2.25 V the SNDR of the original design drops to 86 dB. However, the modified design using 0.6 µm channel length MOSFET switches achieves 92 dB of SNDR at 2.25 V.

Unfortunately, a two-stage BiCMOS opamp is used in this modulator which can not operate below 2.25 V. Thus, in-circuit low-voltage performance of these short-channel switches can not be verified below 2.25 V.

The block diagram of this modulator is similar to the one in [Boser88] and it is a differential SC design, implemented using two single-ended opamps.

3.5.1 Short-Channel MOSFETs

Medici, a 2-D device simulator, was used to find the minimum achievable channel length for short-channel MOSFETs with acceptable punchthrough current in BATMOS. Measurements were also carried out on different sizes of short-channel MOSFETs to verify the simulation results and MOSFETs with channel length of 0.6 µm were found reliable as low-voltage switches.

Characteristics of different short-channel MOSFETs (all with $W/L = 10\ \mu m / 0.6\ \mu m$) were measured for both nMOSFET and pMOSFET transistors. At supply voltage of 3 V, the on-resistances of switches biased at mid-rail ($v_{SB} = 1.5$ V and $v_{DB} = 1.6$ V) were measured. Results are shown in Table 3.1.

Transistor Type	R_{on}		Reduction
	L=0.8 μm	*L=0.6* μm	
nMOSFET	1.3 K	0.709 K	45%
pMOSFET	5.8 K	3.2 K	44%

Table 3.1: On-resistance of switches with W=10μm

Further measurements of the 0.6 μm nMOSFET switch show that R_{on} of 1.2 kΩ is achieved with a supply voltage of 2.1 V.

Figure 3.20 illustrates the i_{DS} versus v_{GS} characteristic of an nMOSFET with 0.6 μm channel length under two different v_{DS} conditions.

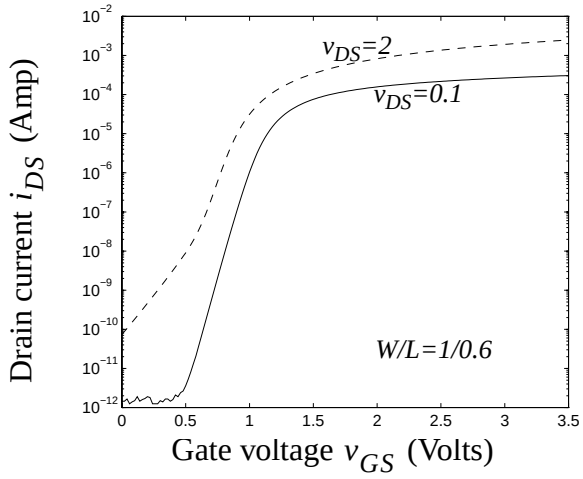


Figure 3.20: Drain current versus gate voltage for a 0.6 μm nMOSFET with v_{DS}=*0.1* V (solid line) and v_{DS}=*2* V (dashed line)

Since the turn-off leakage (i_{DS} at $v_G = 0$) is of prime importance to us, i_{DS} versus v_{DS} is also measured for the same device (a 0.6 μm nMOSFET), with different back bias voltages. It is seen (Figure 3.21) that extremely low current leakage is obtained by setting the back bias to 0.5 V. Both Figure 3.20 and Figure 3.21 show current per micron of width of the transistor.

Measurements of a 0.6 μm pMOSFET device gave similar results.

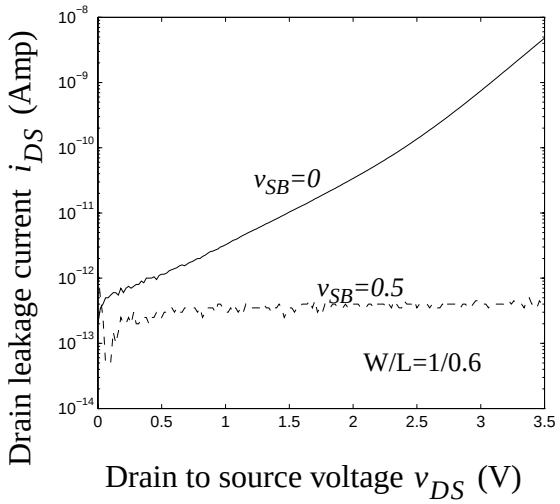


Figure 3.21: Drain off-current ($v_G=0$) versus drain to source voltage for a 0.6 μm nMOSFET with $v_{SB}=0$ (solid line) and $v_{SB}=0.5$ V (dashed line)

3.5.2 Short-Channel MOSFETs Layout Issues

Channel length variation due to processing errors (lithography and etching) is very critical for short-channel MOSFETs and must be minimized. Some layout techniques that help to reduce the 3σ (inter die and intra wafer) channel length variations are as follows.

- Place the structure of interest close to the center of the die; thereby ensuring the best possible optical and focus performance.
- Maintain symmetry around the structure of interest to ensure similar resist flow/ planarization from all directions [Gehm92].
- Keep all the underlying steps (e.g., device well edges) as far away from the area of interest as is feasible.

3.5.3 Measured SNDR

The second-order ΣΔ modulator using short-channel MOSFET switches was fabricated in BATMOS and the measured SNDR is shown in Figure 3.22. Zero dB input level corresponds to a 1.5 V peak-to-peak signal. This modulator operates at 2.25 V and has a maximum SNDR of 92 dB for an oversampling ratio of 256. The SNDR of the original 3.3 V design drops to 86 dB at 2.25 V supply voltage.

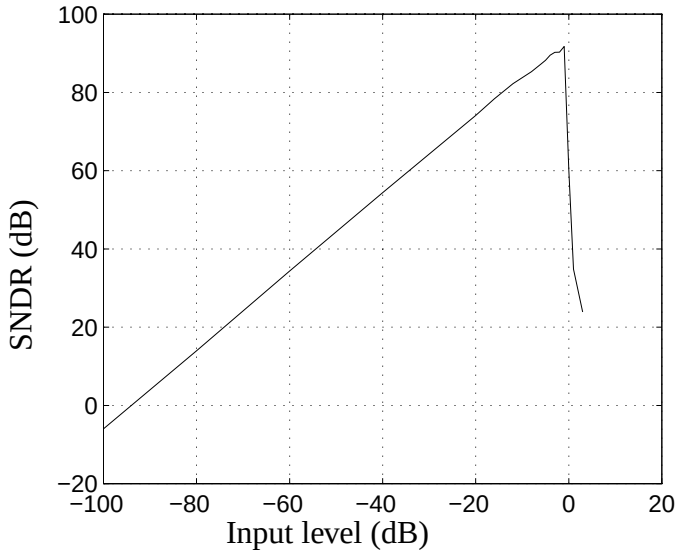


Figure 3.22: Measured ΣΔ modulator performance

3.6 A 1 V First-Order Sigma-Delta Modulator

In a low supply-voltage environment, fully differential circuits are preferred due to larger dynamic range, elimination of second harmonic distortions, and the tolerance to various common mode noises. This design was done at the early stages of process development and the CAD tools had very limited capability. Thus, a simple single-ended first-order SC ΣΔ modulator was chosen as a benchmark to demonstrate the feasibility of using natural MOSFETs for 1 V SC design. To our knowledge, this is the first reported SC ΣΔ modulator operating at a power supply voltage of 1 ± 0.1 V [Bazarjani95a].

The architecture of a first-order SC ΣΔ modulator is shown in Figure 3.23. It consists of a discrete integrator and a two level quantizer in a negative feedback loop.

This modulator was implemented in a 0.5 μm n+/p+ dual poly gate CMOS process using natural threshold voltage MOSFETs. The natural transistors in this process have threshold voltages of about 200 mV which is suitable for 1 V circuits. In the following, design of 1V opamp, comparator and switches used in this circuit is discussed along with some simulation and measured results.

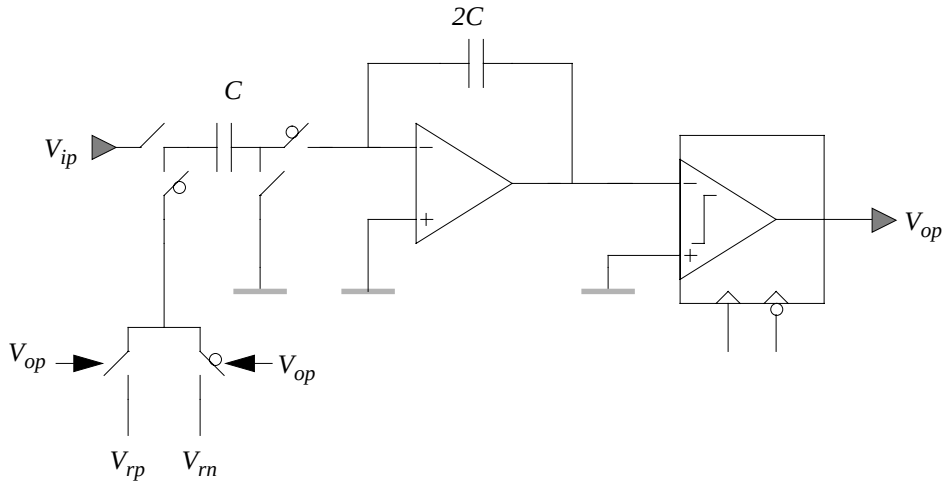


Figure 3.23: A first-order SC ΣΔ modulator

3.6.1 1 V opamp

Lowering the power supply voltage directly reduces the dynamic range and consequently the accuracy of the analog circuitry. Thus rail-to-rail signal swing is desired to maximize the dynamic range. In a SC circuit, signals at the inputs of the opamp are at analog ground, thus no input signal swing is required. However, the output(s) of the opamp must provide the largest possible signal swing. Each transistor at the output stage requires a certain voltage to be kept in saturation ($v_{DS} > v_{GS} - V_t$) which limits the output signal swing. Therefore, cascode structures are avoided at the output stage of the amplifier. A two-stage pole-splitting opamp, Figure 3.24, provides enough gain and maximum signal swing at the output of the amplifier.

In this opamp, the bias current I_{bias} is set to $10\ \mu A$ and the compensation capacitor C_c is $2\ pF$. The dimensions of all the MOSFETs are listed in Table 3.2.

MOSFET	*N1*	*N2*	*N3*	*N4*	*P1*	*P2*	*P3*	*P4*	*P5*	*P6*
W(μm)	*10*	*10*	*10*	*2*	*120*	*120*	*60*	*60*	*4*	*60*
L(μm)	*1*	*1*	*1*	*1*	*0.5*	*0.5*	*1*	*1*	*1*	*1*

Table 3.2: Dimension of MOSFETs used in the opamp of Figure 3.24

This opamp was simulated in Eldo [Eldo] using MISNAN, a physically based MOSFET

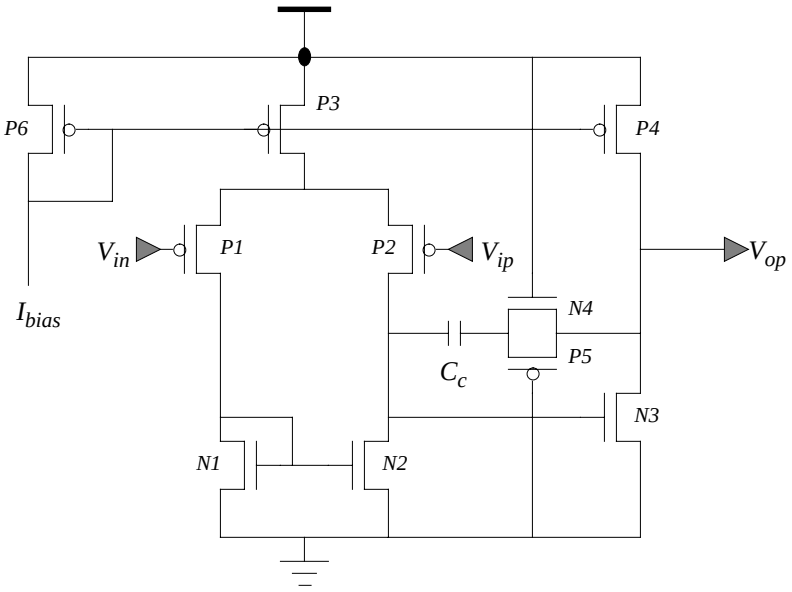


Figure 3.24: A two-stage pole-splitting opamp

model [Boothroyd92]. The device model parameters were obtained from [Tarr95], where parameters are estimated using SUPREM3 and MINIMOS5 simulations.

The overall simulated opamp performance at 1 V power supply voltage and 1 pF load is summarized in Table 3.3.

Parameter	Result
DC gain	60 dB
Unity gain bandwidth	40 MHz
Phase Margin	60°
Slew rate	10 V/μs
Output range	0.5 V
Power Dissipation	30 μW

Table 3.3: Simulated opamp performance for a 1 pF load capacitance

3.6.2 Comparator

In ΣΔ modulators the performance of the comparator is not critical. A class AB comparator similar to [Boser88] is used here. Figure 3.25 illustrates the schematic of this

comparator. Simulations indicate a delay of 6 ns is achieved at a 1V power supply for a 1 pF load capacitance.

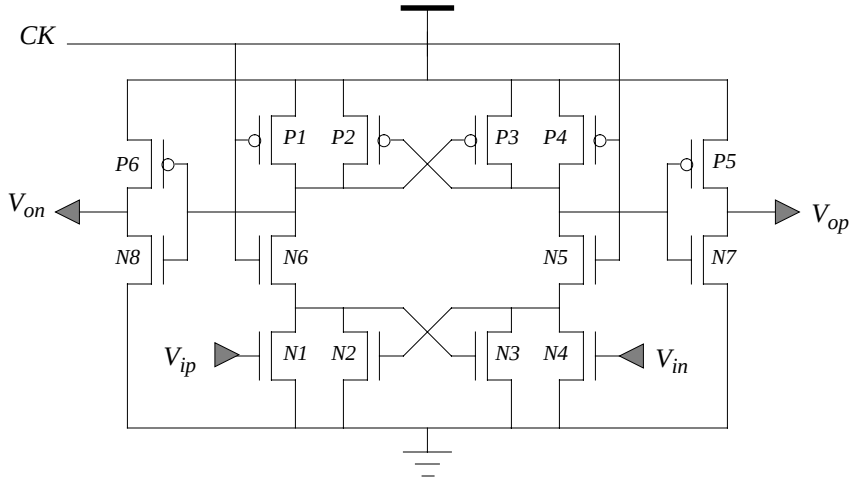


Figure 3.25: Schematic of the comparator

All the transistors sizes for this comparator are listed in Table 3.4.

MOSFET	*N1*	*N2*	*N3*	*N4*	*N5*	*N6*	*N7*	*N8*	*P1*	*P2*	*P3*	*P4*	*P5*	*P6*
W (μm)	*10*	*10*	*10*	*10*	*5*	*5*	*10*	*10*	*3*	*30*	*30*	*3*	*10*	*10*
L (μm)	*2*	*2*	*2*	*2*	*0.5*	*0.5*	*0.5*	*0.5*	*0.8*	*2*	*2*	*0.8*	*0.5*	*0.5*

Table 3.4: Transistor sizes for the comparator

3.6.3 Switches

As previously discussed, a good analog switch will exhibit a low on-resistance when turned on and a very low off-current when turned off. In this SC design, switches are implemented with complementary low-V_t natural MOSFETs. A transmission gate switch with $W/L = 1.5\ \mu m / 0.5\ \mu m$ for both nMOSFET and pMOSFET was simulated in Eldo at 1 V supply voltage. Figure 3.26 shows the on-resistance of the transmission gate switch as a function of the input signal level.

A worst case on-resistance of 12 kΩ is obtained for a signal level of 790 mV. In the SC circuit of Figure 3.23 two of these switches and the sampling capacitor constitute an RC circuit. For the sampling capacitor of 1 pF the time constant τ will be 24 ns. Settling to

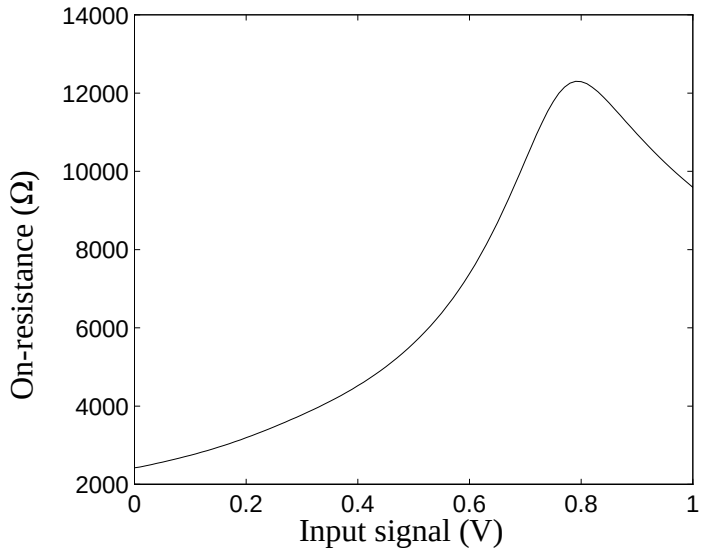


Figure 3.26: Simulated transmission gate switch resistance as a function of input signal

0.1% of the full scale requires 168 ns (7τ) allowing an upper limit of 3 MHz operation for this switch.

The subthreshold off-current of these switches can be calculated from the simplified equation of (3-11). In this process, typical values of I_{D0} and S for an nMOSFET are 100 nA and 86 mV/decade respectively.The W/L = 1.5 µm /0.5 µm nMOSFET switch will have less than 1 nA subthreshold leakage current for a signal at V_{SS}. However, the minimum signal in this ΣΔ modulator is about 0.25 V. Therefore, the maximum leakage current through the above nMOSFET switch (when the signal is 0.25 V) is less than 10 pA. Simulation of the leakage current through a natural nMOSFET transistor is shown in Figure 3.27 and the results correlate well with the above analysis.

3.6.4 Measured Results for the 1 V Sigma-Delta Modulator

The modulator was fabricated in a 0.5 µm n^+/p^+ dual poly gate CMOS process with a linear poly-poly capacitor and triple level metal CMOS process. The chip die photograph is shown in Figure 3.28.

The modulator was tested at a clock frequency of 1 MHz using a 1 V supply voltage and reference voltages of ±0.25 V (with respect to analog ground, 0.5 V). The output

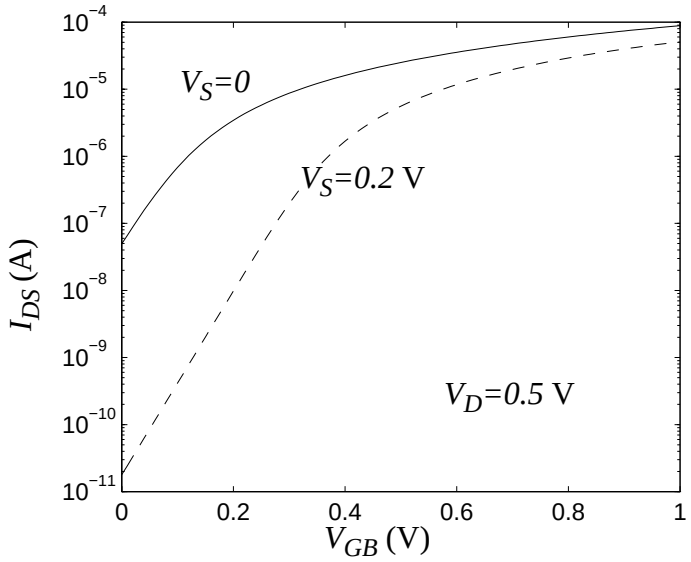


Figure 3.27: Simulated off-current for the nMOSFET switch

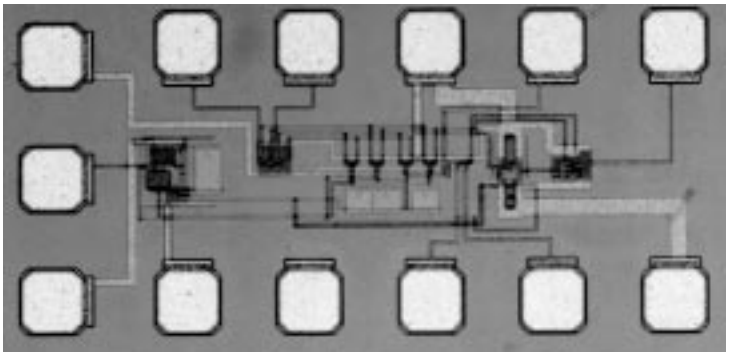


Figure 3.28: Chip die microphotograph

spectrum for an input signal of 4 kHz and 420 mVpp is shown in Figure 3.29.

The output bit-stream was captured by a logic analyzer and *131072*-point FFT was performed in Matlab [Matlab]. For an oversampling of 128, a SNDR of 54 dB is obtained.

3.7 Summary

In this chapter, a process technology and two circuit techniques for achieving low-V_t MOSFETs in current CMOS processes were presented. Effects of low-V_t subthreshold

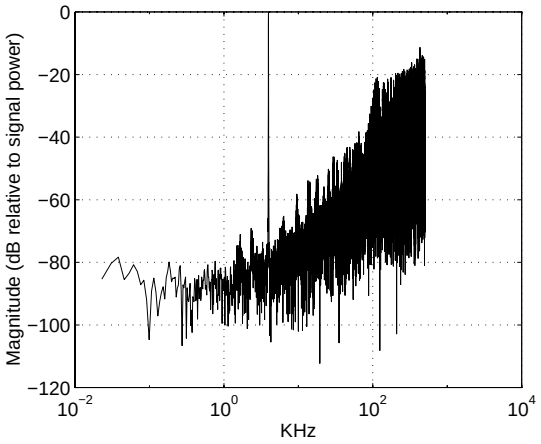


Figure 3.29: Measured spectrum (Vip = 420 mVpp)

leakage currents to the precision of analog SC circuits were analyzed. It was shown that off-current leakage through MOSFET switches reduces the accuracy of SC circuits.

Methods of reducing the leakage current through analog switches were discussed and two very low leakage analog switches suitable for SC circuits were proposed.

Finally, two experimental low-voltage voice-band ΣΔ modulators using low-V_t MOSFETs were described. In the first design, an existing 3.3 V ΣΔ modulator designed in 0.8 μm BiCMOS process was modified using “short-channel MOSFET” as switches and the new design operates at 2.25 V. The second design is a 1 V SC ΣΔ modulator using low-V_t natural MOSFETs in a 0.5 μm CMOS technology.

Chapter 4

High-Speed SC Fourth-Order Bandpass Sigma-Delta Modulators

In Chapter 2, a method of transfer function design for a bandpass ΣΔ modulator from a lowpass ΣΔ modulator using a $z^{-1} \rightarrow -z^{-2}$ change of variable was discussed. It was also mentioned that the stability and SNR characteristics of the resulting bandpass ΣΔ modulator are identical to those of the lowpass prototype.

This chapter starts by introducing a z-domain architecture for a fourth-order bandpass ΣΔ modulator. This modulator is obtained by performing the above mapping to a second-order (double integration) lowpass ΣΔ modulator. The resulting bandpass modulator is a double-resonator ΣΔ modulator. In the sampled-data domain, an efficient method of implementing resonators uses two delay cells in a negative feedback loop. Switched-capacitor delay circuits are considered next and a double-sampled SC delay cell is presented. The impacts of non-ideal circuit behaviors on the performance of a simple SC delay cell and the double-sampled SC delay circuit are analyzed. Then, two SC implementations of the fourth-order bandpass ΣΔ modulator—namely a simple SC structure and a double-sampled SC architecture—are presented along with Eldo simulation results. Finally, the design of both modulators in a 0.5 μm CMOS process is considered and measured results of the modulators are presented.

4.1 Modulator Architecture

The loop filter transfer function for a fourth-order bandpass ΣΔ modulator was derived in Chapter 2, and is

$$H_{bp4}(z) = \frac{z^{-4} + 2z^{-2}}{(1 + z^{-2})^2} \quad . \qquad (4\text{-}1)$$

Assuming the quantization error e to be white noise and the comparator gain to be unity, the output-input transfer characteristic of this modulator is

$$Y(z) = z^{-4}X(z) + (1 + z^{-2})^2 E(z) \quad . \qquad (4\text{-}2)$$

Lowpass ΣΔ modulators are usually implemented as a cascade of integrators. A natural choice for bandpass modulators seems to be a cascade of resonators. One such architecture is shown in Figure 4.1. The quantizer is typically implemented using a 1-bit comparator

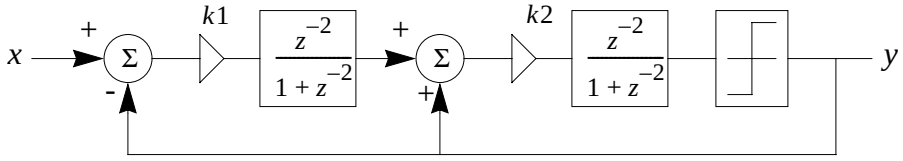


Figure 4.1: A fourth-order double resonator bandpass ΣΔ modulator

with two levels at $\pm V_{ref}$. The z-domain transfer function of this modulator is

$$[1 + (2 - k2)z^{-2} + (1 + k1k2 - k2)z^{-4}]Y(z) = k1k2z^{-4}X(z) + (1 + z^{-2})^2 E(z) \quad . \qquad (4\text{-}3)$$

Comparing equations (4-2) and (4-3), the values of $k1$ and $k2$ are found to be 0.5 and 2 respectively. Since the second resonator is followed by a high gain quantizer, the coefficient $k2$ is irrelevant [Boser88] and is set to 0.5, as is the coefficient of the first stage. This architecture is a direct map of the lowpass ΣΔ modulator in [Boser88] to bandpass by transforming integrators to resonators. Analogous to the lowpass prototype, the signal swings at the output of the resonators are almost within the full scale input range, $\pm V_{ref}$. Figure 4.2 illustrates the histograms of the signal levels at the output of the resonators for an input signal of 6 dB below full scale (i.e., the peak-to-peak signal amplitude is V_{ref}). We use statistical techniques to characterize signal swings, because sigma-delta modulators produce pseudo-random outputs.

The noise transfer function of this modulator has a pair of complex conjugate zeros

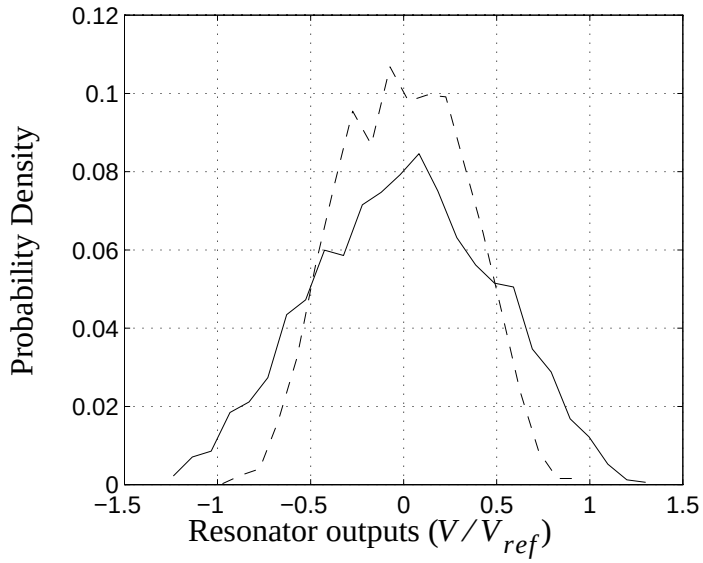


Figure 4.2: Histograms of output levels for the first (solid line) and the second (dashed line) resonator for a -6 dB tone input

located at $z = \pm j$. In the frequency domain, this corresponds to notches around $(2n + 1) f_s/4$, where $n = 0, 1, 2$, ..., and f_s is the sampling frequency. The z-domain simulated output spectrum of this modulator is shown in Figure 4.3.

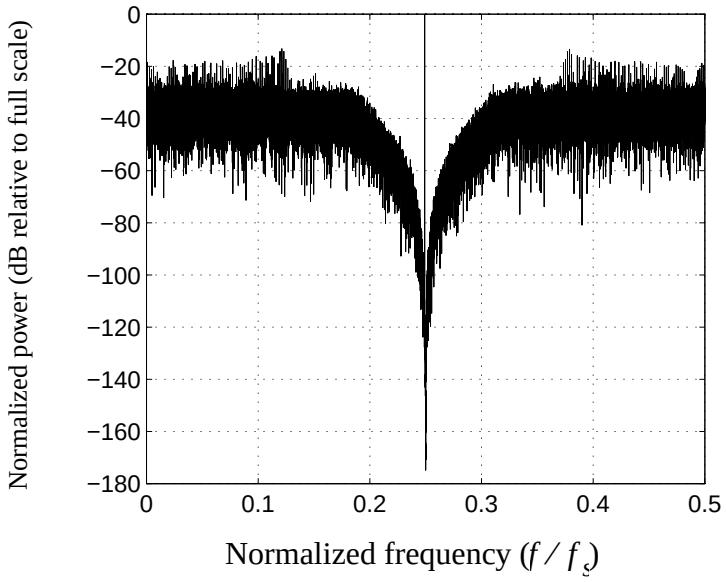


Figure 4.3: Simulated output spectrum of the fourth-order bandpass ΣΔ modulator in Figure 4.1 for a sinusoidal input.

The noise shaping is clearly seen at around a quarter of the sampling frequency. As we discussed in Chapter 2, this fourth-order modulator is guaranteed to be stable because of

the stability of the second-order lowpass prototype.

The $f_s/4$ resonator can be implemented in several different ways using SC techniques. In [Singor94], resonators are implemented using Lossless Discrete Integrators (LDI) and Forward-Euler (FE) integrators. Another approach is to use two delay cells in a negative feedback loop [Longo93], as shown in Figure 4.4.

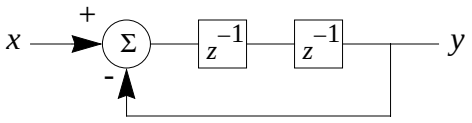


Figure 4.4: Resonator using delay cells

The latter design is chosen here for SC implementation because: (1) it operates at a higher speed [Singor94], (2) an SC delay circuit is immune to capacitor non-linearity [Bazarjani95c] which is useful when a SC circuit is implemented by weakly non-linear MOSFET capacitors and (3) a variation of this architecture can be implemented using a high-speed bipolar sample-and-hold circuit [Varelas96].

4.2 Half Delay SC Circuits

There are many SC amplifier designs that contain a half delay in their operation [Gregorian86]. Some involve techniques to reduce DC offset and $1/f$ noise [Gregorian81], others utilize gain-enhancing methods to compensate for low opamp DC gain [Haug84].

Here, the delay cell is intended to be used in a bandpass ΣΔ modulator, thus, offset and $1/f$ noise do not affect the performance of the circuit. Moreover, sampled-data ΣΔ modulators typically require moderate opamp DC gain (opamp DC gain must be comparable to the oversampling ratio) and, as such, a gain-compensation scheme may not be needed. A simple SC amplifier is used for speed considerations.

The circuit of a fully differential SC amplifier is shown in Figure 4.5a. A two-phase non-overlapping clock, as shown in Figure 4.5b, is required for the operation of this circuit. The output is delayed by a half-clock period and has a gain of C_S/C_H. Assuming infinite opamp DC gain and denoting the differential input and output by v_{od} and v_{id}, where

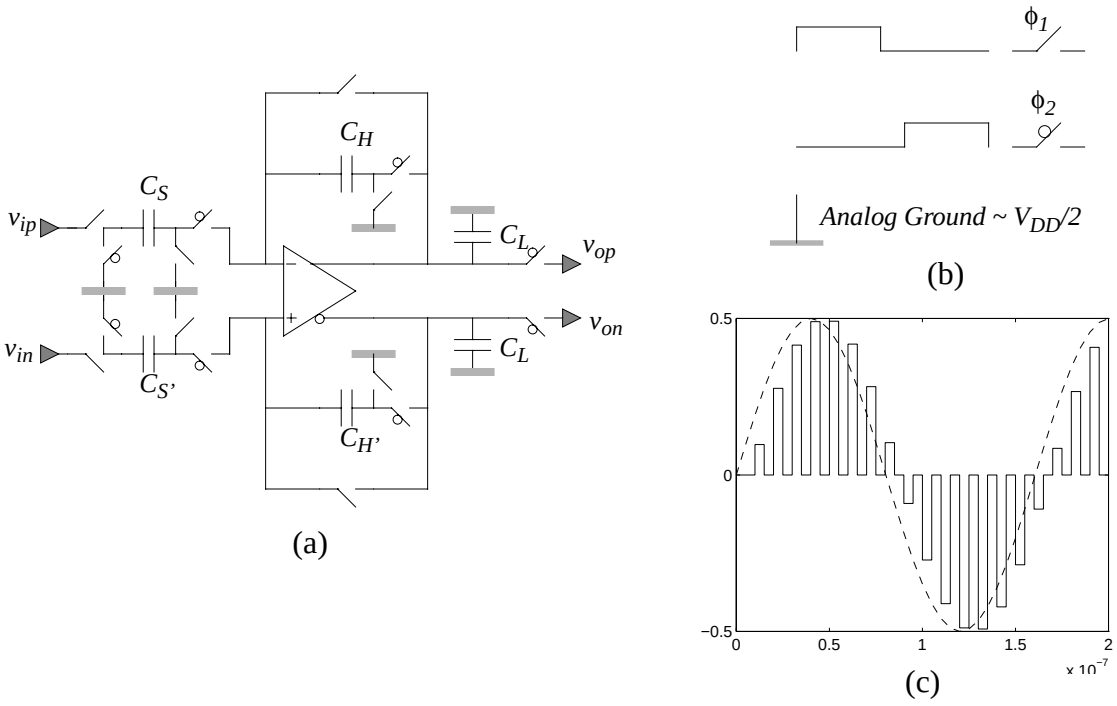


Figure 4.5: (a) A SC half delay gain stage, (b) 2-phase non-overlapping clock, (c) input (dashed line) and output (solid line) waveforms

$$v_{od} = v_{op} - v_{on} \quad \text{and} \quad v_{id} = v_{ip} - v_{in} \ , \tag{4-4}$$

the z-domain transfer function of this amplifier (output sampled during ϕ_2) is

$$\frac{V_{od}(z)}{V_{id}(z)} = H_{HD}(z) = \frac{C_S}{C_H} z^{-1/2} \ . \tag{4-5}$$

If the sampling capacitor, C_S, and the holding capacitor, C_H, are identical, the circuit is called a unity gain buffer or sample-and-hold circuit.

The ideal transfer function of the SC amplifier is affected by a number of non-ideal circuit behaviors. The impacts of finite opamp gain, incomplete settling, switch charge-injection, circuit noise, and capacitor mismatch on the performance of the half delay SC amplifier are analyzed in the following section.

Finite Opamp Gain Errors

Finite DC opamp gain (A) and a non-zero opamp input capacitance (C_{in}) introduce gain error in (4-5), as analyzed below. Figure 4.6 shows single-ended equivalent circuits of

Figure 4.5a during ϕ_1 and ϕ_2 phases.

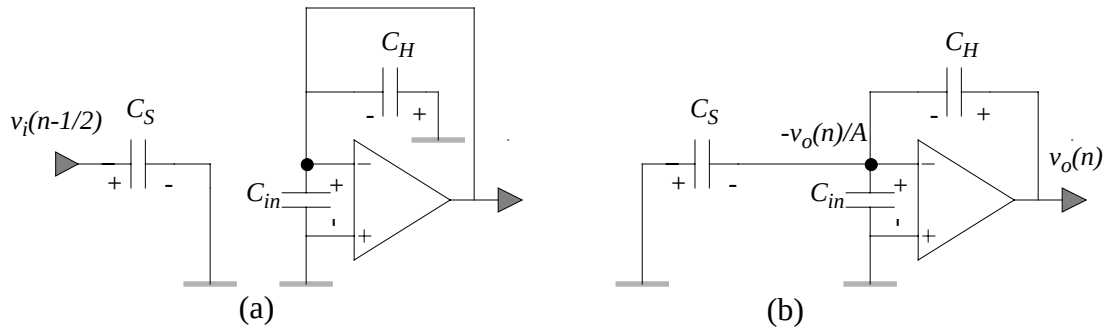


Figure 4.6: A single-ended equivalent circuit of Figure 4.5a during (a) ϕ_1 and (b) ϕ_2 phases

Charge conservation on capacitors C_S, C_H, and C_{in} before and after ϕ_2 yields the following difference equation:

$$C_S\left[v_i(n-1/2)-\frac{v_o(n)}{A}\right]-C_H\left[v_o(n)+\frac{v_o(n)}{A}\right] = C_{in}\frac{v_o(n)}{A} \qquad (4\text{-}6)$$

In the z-domain the actual transfer function of the fully differential SC amplifier becomes

$$H_{HD}(z) = \frac{V_{od}(z)}{V_{id}(z)} = \frac{C_S}{C_H}\cdot\frac{1}{1+\frac{1}{A\beta}}\cdot z^{-1/2}, \qquad (4\text{-}7)$$

where β is the feedback factor and is given by

$$\beta = \frac{C_H}{C_H+C_S+C_{in}}. \qquad (4\text{-}8)$$

Here, C_{in} represents the sum of all parasitic capacitances appearing at the input of the opamp, including opamp input capacitance. If $A\beta \gg 1$, the transfer function of (4-7) can be simplified to

$$H_{HD}(z) = \frac{C_S}{C_H}\left(1-\frac{1}{A\beta}\right)\cdot z^{-1/2} \qquad (4\text{-}9)$$

An opamp with 50 dB DC gain ($A \approx 300$) causes 1 % error in a sample-and-hold circuit

if the input capacitance C_{in} of opamp is comparable to C_S and C_H.

Settling Errors

Another source of error in the half delay circuit is due to incomplete settling. During the hold phase (ϕ_2), the opamp is connected in a negative feedback configuration and is modelled by Figure 4.7.

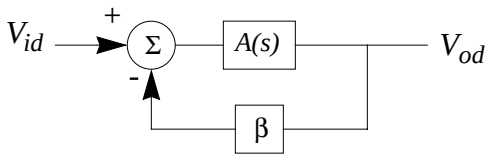


Figure 4.7: Opamp in the closed-loop configuration during ϕ_2

If the opamp is a single-stage topology with a gain of $A = \omega_u / s$, the closed-loop transfer function will be

$$\frac{V_{od}}{V_{id}}(s) = \frac{A(s)}{1 + \beta A(s)} = \frac{\omega_u}{s + \beta\omega_u} . \qquad (4\text{-}10)$$

Thus, the output of the SC half delay amplifier follows an exponential behavior as follows:

$$v_{od} = v_F(1 - e^{-t/\tau}) \qquad (4\text{-}11)$$

Here, v_F is the final output value and τ is the closed-loop time constant given by

$$\tau = \frac{1}{\beta\omega_u}, \qquad (4\text{-}12)$$

where ω_u is the open-loop unity gain frequency of the opamp. The hold time of the SC half delay circuit is about half a clock period. Therefore, the output cannot reach the exact final value and there will be a settling error. The required time constant to settle to α percent of the final value in a half clock period ($T_s/2$) is given by

$$\tau = \frac{T_s/2}{\ln(100/\alpha)} . \qquad (4\text{-}13)$$

For instance, settling to 0.1% of the final value requires the time constant to be

$\tau \leq (T_s / 13.8)$.

In the time constant equation (4-12), the unity gain frequency is determined by

$$\omega_u = \frac{g_m}{C_{TL}}, \qquad (4\text{-}14)$$

where g_m is the transconductance of the opamp and C_{TL} is the total load capacitance appearing at the opamp output during ϕ_2, which in the SC amplifier of Figure 4.5 is

$$C_{TL} = C_L + \frac{C_H(C_S + C_{in})}{C_H + (C_S + C_{in})}. \qquad (4\text{-}15)$$

C_L is the opamp load capacitance plus all the parasitic capacitances at the output of the opamp.

Switch Charge Injection Errors

A third source of error is due to charge injection from MOSFET switches. Consider a simple sample-and-hold circuit comprised of an nMOSFET switch and a holding capacitor C_H as shown in Figure 4.8.

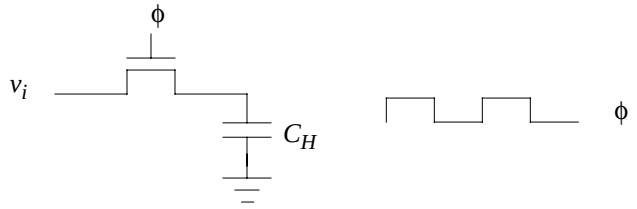


Figure 4.8: A simple SC sample-and-hold circuit

At the end of the sampling phase, $\phi = V_{DD}$, the holding capacitor reaches a voltage that is equal to the input voltage v_i (assuming the settling error is negligible). During the hold phase, $\phi = 0$, the clock voltage is dropped from V_{DD} to zero and ideally the voltage on the holding capacitor is held constant and equal to the value of the input voltage at the end of the sampling phase. However, the sampled voltage is disturbed due to channel charge injection and clock feedthrough when the nMOSFET switch is turned off. The inversion channel charge in a turned-on nMOSFET is given by

$$Q_{ch} = C_{ox}(WL)(v_{GS} - V_t) . \qquad (4\text{-}16)$$

When the transistor is turned off, this charge is released to drain, source and substrate. If the fall time of the clock is longer than the channel transit time ($\tau_0 = L^2/\mu_n(v_{GS} - V_t)$), the charge absorbed by the substrate is negligible. The charge partition between source and drain is a function of clock fall time and drain/ source capacitance. For a sharp clock edge, channel charge is divided equally between source and drain sides [Wegmann87].

The error introduced in the sample-and-hold circuit is

$$\Delta V = -\alpha \cdot \frac{C_{ox}(WL)(V_{DD} - v_i - V_t)}{C_H} \qquad (4\text{-}17)$$

where α is the percent of channel charge injected to the holding capacitor. This channel charge causes offset, gain error and distortion in the sample-and-hold circuit.

A method for eliminating the signal dependent charge injection is bottom plate sampling [Gregorian86], as illustrated in Figure 4.9. The channel charge associated with the

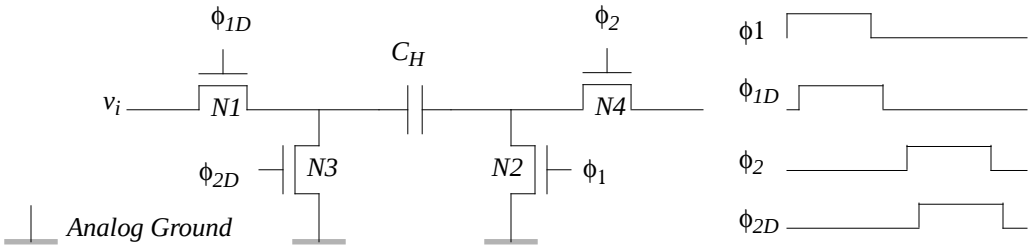


Figure 4.9: Bottom-plate sampling technique to eliminate signal dependent charge injection

nMOSFET switch $N2$ is independent of the signal because it is connected to analog ground. Switch $N2$ is opened first, thus the charge injected to the sampling capacitor is signal independent. Charge injected by the switch $N1$ to the top plate causes no error because it is shorted to ground in the next phase.

Another charge injection error is due to clock coupling through the gate to drain overlap capacitance. In a fully differential architecture, Figure 4.10, both clock feedthrough and fixed channel charge is cancelled.

Noise Errors

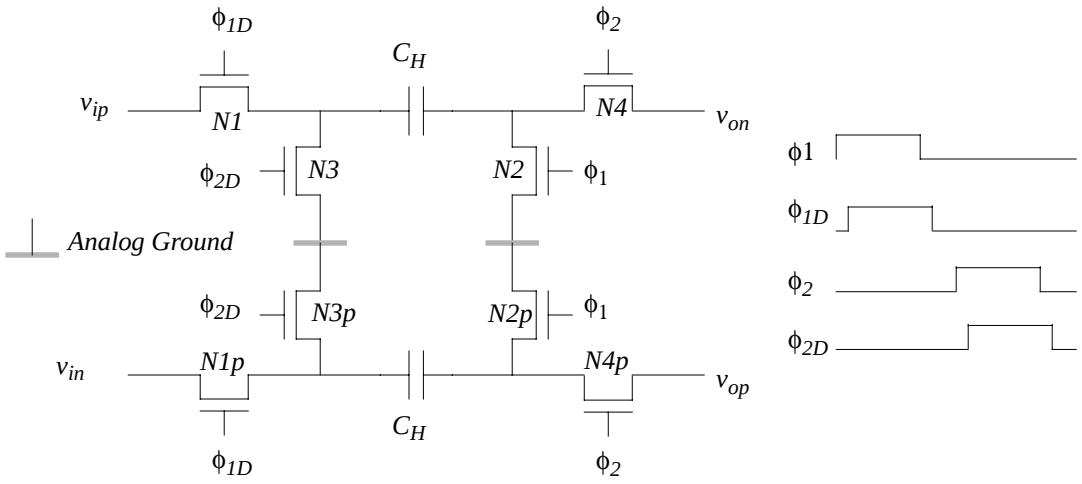


Figure 4.10: Fully differential bottom-plate sampling to cancel fixed charge injection and clock feedthrough

In SC circuits, thermal and flicker ($1/f$) noise generated by transistors used in opamps and analog switches determine the minimum detectable signal amplitude. The power of flicker noise at high frequencies is very low and therefore its effect on the performance of high frequency SC circuits can be neglected. Thermal noise due to on-resistance of the analog switches and opamp wide-band noise is analyzed for a single-ended SC amplifier. During the sampling phase, Figure 4.11a, there will be a mean squared noise charge

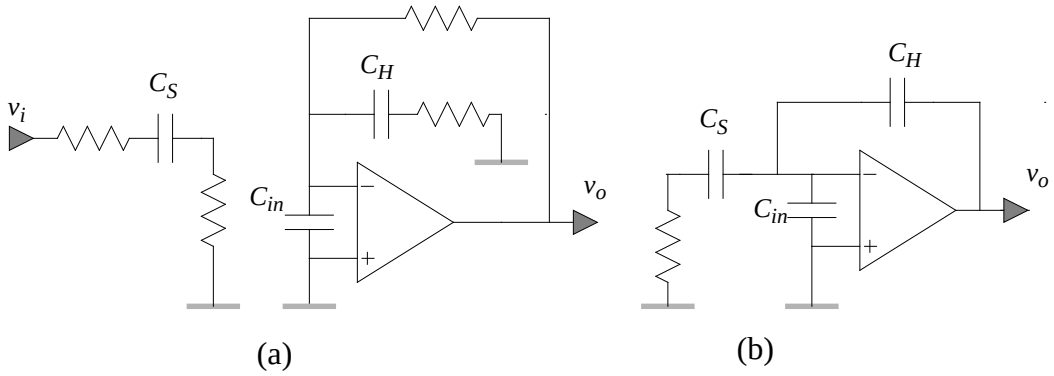


Figure 4.11: Single-ended equivalent circuits of Figure 4.5a during (a) sampling phase, and (b) holding phase

(kTC) on both sampling capacitor C_S and holding capacitor C_H. In the hold phase ϕ_2, Figure 4.11b, there will be a new kTC_S noise on sampling capacitor. The thermal noise on holding capacitor during ϕ_2 is at low frequencies and will not affect the circuit. The net

noise on the sampling capacitor (i.e. $2kTC_S$) is transferred to the holding capacitor and the total charge noise power at the output will be

$$\bar{q}_n^2 = kT(C_H + 2C_S) \ . \qquad (4\text{-}18)$$

The mean squared kT/C noise voltage at the output will be

$$\bar{v}_{n(out)}^2 = \frac{\bar{q}_n^2}{C_H^2} = \frac{kT}{C_H}(1 + 2G) \ , \qquad (4\text{-}19)$$

where $G = C_S/C_H$ is the gain of the SC amplifier. In a fully differential SC architecture, there are twice as many capacitors as in a single-ended SC circuit, thus the noise power is doubled. Moreover, for a constant power dissipation and speed, capacitor sizes in a fully differential circuit must be half the size (thus having twice the noise power) of a single-ended circuit. Therefore, the thermal kT/C noise of a fully differential circuit will be four times higher than that of a single-ended circuit. However, the voltage swing of a fully differential circuit is twice as high (4 times in power) as that of a single-ended SC circuit. Thus, for a given speed and power dissipation the SNR will be equal for both a fully differential and a single-ended SC circuit.

The thermal noise associated with an opamp has a power spectral density of at least

$$S_{OTA}(f) = 4kT\left(\frac{2}{3} \cdot \frac{1}{g_m}\right). \qquad (4\text{-}20)$$

Assuming a single-pole opamp and using the equivalent noise bandwidth ($\omega_{3dB}/4$) introduced in [Gray93], the total opamp thermal noise power will be

$$\bar{v}_{nT(ota)}^2 = \frac{2}{3} \cdot \frac{kT}{C_{TL}} \cdot \beta \ , \qquad (4\text{-}21)$$

where β and C_{TL} are given by (4-8) and (4-15) respectively. The input referred overall voltage noise power of the SC amplifier can be expressed as

$$\bar{v}_n^2 = kT\left(\frac{1 + 2G}{C_H} + \frac{2}{3} \cdot \frac{\beta}{C_{TL}}\right)\left(\frac{C_H}{C_S}\right)^2 \qquad (4\text{-}22)$$

In a sample-and-hold circuit where $C_S = C_H = C_{in} = C_L = C_u$, the RMS value of the input referred thermal noise voltage is

$$\bar{v}_{n,\,i} = \sqrt{\frac{47}{15} \cdot \frac{kT}{C_u}} \qquad (4\text{-}23)$$

If the above sample-and-hold is changed to a SC amplifier with a gain of 0.5 (by changing $C_H = 2C_u$) the input referred thermal noise will be

$$\bar{v}_{n,\,i} = 2\sqrt{\frac{7}{6} \cdot \frac{kT}{C_u}} \qquad (4\text{-}24)$$

Capacitor Mismatch Error

Another source of gain error is due to capacitor mismatch. Device matching is technology and layout dependent. Dielectric thickness variation and edge errors across the die contribute to inaccuracy in capacitance matching. In general, matching is improved as the size of the devices to be matched is increased. Proximity and having similar geometry also help to achieve better matching. Typically, poly-to-poly capacitor matching in the order of 1% to 0.1% is readily achievable in many analog CMOS processes.

An efficient architecture for unity gain sample-and-hold exists which is immune to capacitor mismatch and requires one capacitor to perform both sample and hold operations, as shown in Figure 4.12.

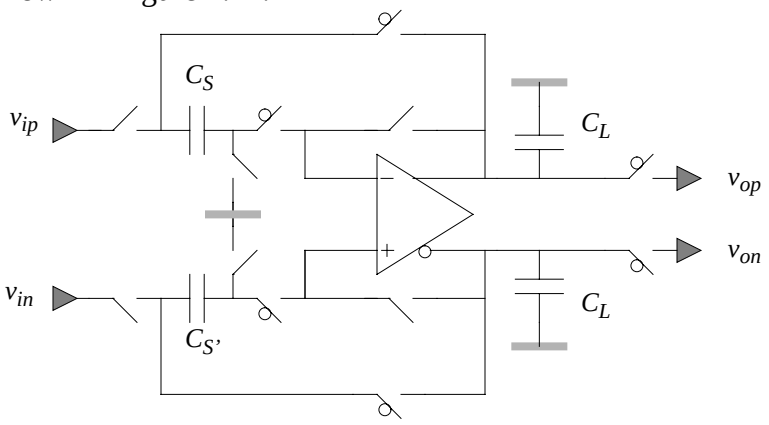


Figure 4.12: One capacitor sample-and-hold circuit

In this circuit, during ϕ_1 input voltage is stored on sampling capacitor C_S and during ϕ_2

capacitor C_S is switched to the output and plays the role of holding capacitor. Thus, gain error due to mismatch between sampling capacitor and holding capacitor is irrelevant. Furthermore, the one-capacitor sample-and-hold structure has other advantages over the two-capacitor version. In the one-capacitor sample-and-hold circuit, finite opamp gain A still causes gain error and the transfer function is

$$H(z) = \frac{V_{od}}{V_{id}}(z) = \frac{1}{1+\frac{1}{A\beta}} \cdot z^{-1/2}, \qquad (4\text{-}25)$$

where the feedback factor β is given by

$$\beta = \frac{C_S}{C_S + C_{in}}. \qquad (4\text{-}26)$$

Compared to the two-capacitor sample-and-hold circuit, the one-capacitor sample-and-hold structure has a higher β and therefore a lower gain error.

The total load capacitance in this sample-and-hold circuit is

$$C_{TL} = C_L + \frac{C_S C_{in}}{C_S + C_{in}}. \qquad (4\text{-}27)$$

The value of C_{TL} is less in a single capacitor sample-and-hold circuit (4-27) than in a two-capacitor sample-and-hold circuit (4-15). From equation (4-14), a lower equivalent output capacitance results in a higher unity gain frequency ω_u. Therefore, the closed loop time constant (4-12) of the one-capacitor sample-and-hold is smaller than the closed-loop time constant of a two-capacitor sample-and-hold circuit due to both higher ω_u and higher β.

In the one-capacitor sample-and-hold circuit, the sampling capacitor is the only source of thermal kT/C noise. Therefore, the output kT/C noise power (which is the same as input referred noise power) in the one-capacitor sample-and-hold circuit is kT/C_S and is 5 dB lower than the two-capacitor sample-and-hold circuit. Again, in a fully differential structure, the noise power is doubled and is equal to $2kT/C_S$.

Example 4.1: In sample-and-hold circuits of Figure 4.5 and Figure 4.12, if opamp input

capacitance C_{in} and output load C_L are equal to the sampling capacitor C_S (and holding capacitor C_H), the one-capacitor sample-and-hold SC circuit is about 1.6 times faster than the two-capacitor sample-and-hold SC circuit.

4.3 Full Delay SC Circuits

The SC amplifier of Figure 4.5 performs a half delay operation. A simple full delay SC circuit is obtained by cascading two of these half delay circuits with alternate ϕ_1 and ϕ_2 clock phases as shown in Figure 4.13. This two-stage SC amplifier circuit delays the input

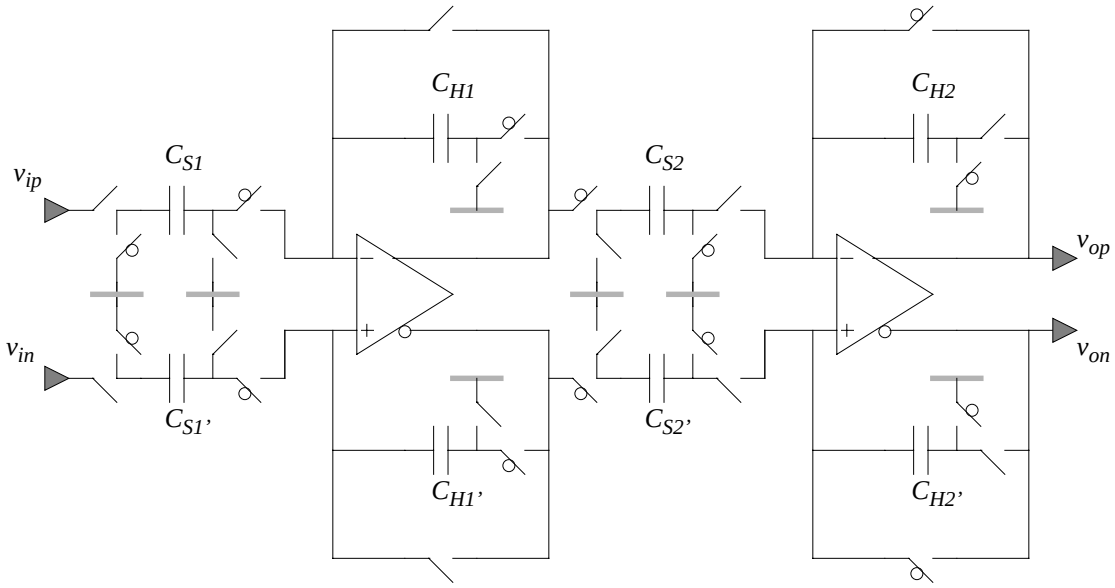


Figure 4.13: A simple cascade SC delay circuit

signal for a full clock period and scales it. The z-domain transfer function of this circuit is

$$\frac{V_{od}}{V_{id}}(z) = \frac{C_{S1}}{C_{H1}} \cdot \frac{C_{S2}}{C_{H2}} \cdot z^{-1}. \qquad (4\text{-}28)$$

Both opamps in this configuration are idle for a half clock period. A more efficient full delay gain stage circuit is achieved by merging the two half delay circuits into a cell using one opamp [Longo93], as shown in Figure 4.14. The z-domain transfer function of this circuit is

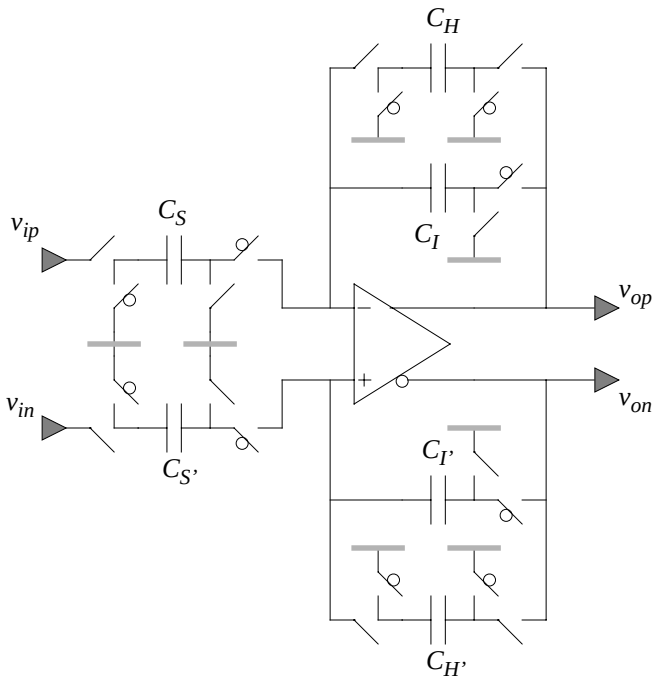


Figure 4.14: A SC delay gain stage

$$H_D(z) = \frac{V_{od}}{V_{id}}(z) = \frac{C_S}{C_H} \cdot z^{-1} \ . \qquad (4\text{-}29)$$

Finite opamp gain causes gain and phase error in the full delay circuit of Figure 4-14, as analyzed below. Single-ended equivalent circuits for the SC delay circuit of Figure 4.14 during ϕ_1 and ϕ_2 are depicted in Figure 4.15. An opamp gain of A causes the virtual

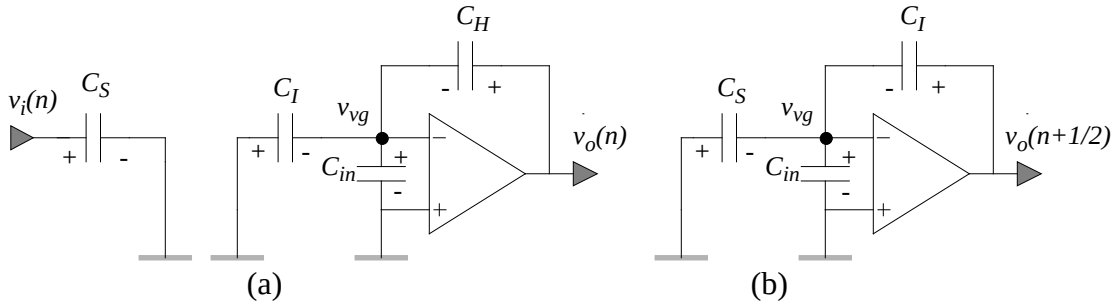


Figure 4.15: A single-ended equivalent circuit of Figure 4.14 during (a) ϕ_1 and (b) ϕ_2 phases

ground node of the opamp v_{vg} to be at $-v_o/A$ with respect to analog ground. The charge conservation equation before and after ϕ_2 yields the following difference equation:

$$C_S\left[v_i(n)-\frac{v_o(n+1/2)}{A}\right]+C_I\left[\frac{v_o(n)}{A}-\left(v_o(n+1/2)+\frac{v_o(n+1/2)}{A}\right)\right] = C_{in}\left[\frac{-v_o(n)}{A}+\frac{v_o(n+1/2)}{A}\right] \quad (4\text{-}30)$$

In the z-domain, the transfer function of the half delay circuit (during ϕ_2 in Figure 4-14) becomes

$$H_{HD}(z) = \frac{C_S}{C_I}z^{-1/2}\left[\frac{g_0}{1-p_0z^{-1/2}}\right] \quad (4\text{-}31)$$

where g_0 and p_0 are given by

$$g_0 = \frac{1}{1+1/A\beta} \qquad p_0 = \frac{g_0}{A}\left(1+\frac{C_{in}}{C_I}\right), \quad (4\text{-}32)$$

where $\beta = C_I/(C_I+C_S+C_{in})$. If $1/A\beta \ll 1$, the above equations can be simplified to

$$g_0 \approx 1-1/A\beta \qquad p_0 \approx \frac{1}{A}(1+C_{in}/C_I)\ . \quad (4\text{-}33)$$

The term in the square bracket of equation (4-31) is the error term $E(z)$. The frequency response of the error term is derived by substituting $z = e^{j\omega T}$ in $E(z)$, and is given by

$$E(e^{j\omega T}) = \frac{g_0}{1-p_0\cos(\omega T/2)+jp_0\sin(\omega T/2)}\ . \quad (4\text{-}34)$$

The magnitude $|E(\omega)|$ and the phase $\angle E(\omega)$ of the above equation are

$$|E(\omega)|^2 = \frac{g_0^2}{[1-p_0\cos(\omega T/2)]^2+[p_0\sin(\omega T/2)]^2} \quad (4\text{-}35)$$

$$\angle E(\omega) = -\tanh\frac{p_0\sin(\omega T/2)}{1-p_0\cos(\omega T/2)}\ . \quad (4\text{-}36)$$

For $A \gg 1$, we have $p_0 \ll 1$ and the magnitude and phase of the error term can be approximated as

$$|E(\omega)| = m_{HD} = 1 - \frac{1}{A\beta} + \frac{\cos(\omega T/2)}{A}\left(1 + \frac{C_{in}}{C_H}\right) \quad (4\text{-}37)$$

$$\angle E(\omega) = \theta_{HD} = -\frac{\sin(\omega T/2)}{A}\left(1 + \frac{C_{in}}{C_H}\right) . \quad (4\text{-}38)$$

Therefore, the transfer function of the half delay SC circuit with finite opamp gain will be

$$H_{HD}(z) = \frac{C_S}{C_I} z^{-1/2}[m_{HD} \cdot e^{j\theta_{HD}}] . \quad (4\text{-}39)$$

The full delay SC circuit of Figure 4.14 will experience errors during ϕ_1 and ϕ_2 and the actual transfer function of the full delay circuit will be

$$H_{FD}(z) = \frac{C_S}{C_H} z^{-1}\left[\frac{(g_0)_{\phi_1}}{1 - (p_0)_{\phi_1} z^{-1/2}} \cdot \frac{(g_0)_{\phi_2}}{1 - (p_0)_{\phi_2} z^{-1/2}}\right] . \quad (4\text{-}40)$$

Substituting $z = e^{j\omega T}$ in the above equation and assuming $(p_0)_{\phi_1}$ and $(p_0)_{\phi_2} \ll 1$, the magnitude and the phase of the error term in a full delay circuit due to finite opamp gain are obtained to be

$$m_{FD} = 1 - \frac{1}{A}\left[\frac{1}{\beta_{\phi_1}} + \frac{1}{\beta_{\phi_2}}\right] + \frac{\cos(\omega T/2)}{A}[(1 + C_{in}/C_I) + (1 + C_{in}/C_H)] \quad (4\text{-}41)$$

$$\theta_{FD} = -\frac{\sin \omega T/2}{A}[(1 + C_{in}/C_I) + (1 + C_{in}/C_H)] , \quad (4\text{-}42)$$

where β_{ϕ_1} and β_{ϕ_2} are the feedback factor during ϕ_1 and ϕ_2 respectively.

The actual transfer function of a full delay circuit is

$$H_{FD}(z) = \frac{C_S}{C_H} z^{-1}[m_{FD} \cdot e^{j\theta_{FD}}] \quad (4\text{-}43)$$

Example 4.2: In the SC full delay circuit of Figure 4.14, opamp DC gain is 100, signal is a sinusoid with frequency of $f_S/4$ and $C_S = C_I = C_H = C_{in}$. The gain and phase of the error term, calculated from (4-41) and (4-42) respectively, are

$$m_{FD} = 0.968 \qquad \theta_{FD} = -0.028\,. \qquad (4\text{-}44)$$

Therefore, an opamp gain of 40 dB will cause 3.2 % gain error in the full delay SC sample-and-hold circuit. The phase error is 2.8 % (in the sense that $\left|e^{-j0.028} - e^{j0}\right|$ is 2.8 % of e^{j0}).

A Double-Sampled SC Delay Cell

The opamp in the one-capacitor sample-and-hold circuit of Figure 4.12 is idle during the sampling phase ϕ_1. By duplicating the sampling circuitry and using an alternate clock phase for it, a two-path SC sample-and-hold is obtained, as shown in Figure 4.16.

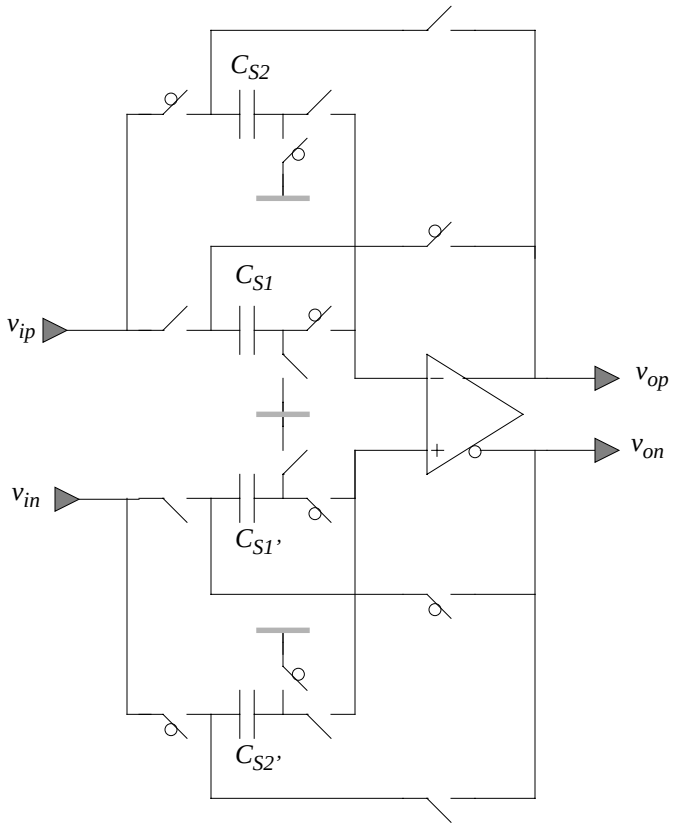
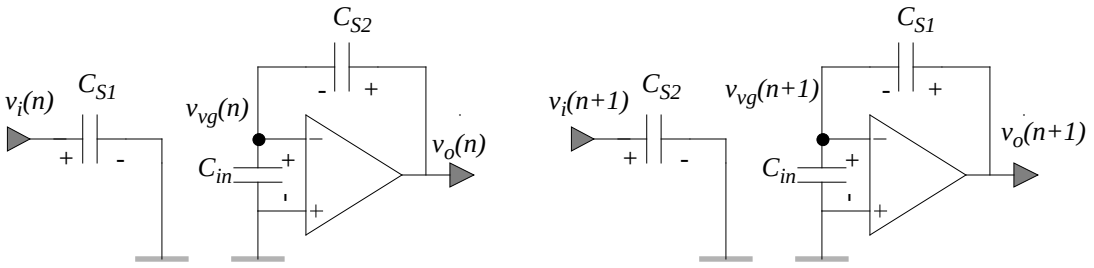


Figure 4.16: A double-sampled SC delay circuit

In this circuit, the input signal is sampled every half clock period ($T_s/2$) and appears at the output with a half-clock period delay. Thus, the transfer function of this cell is

$$\frac{V_{od}}{V_{id}}(\hat{z}) = \hat{z}^{-1}\,, \qquad (4\text{-}45)$$



(a) (b)

Figure 4.17: A single-ended equivalent circuit of Figure 4.16 during (a) ϕ_1 and (b) ϕ_2 phases

where $\hat{z} = e^{j\omega(T_s/2)}$.

Therefore, the effective sampling frequency in this two-path sample-and-hold circuit is twice the clock frequency. This structure is also called a double-sampled SC circuit [Choi80] [Hurst90]. The factor-of-two improvement in the speed of the double-sampled SC delay cell is achieved without increasing the clock rate or requiring a faster opamp settling time. In return, mismatch and uneven clock phases create image errors as we will discuss later.

Finite opamp gain and opamp input capacitance cause both gain and phase error in the transfer function of the double-sampled SC delay circuit. Figure 4.17 shows a single-ended equivalent circuit of the double-sampled delay circuit during ϕ_1 and ϕ_2. Charge conservation on capacitors C_{S1} and C_{in} before ϕ_2 (the non-overlapping phase) and after ϕ_2 yields the following difference equation:

$$C_{S1}\left[v_i(n) - \left(v_o(n+1) + \frac{v_o(n+1)}{A}\right)\right] = C_{in}\left[\frac{v_o(n)}{A} + \frac{v_o(n+1)}{A}\right] \quad . \qquad (4\text{-}46)$$

Here the time indices at the end of ϕ_1 and ϕ_2 are denoted by n and $n+1$ respectively due to the double sampling property of the circuit. If capacitors $C_{S1} = C_{S2} = C_S$, a similar difference equation would be obtained for the ϕ_1 phase and the overall transfer function in z-domain will be

$$\frac{V_{od}(z)}{V_{id}(z)} = H_{dD}(z) = \left[\frac{g_0}{1 - p_0 z^{-1}}\right] z^{-1} \quad , \qquad (4\text{-}47)$$

where g_0 and p_0 are given by

$$g_0 = \frac{1}{1 + \frac{1}{A} + \frac{C_{in}}{C_S} \cdot \frac{1}{A}} \qquad (4\text{-}48)$$

$$p_0 = \frac{C_{in}}{C_S} \cdot \frac{g_0}{A}. \qquad (4\text{-}49)$$

Thus, finite opamp gain and non-zero input capacitance modify the transfer function of the double-sampled delay cell by a damped integrator term from its ideal response. This change of transfer function causes both gain and phase error in the response of the delay circuit. The actual transfer function becomes

$$H_{dD}(z) = [m_{dD} \cdot e^{j\theta_{dD}}] \cdot z^{-1} \quad , \qquad (4\text{-}50)$$

where m_{dD} and θ_{dD} are magnitude and phase of the error term in the double-sampled delay circuit. Assuming $A \gg 1$, the magnitude and phase error are given by

$$m_{dD} \approx 1 - \frac{1}{A\beta} + \frac{\cos \omega T}{A}\left(\frac{C_{in}}{C_S}\right) \qquad (4\text{-}51)$$

$$\theta_{dD} \approx -\frac{\sin \omega T}{A}\left(\frac{C_{in}}{C_S}\right). \qquad (4\text{-}52)$$

Example 4.3: In Figure 4.16, if the input capacitance of the opamp is equal to the sampling capacitor and the opamp has 40 dB DC gain, both gain error and phase error are 1 % for a signal at one half the clock frequency.

A major limitation of double-sampled SC circuits is due to mismatch in the two paths [Gregorian86] that causes in-band image of the signal as described later. However, the double-sampled circuit of Figure 4.16 uses the one-capacitor sample-and-hold architecture and its gain is not affected (to a first order) by capacitor mismatch.

Double-sampled SC circuits are a subset of a class of circuits called N-path filters with N being equal to two. A diagram of a two-path circuit and its corresponding clock phases is shown in Figure 4.18.

The non-overlapping clock has a frequency of f_{clock} and the effective sampling frequency (f_s) of a double-sampled SC circuit is $f_s = 2f_{clock}$. The sequence of the signals during ϕ_1 (odd samples) is denoted by an "o" superscript and the sequence of the signals during ϕ_2 (even samples) is denoted by an "e" superscript. The odd and even sequences have a sampling frequency of $f_{clock} = f_s/2$. The input sequence v_{in} is a time-interleaved vector sum of odd (v_{in}^o) and even (v_{in}^e) sequences and in the z-domain we have

$$V_{in}(z) = V_{in}^o(z) + V_{in}^e(z) \qquad (4\text{-}53)$$

Similarly, the output sequence is expressed as

$$V_{out}(z) = V_{out}^o(z) + V_{out}^e(z) \ , \qquad (4\text{-}54)$$

where odd and even sequences are related by

$$V_{out}^o(z) = H(z)V_{in}^o \qquad V_{out}^e(z) = H(z)V_{in}^e \ . \qquad (4\text{-}55)$$

If the two paths are not symmetric and, for instance, there is a gain mismatch of δ between them, the input-output relation is

$$V_{out}(z) = (1+\delta)H(z)V_{in}^o + H(z)V_{in}^e \ . \qquad (4\text{-}56)$$

This equation can be expressed as

$$V_{out}(z) = H(z)[V_{in}(z) + \delta V_{in}^o(z)] \ . \qquad (4\text{-}57)$$

Therefore, a mismatch between the two channels is equivalent to having an attenuated image of the signal being applied at the input along with the real input. Figure 4.19 shows

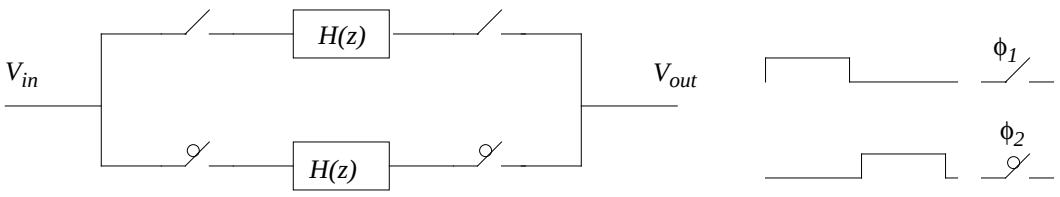


Figure 4.18: Two-path SC circuit and clock phases

the periodic spectrum of the input signals V_{in} and δV_{in}^{o}.

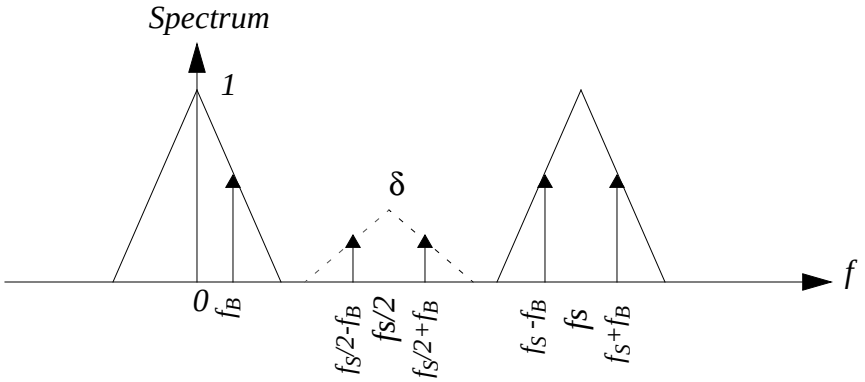


Figure 4.19: Spectrum of the input signal V_{in} (solid line) and the attenuated odd samples of the input signal (dotted line)

In the frequency domain, a sampled input signal V_{in} with a frequency f_B will have a periodic spectrum with the signal appearing at $\imath f_s \pm f_E$. The odd sequence of the signal has a sampling frequency of $f_s/2$ and thus attenuated images appear at $n(f_s/2) \pm f_B$.

Non-uniform sampling due to uneven ϕ_1 and ϕ_2 phases has a similar effect [Yang94]. If phase ϕ_1 is longer by an amount τ compared to the ϕ_2 phase, then we can write $1 + \delta = e^{-s\tau} \approx 1 - s\tau$, so $\delta \approx -s\tau$.

4.4 A SC Bandpass Sigma-Delta Modulator

A fully differential SC resonator using two sample-and-hold delay cells in a negative feedback loop is illustrated in Figure 4.20.

In this circuit, if all the capacitors have the same size the transfer function of the resonator is

$$H_R(z) = \frac{V_{od}}{V_{id}}(z) = \frac{z^{-2}}{1 + z^{-2}} \ . \qquad (4\text{-}58)$$

Poles of this resonator are at $z = \pm j$. Capacitor mismatch and finite opamp gain cause errors in the transfer function.

If the gain error in the unity gain delay cell due to capacitor mismatch is δ, the resulting transfer function of the resonator will be

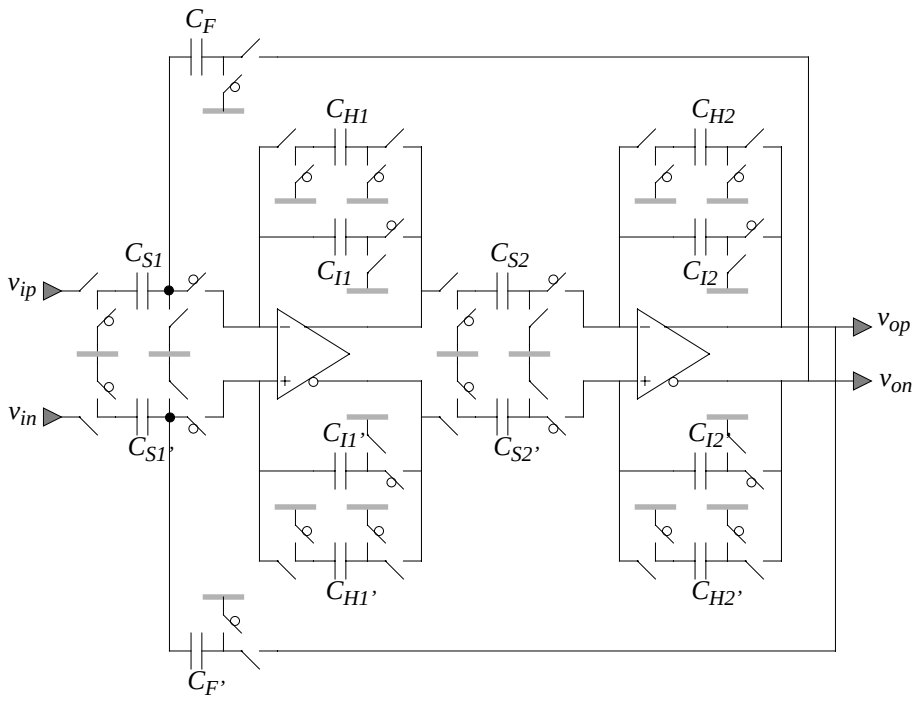


Figure 4.20: A SC resonator using two delay cells

$$H_R(z) = \frac{(1-\delta)^2 z^{-2}}{1+(1-\delta)^2 z^{-2}} \ . \qquad (4\text{-}59)$$

The new location of poles are at $z = \pm(1-\delta)j$. Therefore, a δ percent gain error in the unity gain delay circuit will cause 2δ percent change in the gain of the resonator and δ percent change in the location of the poles of the resonator. Note that the poles of the resonator are still on the $j\omega$-axis.

In section 4.3, it was shown that finite opamp gain causes both gain error and phase error in the ideal transfer function of a SC delay circuit, and the actual transfer function is given by (4-43). Using this transfer function for the delay cell, the resonator transfer function will be

$$H_R(z) = \frac{[(m_{FD1}\cdot e^{j\theta_{FD1}})\cdot(m_{FD2}\cdot e^{j\theta_{FD2}})]z^{-2}}{1+[(m_{FD1}\cdot e^{j\theta_{FD1}})\cdot(m_{FD2}\cdot e^{j\theta_{FD2}})]z^{-2}} \ , \qquad (4\text{-}60)$$

where m_{FDi} and $e^{j\theta_{FDi}}$ are the gain and phase error of the i-th delay cell. Poles of this

resonator are

$$z_{p1,\,p2} = \pm j\sqrt{m_{FD1} \cdot m_{FD2}} \cdot e^{j\frac{(\theta_{FD1} + \theta_{FD2})}{2}}. \qquad (4\text{-}61)$$

Thus, resonator poles are moved inside the unit circle (because $m_{FD1} \cdot m_{FD2} < 1$) and have a phase lag of θ_{R0}. Using the simplified equation of (4-42), the phase shift of the $f_s/4$ resonator is

$$\theta_{R0} = \frac{\sqrt{2}}{2A}[(1 + C_{in}/C_I) + (1 + C_{in}/C_H)] \qquad (4\text{-}62)$$

Example 4.4: If an $f_s/4$ resonator is built using two delay cells in a negative feedback loop and the capacitor sizes in terms of a unit capacitor C_u are $C_{in} = C_I = 2C_u$ and $C_H = C_u$, an opamp gain of 40 dB will cause a phase error of 0.035 radians, almost 2.2 % of the nominal frequency.

A resonator with an arbitrary gain is achieved by choosing different values for the capacitors C_{S2} and C_{I2} in the second delay cell of the resonator of Figure 4.20. During ϕ_2 the transfer function of this circuit is

$$H_R(z) = \frac{C_{S2}}{C_{I2}} \cdot \frac{z^{-3/2}}{1 + z^{-2}}. \qquad (4\text{-}63)$$

If $C_{I2} = 2C_{S2}$, a resonator with gain of 0.5 is obtained which is useful for the implementation of the fourth-order bandpass ΣΔ modulator shown in Figure 4.1.

A fourth-order SC ΣΔ modulator is achieved by cascading two resonators and a quantizer in a feedback loop as shown in Figure 4.21.

In this circuit all the capacitors are identical (C_u) except for the four marked by asterisks which have a value of $2C_u$. These four capacitors scale the gain of the resonators to the required value of 0.5.

Speed of operation is determined by the closed-loop time constant of the opamps, as discussed before. Worst case opamp loading for this architecture occurs for the second opamp (OA2) during ϕ_1, and a single-ended representation of it is shown in Figure 4.22a.

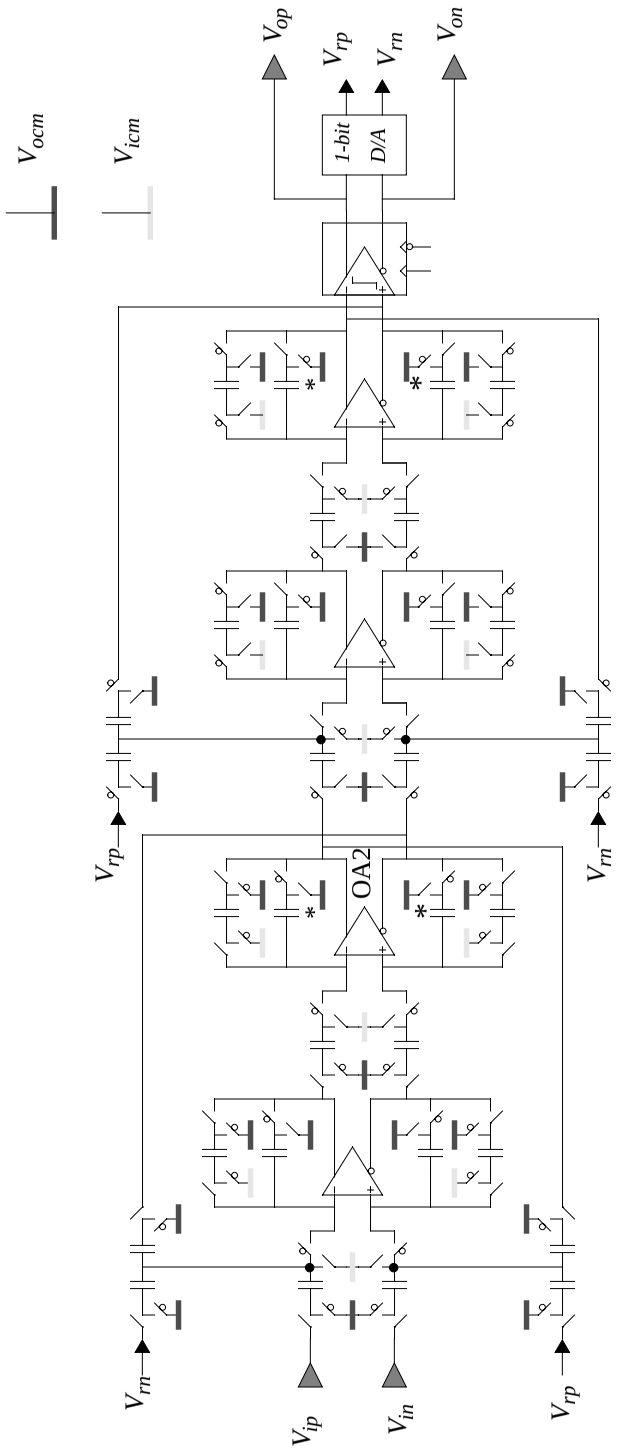


Figure 4.21: A fourth-order SC bandpass sigma-delta modulator

If the opamp input capacitance C_{in} is assumed to be equal to the unit capacitance C_u used in the modulator, the worst case closed-loop time constant is found to be $\tau = 7C_u/g_m$ (from equation (4-12)).

A similar analysis for the fourth-order SC bandpass ΣΔ reported in [Longo93] indicates that the first opamp during ϕ_2 has the worst case loading, as shown in Figure 4.22b. The settling time constant of this structure is $9C_u/g_m$, which is about 28 % slower than the circuit presented in this work.

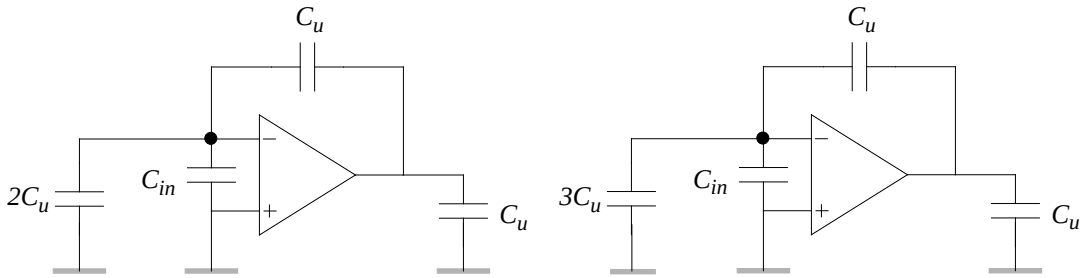


Figure 4.22: Worst case opamp loading for (a) bandpass ΣΔ of Figure 4.21
(b) bandpass ΣΔ modulator in [Longo93]

This modulator was simulated in Eldo using near ideal models for switches, capacitors, opamps, and the quantizer. The DC gain of opamps was set to 60 dB and switch on-resistance was set to 200 Ω. Figure 4.23 shows the modulator output spectrum for a 24.9 MHz sinusoidal input signal with an amplitude of 12 dB below full scale. The

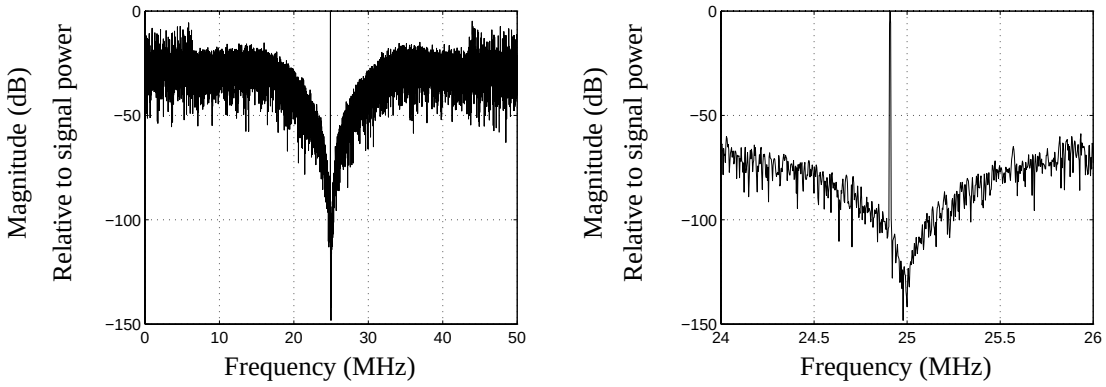


Figure 4.23: Output spectrum from Eldo simulation

sampling rate of 100 MHz is provided by a two-phase non-overlapping clock. Simulated SNR are 94.3 dB and 58.8 dB in 200 kHz ($OSR = 250$) and 1 MHz ($OSR = 50$) bandwidths respectively.

4.4.1 Sources of Error

Practical analog circuit realization of bandpass sigma-delta modulators involves errors due to device and circuit non-idealities. In the following section, some prominent sources of error, namely capacitor mismatch, finite opamp gain, and thermal noise are considered.

Capacitor Mismatch

Noise shaping is determined by the quality of the resonators used in the forward path of the modulator. Resonators used in the bandpass ΣΔ modulator have a gain of 0.5 and their ideal transfer function is

$$H_R(z) = \frac{1}{2} \cdot \frac{z^{-2}}{1 + z^{-2}} . \qquad (4\text{-}64)$$

A mismatch of δ between capacitors changes the ideal transfer function of the resonators to

$$H_R(z) = \frac{1}{2} \cdot \frac{g_0 z^{-2}}{1 + p_0 z^{-2}} \qquad (4\text{-}65)$$

where

$$g_0 = p_0 = (1 - \delta)^2 . \qquad (4\text{-}66)$$

As mentioned earlier, gain of the second resonator is not a critical parameter because it is followed by a high gain quantizer. Thus, gain error in the second resonator is not going to affect the ideal behavior of the modulator. Simulations show that changing the gain of the second resonator by as much as ±100 % has virtually no effect on the SNR of the modulator. However, gain error in the first resonator will deteriorate the SNR of the modulator.

The ideal resonator of (4-64) has infinite gain at $f_S/4$. The gain of the actual resonator of

(4-65) at a quarter of the sampling frequency is

$$H_{R0} = H_R(e^{j\omega T})\Big|_{f = f_S/4} = \frac{g_0}{1-p_0} \approx \frac{1}{2\delta}. \qquad (4\text{-}67)$$

A lower resonator gain causes less attenuation of the quantization noise in the narrow band around $f_S/4$. Performing a bandpass to lowpass transformation, using a $z^{-2} \rightarrow -z^{-1}$ change of variable on the resonator of (4-65), results in

$$H_I(z) = \frac{-g_0 z^{-1}}{1-p_0 z^{-1}}, \qquad (4\text{-}68)$$

which is a leaky integrator with DC gain of $H_{I0} = g_0/(1-p_0)$. From (4-67), we can see a capacitor mismatch of δ reduces the DC gain in (4-68) to $H_{I0} = 1/2\delta$. The effect of integrator leakage on the in-band quantization error of a second-order lowpass ΣΔ has been analyzed in [Boser88] and is given by

$$\frac{S_B}{S_{B0}} = 1 + \frac{5}{\pi^4}\left(\frac{OSR}{H_{I0}}\right)^4 + \frac{10}{3\pi^2}\left(\frac{OSR}{H_{I0}}\right)^2 . \qquad (4\text{-}69)$$

Here, S_B is the power of in-band quantization noise for a leaky integrator, and S_{B0} is the power of in-band quantization noise for a perfect integrator. If the DC gain of the integrator (or equivalently, resonator gain at $f_s/4$) is equal to the oversampling ratio OSR of the modulator, the SNR performance loss is about 1.3 dB.

Therefore, matching between capacitors must be better than $1/(2 \cdot OSR)$ in a fourth-order bandpass ΣΔ modulator.

Finite Opamp Gain

Finite opamp gain causes errors in the resonant frequency and the gain of the resonator. This in turn changes the position of the notch in the noise transfer function of the bandpass ΣΔ modulator away from $f_s/4$, and also increases the in-band quantization noise. The notch will be shifted to a lower frequency $f_s/4 - \Delta f$, where

$$\Delta f = \frac{f_s}{2\pi} \cdot \theta_{R0}. \qquad (4\text{-}70)$$

In this equation, θ_{R0} is the phase error associated with the poles of the resonator and is given by (4-62). The frequency shift of the notch can be expressed in terms of the opamp gain and oversampling ratio of the modulator as

$$\Delta f = \frac{\theta_{R0}}{\pi} \cdot OSR \cdot BW. \qquad (4\text{-}71)$$

For a fourth-order bandpass ΣΔ modulator with a quantization noise slope of about 15 dB/octave, a Δf shift in the notch frequency will increase the power of in-band quantization noise by ΔS_B which is approximately

$$\Delta S_B = \frac{15}{(BW)/2} \cdot \Delta f = 30 \cdot \frac{\theta_{R0}}{\pi} \cdot OSR \quad \text{dB}. \qquad (4\text{-}72)$$

Substituting θ_{R0} (4-62) in the above equation yields

$$\Delta S_B = 15\frac{\sqrt{2}}{\pi} \cdot \frac{OSR}{A} \cdot \left[2 + \frac{C_{in}}{C_I} + \frac{C_{in}}{C_H}\right]. \qquad (4\text{-}73)$$

For an acceptable SNR loss, the minimum opamp gain can be found in terms of OSR.

Example 4.5: In the bandpass ΣΔ modulator of Figure 4.21, the values of different capacitors in terms of a unit capacitor C_u are: $C_I = C_{in} = 2C_u$ and $C_H = C_S = C_u$. For an oversampling ratio of 40 the minimum required opamp gain is 53 dB, if a penalty of 3 dB SNR loss is acceptable due to notch frequency shift. Note that opamp gain (53 dB) is 21 dB higher than the value of OSR, in decibels.

Example 4.6: In the above example, if the opamp gain is 40 dB and the sampling frequency is 100 MHz, the phase shift θ_{R0} is found to be 0.035 radians and from equation (4-70), the notch frequency shift is found to be 562 kHz.Thus, the resonant frequency will be at 24.44 MHz, instead of being at 25 MHz. For an $OSR = 50$, the in-band quantization noise power (4-72) will increase by about 16.7 dB.

The bandpass SC ΣΔ modulator was simulated using opamps with DC gain of 40 dB, and

the parasitic capacitances at the input of the opamp was assumed to be $2C_u$. The input signal is a 24.9 MHz sinusoid with an amplitude of 12 dB below full scale. Figure 4.24 shows the output spectrum of the modulator. The notch frequency is shifted by about 450 kHz. Simulated SNR are 56.5 dB and 46.1 dB for bandwidth of 200 kHz and 1 MHz respectively.

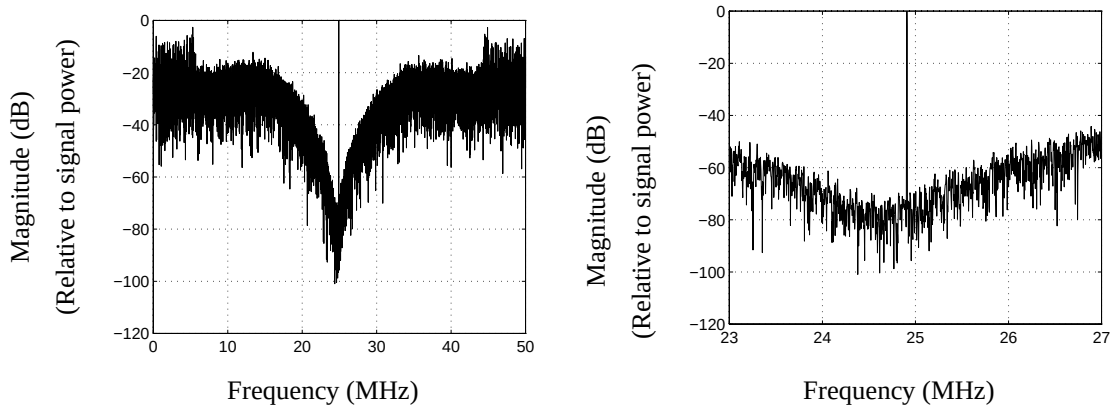


Figure 4.24: Output spectrum of the fourth-order bandpass ΣΔ modulator with an opamp gain of 40 dB and opamp input capacitance of *Cin =2Cu*

If we neglect the phase error, the effect of finite opamp gain on the transfer function of a resonator is similar to capacitor mismatch and the actual transfer function of the resonator will be like equation (4-65), with g_0 and p_0 being

$$g_0 = p_0 = 1 - \frac{1}{A}\left(\frac{1}{\beta_{\phi 1,\,1}} + \frac{1}{\beta_{\phi 2,\,1}} + \frac{1}{\beta_{\phi 1,\,2}} + \frac{1}{\beta_{\phi 2,\,2}}\right) \qquad (4\text{-}74)$$

where, $\beta_{\phi j,\,i}$ is the feedback factor of the ith delay circuit during the ϕ_jth clock phase. If the feedback factors are comparable and assumed to be equal to β, the above equation is simplified to

$$g_0 = p_0 = 1 - \frac{4}{A\beta}. \qquad (4\text{-}75)$$

The gain of the resonator at its resonant frequency is

$$H_{R0}(e^{j\omega T})\Big|_{f\,=\,f_S/4} = \frac{g_0}{1 - p_0} \approx \frac{A\beta}{4}. \qquad (4\text{-}76)$$

The in-band quantization error as a function of resonator gain can be expressed by an equation similar to (4-69). Therefore the minimum required opamp DC gain for this double-resonator SC bandpass ΣΔ modulator is $A_{min(bp)} = 4(OSR)/\beta$.

In a SC integrator, using an opamp with DC gain of A and feedback factor of β, the integrator DC gain is $H_0 \approx A\beta$. Thus, the minimum required opamp DC gain in a lowpass ΣΔ modulator is $A_{min(lp)} = OSR/\beta$. Note that for a similar SNR performance, the opamp used in the sample-and-hold based fourth-order bandpass ΣΔ modulator requires 12 dB higher DC gain than the opamp used in the second-order lowpass ΣΔ modulator.

Figure 4.25 shows the SNR loss as a function of OSR/H_{R0}. From this figure, one can find the requirements on capacitor matching and/or opamp DC gain.

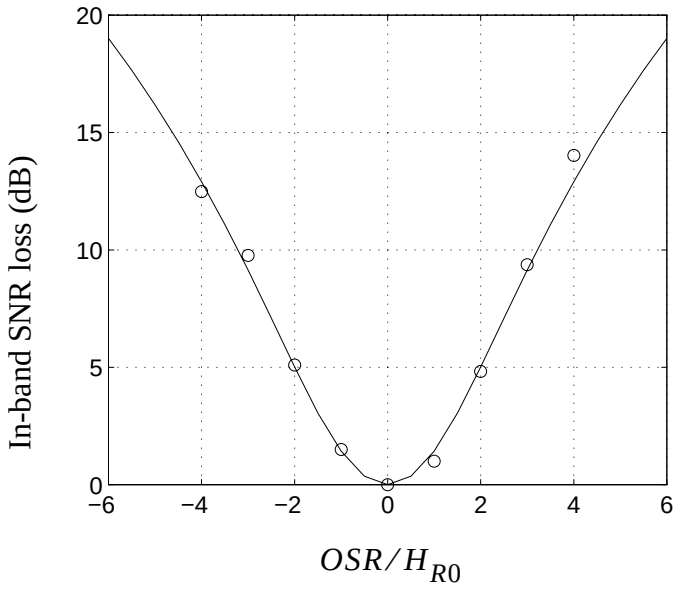


Figure 4.25: SNR loss versus OSR / H_{R0} from analytical result (solid line) and from simulation results (o points).

In the bandpass ΣΔ modulator of Example 4.5, if the oversampling ratio is 40, a capacitor matching accuracy of at least $1.25\,\%$ is needed for a SNR loss of 1.5 dB. Calculating the β during each phase for the two opamps and using equations (4-74) and (4-76), H_{R0} is found to be equal to $A/16$. Thus, the minimum opamp DC gain is 56 dB for the same SNR loss, i.e. 1.5 dB.

Noise

Thermal noise generated by various switches and the two opamps in the first resonator is going to limit the accuracy of the bandpass ΣΔ modulator. Thermal noise generated in the second stage undergoes a second-order band-reject noise shaping, and thus its effect is not critical.

Using the results obtained earlier in this chapter on the analysis of the noise in a SC amplifier, the total input referred thermal noise power of the first stage of the single-ended SC bandpass ΣΔ modulator in Figure 4.21 is

$$\bar{v}_{nT}^2 = \frac{14.75kT}{C_u}. \qquad (4\text{-}77)$$

In this calculation, the input capacitance of the opamp is assumed to be comparable to the unit capacitor, i.e. $C_{in} = C_u$. The total noise power for a fully differential SC circuit is twice as large as (4-77). The in-band noise power is reduced due to the oversampling process and is given by:

$$\bar{v}_{nT}^2\Big|_{in-band} = \frac{29.5}{OSR} \cdot \frac{kT}{C_u} \qquad (4\text{-}78)$$

4.5 A Double-Sampled SC Bandpass Sigma-Delta Modulator

A double-sampled SC resonator is obtained by cascading two double-sampled delay circuits as shown in Figure 4.26. The ideal transfer function of this circuit is

$$H(z) = \frac{C_I}{C_{S1}} \cdot \frac{z^{-2}}{1+z^{-2}}. \qquad (4\text{-}79)$$

In this configuration, capacitance mismatch (between C_I and C_{S1}) causes a gain error on the input signal $v_{id} = v_{ip} - v_{in}$ that is added to the feedback signal using a two-capacitor sample-and-hold architecture. If the error due to capacitor mismatch is δ, the transfer function of the double-sampled resonator will be

$$H(z) = (1+\delta)\frac{C_I}{C_{S1}} \cdot \frac{z^{-2}}{1+z^{-2}}. \qquad (4\text{-}80)$$

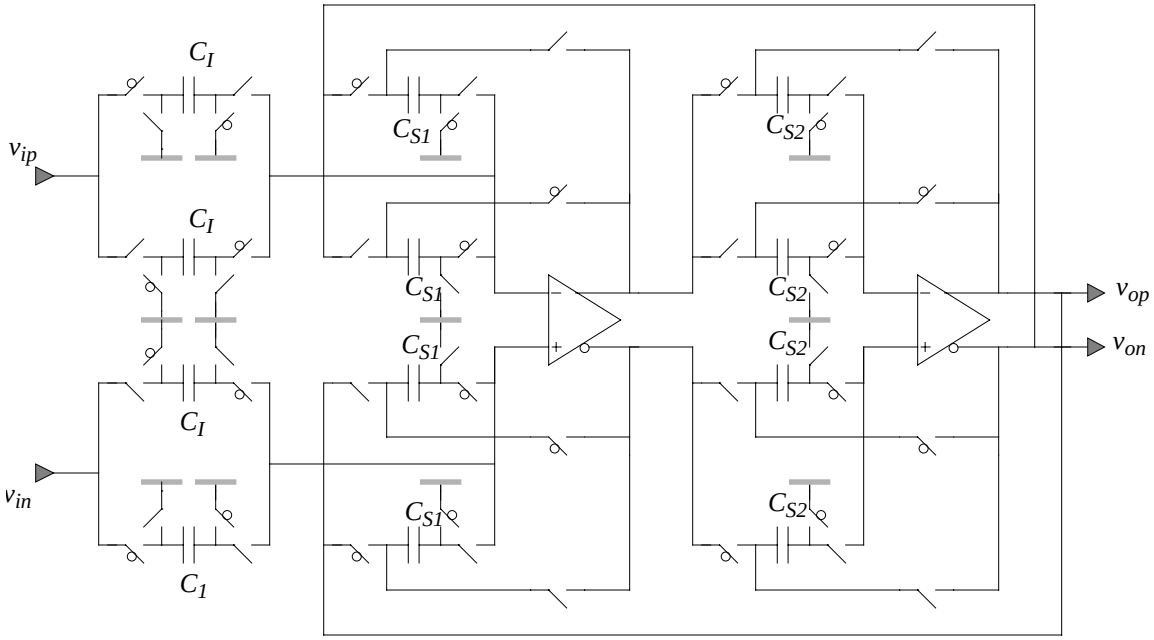


Figure 4.26: A double-sampled SC resonator

Therefore, the location of resonator poles is not affected by the capacitor mismatch. However, finite opamp gain (A) causes errors in the ideal transfer function of a double-sampled SC delay circuit (given by (4-50)) and the transfer function of a double-sampled resonator becomes

$$H_{dR}(z) = \frac{C_I}{C_{S1}} \cdot \frac{[(m_{dD1} \cdot e^{j\theta_{dD1}}) \cdot (m_{FD2} \cdot e^{j\theta_{dD2}})]z^{-2}}{1 + [(m_{dD1} \cdot e^{j\theta_{dD1}}) \cdot (m_{dD2} \cdot e^{j\theta_{dD2}})]z^{-2}} \quad . \qquad (4\text{-}81)$$

Poles of this resonator are

$$z_{p1,\,p2} = \pm j\sqrt{m_{dD1} \cdot m_{dD2}} \cdot e^{j\frac{(\theta_{dD1} + \theta_{dD2})}{2}} \quad . \qquad (4\text{-}82)$$

The poles are inside the unit circle, close to the intersection of $j\omega$-axis and the unit circle. The phase error of the poles of this resonator in radians is

$$\theta_{dR} = -\frac{\sin\omega T}{2A}\left[\frac{C_{in1}}{C_{S1}} + \frac{C_{in2}}{C_{S2}}\right]. \qquad (4\text{-}83)$$

Both magnitude and phase errors are inversely proportional to the DC gain of the opamp.

A double-sampled double-resonator SC bandpass ΣΔ modulator is constructed using two double-sampled resonators and a quantizer in a feedback loop, as shown in Figure 4.27.

All the capacitors are unit size capacitors (C_u), except for the eight marked by asterisks which have a value of $2C_u$, and are made of two unit size capacitors in parallel. The gain of resonators is set by the eight capacitors to the required value of 0.5.

The functionality of this double-sampled SC bandpass ΣΔ modulator was verified in Eldo using ideal components. The on-resistance of the switches was set to $200\ \Omega$ and the DC gain of opamps was assumed to be 60 dB. Figure 4.28 shows the output spectrum of the modulator for a sinusoid input signal of 50.1 MHz. The amplitude of the signal was 12 dB below full scale and the clock frequency was 100 MHz.

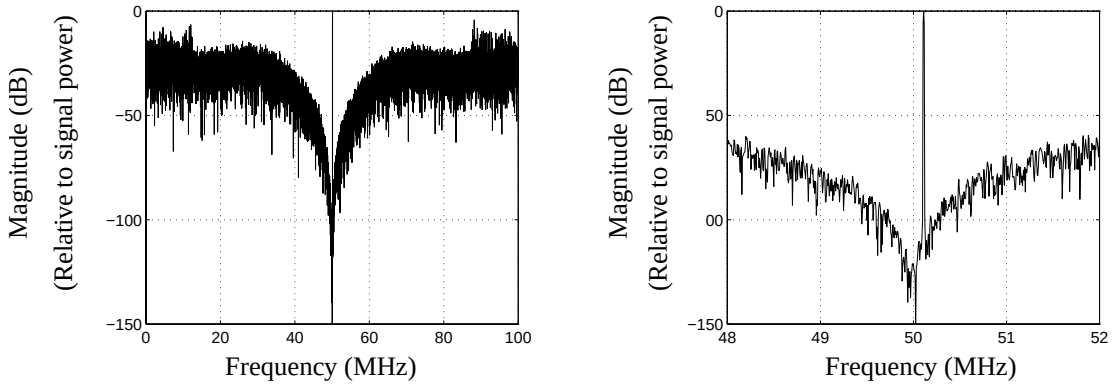


Figure 4.28: Output spectrum from Eldo simulation

Simulated SNR is about 108 dB and 72.8 dB for bandwidths of 200 kHz and 1 MHz respectively. For the same clock frequency and signal bandwidth, the oversampling ratio of this modulator is twice as large as the single-sampled modulator. Thus, the SNR of this modulator is 15 dB higher than that of a single-sampled counterpart.

4.5.1 Sources of Error

Performance of the double-sampled ΣΔ modulator is affected by circuit non-idealities. In the following, effects of some prominent non-idealities such as capacitor mismatch, finite opamp gain, and noise on the SNR of the double-sampled ΣΔ modulator are described.

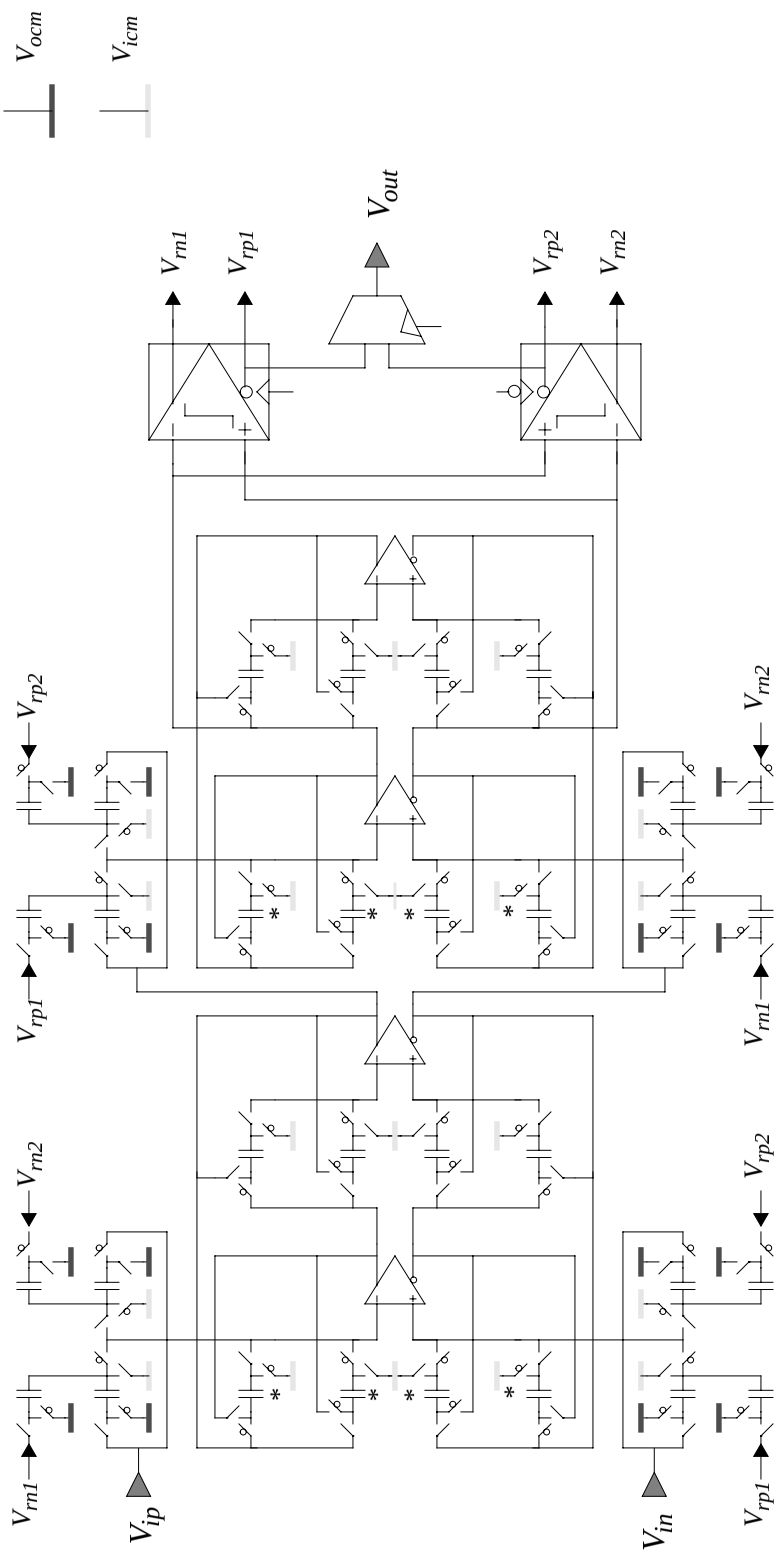


Figure 4.27: A double-sampled SC fourth-order bandpass sigma-delta modulator

Capacitor Mismatch

As mentioned before, double-sampled SC circuits are sensitive to path mismatch and any mismatch between the two channels will produce image problems. Mismatch in the second stage of the modulator is noise shaped (second-order noise-shaping) and will not cause a noticeable image signal. Simulations were carried out using different capacitor mismatches to verify the above argument. A path mismatch of 5 % in the second stage will produce an image 45 dB below full scale. However, mismatch in the first stage of the modulator is critical and must be avoided.

A path mismatch of 1 % on the input in the first stage of the modulator will produce an image signal which is only 40 dB below the signal. Figure 4.29 shows the output spectrum of the modulator with a capacitor mismatch of 1 % between the input sampling capacitors (during ϕ_1 and ϕ_2). Using layout techniques such as common-centroid, good

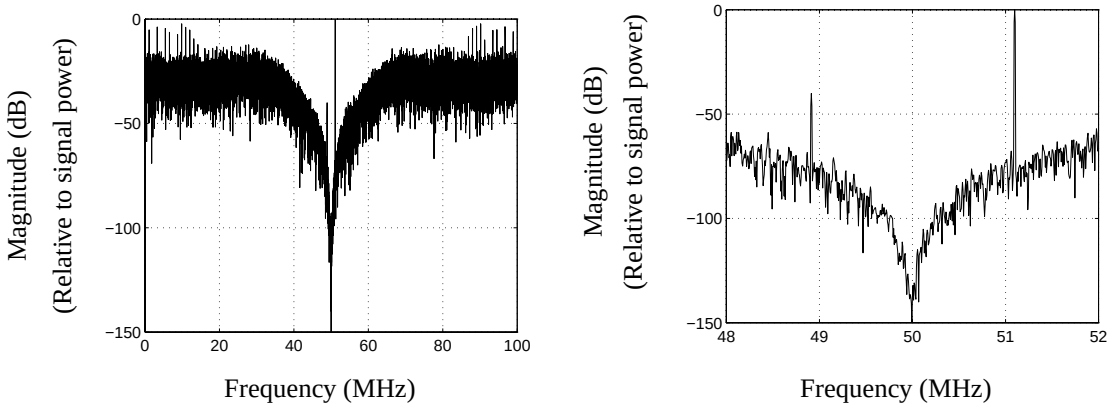


Figure 4.29: Output spectrum of the double-sampled bandpass sigma-delta modulator with 1% capacitor mismatch between the two paths. Note that the image power is 40 dB below the signal power.

capacitor matching—in the order of 0.1 %—can be achieved. A capacitor mismatch of 0.1 % will reduce the power of image signal to about 60 dB below the signal power. This kind of accuracy, ten bits, is acceptable for some high-speed wide-band applications, such as cable modems and PCS basestations.

Other methods of overcoming mismatch error, which have previously been applied to lowpass ΣΔ modulators, include a four-phase clocking scheme proposed by Ribner

[Ribner91], a switching scheme that converts the capacitive mismatch into an additive out of band noise [Hurst92] [Burmas95], and a method of using bilinear integrator [Yang94].

Finite Opamp Gain

Finite opamp gain causes both phase and gain errors in the ideal transfer function of a double-sampled resonator. The resonant frequency of the double-sampled SC resonator due to finite opamp gain is shifted by an angle θ_{dR0} from the $j\omega$-axis. If the same opamp is used in both delay cells and $C_{S1} = C_{S2} = C_S$, using (4-83) the phase error in the location of the poles of the double-sampled SC resonator is

$$\theta_{dR0} = \frac{C_{in}}{C_S} \cdot \frac{1}{A}. \qquad (4\text{-}84)$$

Thus, increasing the opamp DC gain and/or reducing the opamp input capacitance reduces the phase error. The frequency of the notch filter (for noise transfer function) will be shifted by Δf where

$$\Delta f = \frac{2 f_s}{2\pi} \cdot \theta_{dR0} = \frac{C_{in}}{C_S} \cdot \frac{OSR}{A} \cdot \frac{2BW}{\pi}. \qquad (4\text{-}85)$$

In a fourth-order bandpass ΣΔ modulator, the quantization noise slope is 15 dB/octave, reaching its minimum at the resonant frequency. If the resonant frequency is shifted by Δf, the in-band noise will be increased by approximately

$$\Delta S_B = \frac{15}{(BW)/2} \cdot \Delta f = \frac{60}{\pi} \cdot \frac{C_{in}}{C_S} \cdot \frac{OSR}{A}. \qquad (4\text{-}86)$$

For a 1.5 dB penalty in SNR, the opamp gain must be larger than the oversampling ratio by a factor of 12.7 (about 22 dB), if the input capacitance of the opamp is equal to the sampling capacitor.

Noise

The RC thermal noise associated with the different capacitors and switches in a double-sampled ΣΔ is less than the simple SC ΣΔ modulator because fewer capacitors are involved. Using the result of noise analysis in section 4.2, the total input referred thermal

noise associated with switches and opamp in a fully differential double-sampled SC ΣΔ modulator is

$$\bar{v}_{nT}^2 = \frac{17.8kT}{C_u}. \qquad (4\text{-}87)$$

Compared to the total noise of a simple SC bandpass ΣΔ modulator, this is smaller by a factor of 1.65 times. The in-band input referred thermal noise will be

$$\bar{v}_{nT}^2 = \frac{17.8}{OSR} \cdot \frac{kT}{C_u}. \qquad (4\text{-}88)$$

4.6 Implementation

Fourth-order bandpass ΣΔ modulators in Figure 4.21 and Figure 4.27 were designed and fabricated in a 0.5 μm double-poly CMOS process (HCMOS5a from SGS-Thomson). Chip microphotographs of the simple SC bandpass and the double-sampled bandpass modulator are shown in Figure 4.30 and Figure 4.31 respectively. The active chip area of both modulators is about 1.1 mm^2.

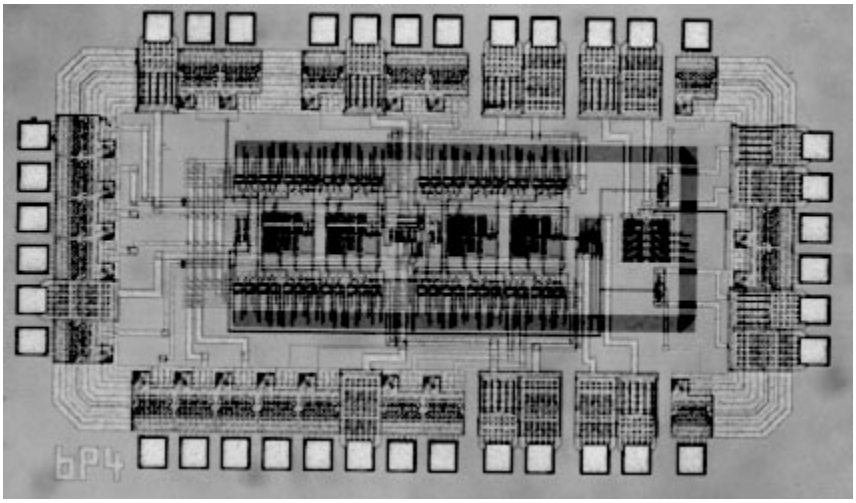


Figure 4.30: Chip microphotograph of the fourth-order SC bandpass sigma-delta modulator

HCMOS5a technology offers MOSFETs with a channel length of 0.5 μm and a high quality poly-to-poly capacitor, with a capacitance per unit area of 1.1 $fF/\mu m^2$. Some

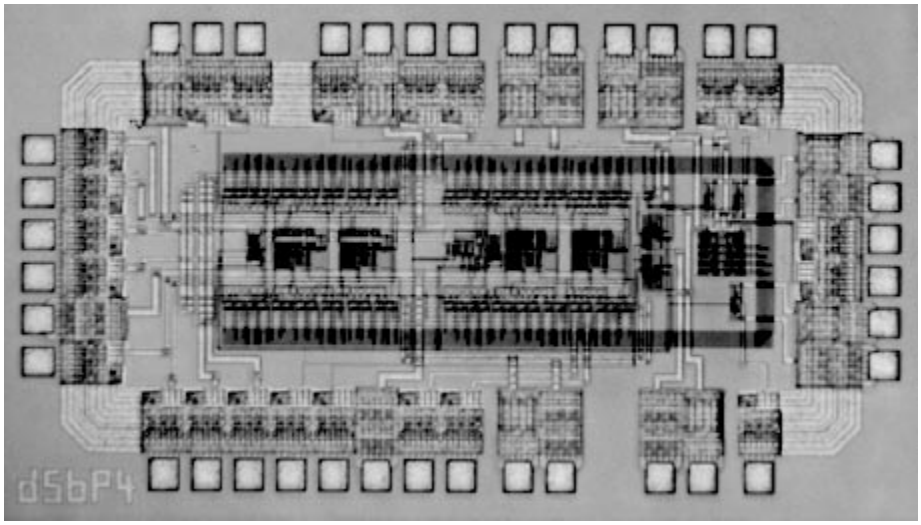


Figure 4.31: Chip microphotograph of the fourth-order double-sampled SC bandpass sigma-delta modulator

MOSFET parameters in this technology are listed in Table 4.1.

Parameters	*nMOSFET*	*pMOSFET*
Vt (10 μm/0.5 μm)	*600* mV	*600* mV
Isat (@ Vg=Vd=3.3 V*)*	*0.33* mA/μm	*0.15* mA/μm
μC_{ox}	*120* μA/V^2	*31* μA/V^2

Table 4.1: Some MOSFET parameters in HCMOS5a process

The main objective of the design was to demonstrate high-speed SC capabilities in submicron CMOS technologies. In [Singor94], it is shown that SC circuits operating at 40 MHz are feasible in a 0.8 μm BiCMOS process. Here, the target clock frequency was set to be 80 MHz. Therefore the IF frequency was at 20 MHz.

An interesting application of the bandpass ΣΔ modulator is in A/D conversion of narrow-band (200 kHz - 1 MHz) signals in high-speed RF modems. The required dynamic range of these A/D converter depends on the specific system architecture. Typically, a SNDR of about 60 dB is needed.

The target specification for the bandpass ΣΔ modulator is given in Table 4.2.

Parameter	Specification
IF frequency	20 MHz
Bandwidth	1 MHz
SNDR	~ 60 dB
Power	< 100 mW

Table 4.2: Target specification for the bandpass ΣΔ modulator

The oversampling ratio of this modulator is 40. An ideal fourth-order bandpass ΣΔ modulator with an OSR of 40 can achieve a maximum SNR of 62 dB.

To achieve high speed at moderate power, the unit capacitors are chosen to be as low as 300 fF. The total in-band kT/C noise of the single-sampled modulator (4-78) with $OSR = 40$ is calculated to be less than -76 dB relative to a 2 V peak-to-peak signal. In the following, the design of switches, opamp, and comparator circuits is described.

Switch Design

In stray insensitive SC circuits, typically the signal is sampled on a capacitor by means of two turned-on MOSFET switches. For example in the SC amplifier of Figure 4.5a, during ϕ_1 the input is sampled on C_s through $S1$ and $S2$ switches. The on-resistance of the switches along with the sampling capacitor constitutes an RC circuit. The sampled signal on C_s has the following exponential behavior:

$$v_{C_s} = v_{ip}(1 - e^{-t/RC_s}) . \qquad (4\text{-}89)$$

Therefore, at the end of the sampling phase ($t = T_s/2$), the input voltage is sampled on C_s with a settling error given by the term in the parentheses of (4-89). For a 0.1 % settling error in 4.5 ns (the sampling period), the on-resistance of each MOSFET switch must be less than $560\ \Omega$. For a better fixed charge cancellation, equal size pMOSFET and nMOSFET switches are utilized. Eldo simulations were carried out to find the exact value of the MOSFET aspect ratios. Figure 4.32 shows the simulated on-resistance of a parallel nMOSFET and pMOSFET switches with $W/L = 40\ \mu m / 0.5\ \mu m$. The worst case on-resistance is about $333\ \Omega$.

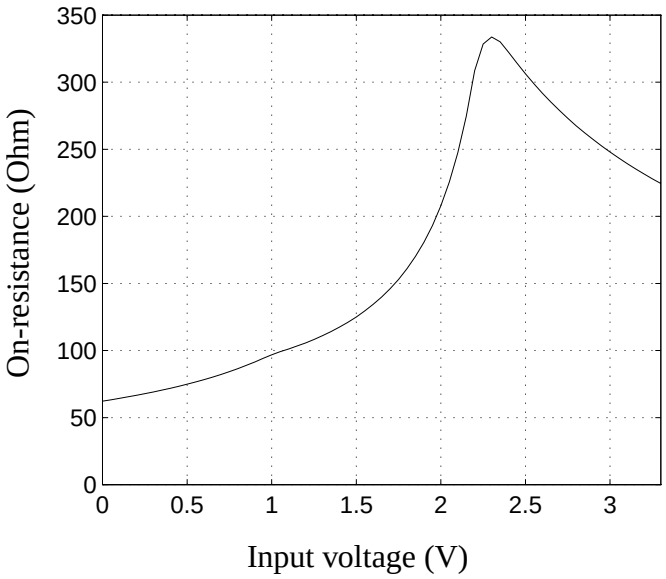


Figure 4.32: Transmission gate switch on-resistance vs. signal level

Operational Transconductance Amplifier Design

For high-speed SC operation, the unity gain frequency of the opamp must be 5 to 10 times greater than the clock frequency [Gregorian86]. For a $0.1\,\%$ settling error in half a clock period, the unity gain frequency of the opamp (with the worst case capacitive load) must be 7 times greater than the clock frequency. The worst case opamp load in our design is about $1\ \text{pF}$. Thus, for $80\ \text{MHz}$ clock frequency the unity-gain frequency of the opamp driving a $1\ \text{pF}$ load must be greater than $560\ \text{MHz}$.

The required DC gain of the opamp depends on the oversampling ratio of the modulator. In section 4.4.1, it was shown that for a $3\ \text{dB}$ penalty in SNR at an oversampling ratio of 40, the opamp DC gain must be at least $53\ \text{dB}$.

For large input signals, slewing response of the opamp determines the maximum speed of operation. During the non-overlapping phase, the opamp is in an open-loop configuration and its output levels are typically clipped to a voltage close to the rails. A fast slew rate of $1\ \text{V/ns}$ is chosen to bring the output voltages quickly to the workable levels of $1.4\ \text{V}$ and $2.4\ \text{V}$. For the worst case opamp load of $1\ \text{pF}$, a bias current of $1\ \text{mA}$ at each output stage is required.

A single stage cascode opamp (also called a telescopic opamp [Senderow94]) is used to

achieve the high speed and adequate DC gain needed for the opamp. The schematic of a fully differential cascode opamp designed to fulfill these requirements is shown in Figure 4.33. A continuous time common-mode feedback circuit sets the output common mode to the desired value. Resistors in the common-mode feedback circuit have a high value of $68\ \text{k}\Omega$ to ensure the opamp DC gain does not drop below $54\ \text{dB}$. The capacitors in the common mode feedback circuit have a value of $400\ \text{fF}$.

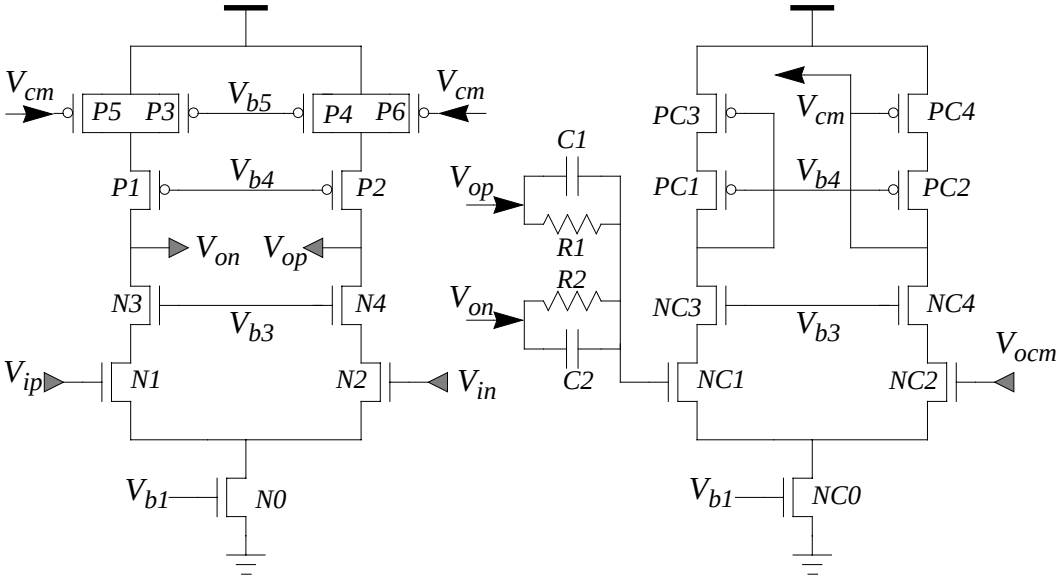


Figure 4.33: Fully differential cascode opamp

Dimensions of all the transistors used in the opamp are listed in Table 4.3, and transistor sizes for the common mode feedback are given in Table 4.4.

MOSFET	*N0*	*N1*	*N2*	*N3*	*N4*	*P1*	*P2*	*P3*	*P4*	*P5*	*P6*
W (μm)	*400*	*200*	*200*	*200*	*200*	*360*	*360*	*240*	*240*	*120*	*120*
L (μm)	*0.7*	*0.5*	*0.5*	*0.7*	*0.7*	*0.7*	*0.7*	*0.7*	*0.7*	*0.7*	*0.7*

Table 4.3: Transistors sizes used in the opamp

MOSFETs	*NC0*	*NC1*	*NC2*	*PC1*	*PC2*	*PC3*	*PC4*
W (μm)	*133*	*80*	*80*	*120*	*120*	*120*	*120*
L (μm)	*0.7*	*0.5*	*0.5*	*0.7*	*0.7*	*0.7*	*0.7*

Table 4.4: Transistor sizes used in the CMFB circuit

This opamp was simulated in Eldo using SPICE level 3 MOSFET models. Output conductance of transistors is poorly modeled in SPICE level 3 models. Therefore, simulations typically predict an optimistically high DC gain for the opamp. A safety margin of 12 dB was added to the required simulated opamp DC gain (not including the loading by resistor divider in the CMFB circuit) because of this modelling error. The

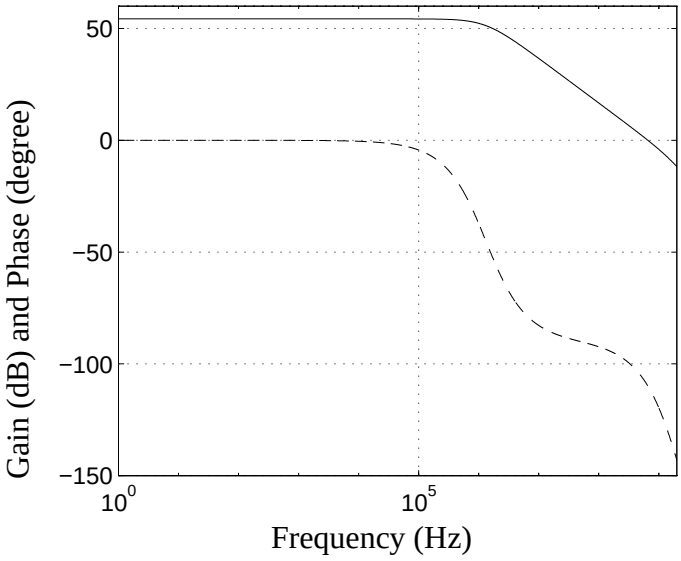


Figure 4.34: Simulated open loop gain (solid line) and phase (dotted line) of the cascode opamp for 1 pF load capacitance

opamp was simulated by itself and the DC gain was about 66 dB. The resistor divider in the CMFB circuit reduces the DC gain to 54 dB.

Simulated characteristics of the complete opamp at 3.3V power supply, 2 mA bias current and 1 pF output load are summarized in Table 4.5.

The settling time of the delay circuit was simulated in Eldo using the schematic of Figure 4.35. In the modulator of Figure 4.21, the worst case settling time happens when $C_S = 2C_u$, $C_H = C_u$, and $C_L = C_u$. Settling time to 0.1% of the full scale in this configuration is about 4.9 ns, as shown in Figure 4.36.

Comparator

In a ΣΔ modulator circuit, the required specification of the comparator is relatively easy to achieve. The comparator hysteresis can be modelled as an additive white noise at the input

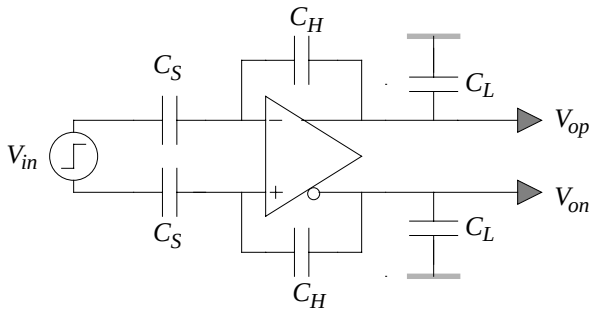


Figure 4.35: Test structure for settling time simulation

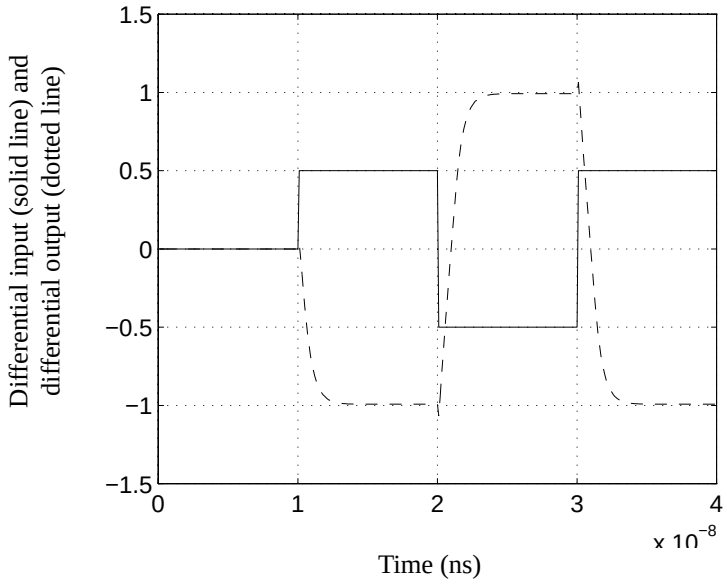


Figure 4.36: Worst case settling time simulation in Eldo.

of the comparator. Both the input referred noise and comparator hysteresis are noise-shaped (similarly to quantization noise) by the feedback loop and will be band-rejected around the center frequency ($f_s/4$). Eldo SC simulations of the fourth-order ΣΔ modulators show that for a hysteresis voltage of 10 % of the full scale (reference levels), the in-band noise power is increased by about 1.5 dB.

The schematic of a fully differential comparator used in the design of both modulators is shown in Figure 4.37. The first stage is a preamplifier with a gain of 22 dB and a unity gain bandwidth of 650 MHz. The second stage is a cross-coupled latch reset by $N5$. Gain and unity gain bandwidth of the second stage are 28 dB and 620 MHz respectively. This

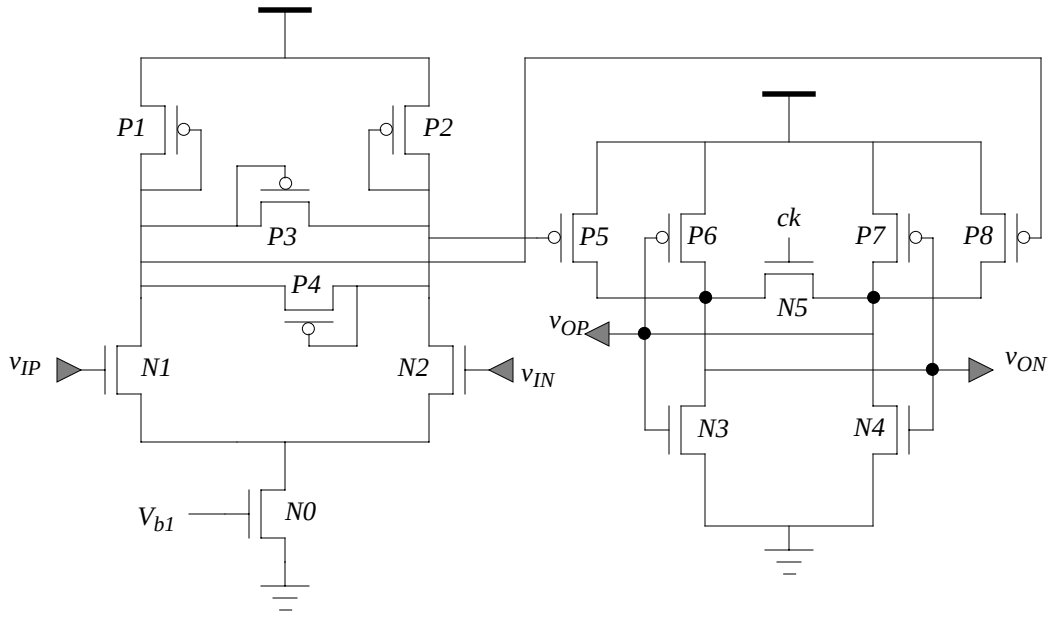


Figure 4.37: Fully differential comparator

Parameter	Value
DC gain	54 dB
Unity gain frequency	650 MHz
Phase Margin	70°
Slew rate	1000 V/μs
Differential Output swing	2 V
Power dissipation (including CMFB circuit)	8.8 mW

Table 4.5: Simulated characteristics of opamp for 1 pF load capacitance

comparator is followed by a cross-coupled NAND latch.

The transistor dimensions in this circuit are listed in Table 4.6.

In both fourth-order bandpass ΣΔ modulators, this comparator is followed by a latch. Thus, the outputs of the comparator have to drive a single logic gate with an input capacitance of 25 fF. For a 2 mV differential input signal, the delay time (clock going

MOSFET	N0	N1	N2	N3	N4	N5	P1	P2	P3	P4	P5	P6	P7	P8
W (μm)	200	200	200	4	4	8	50	50	50	50	10	1.2	1.2	10
L (μm)	1	0.5	0.5	1	1	0.5	2	2	2	2	0.5	1	1	0.5

Table 4.6: Comparator transistor sizes

low and output becoming ready) of the comparator driving 50 fF capacitor loads is about 2 ns. The power consumption of the comparator at 3.3 V is about 3 mW.

4.7 Measurement Results

This section describes measured results for the fourth-order bandpass ΣΔ modulator and the double-sampled fourth-order bandpass ΣΔ modulator. Both modulators were packaged in a 60-pin high speed metal package and were tested separately. A PCB was designed for testing the modulator. All the reference voltages, and reference currents needed for the modulators were generated on the PCB board using voltage regulators and resistors.

4.7.1 Fourth-Order Bandpass Sigma-Delta Modulator

The fourth-order SC bandpass ΣΔ modulator was tested at a clock frequency of 80 MHz using a supply voltage of 3.3V. Measured output spectrum for this modulator for a 20.1 MHz sinusoid signal, with an amplitude of 10 dB below full scale, is shown in Figure 4.38.

This output spectrum is generated in Matlab, by performing an FFT on 65536 bits of the modulator output captured by a logic analyzer. Measured maximum SNR for this modulator is 42 dB in a bandwidth of 1 MHz. This value is 20 dB less than the expected theoretical value of 62 dB.

Such a low SNR can be caused by a number of circuit imperfections, including capacitor mismatch and low opamp gain. In this process, poly-poly capacitors have good matching properties and 300 fF unit capacitors used in this modulator are expected to match within 1%. For an oversampling ratio of 40, this capacitor mismatch reduces the SNR by only $1-2$ dB.

Unfortunately, a stand alone opamp circuit was not included in the test chip due to the

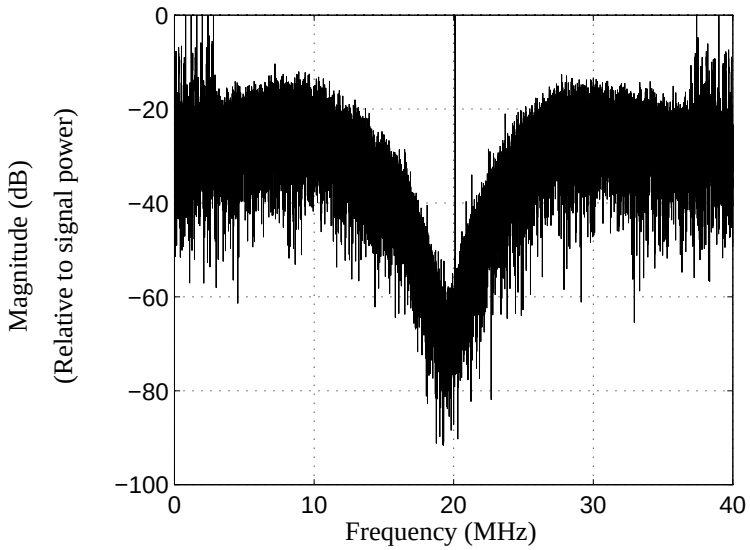


Figure 4.38: Measured output spectrum of the fourth-order bandpass sigma-delta modulator for an input signal of 10 dB below full scale.

limited chip area available. Therefore, opamp gain can not be measured by itself. Four indirect methods used to estimate the opamp gain consistently indicate a low DC gain of about $40 - 46$ dB.

First, the output conductances of a number of 0.7 μm MOSFETs were measured. The measured output conductance was typically lower than the simulated value by a factor of 3 to 3.5. Since a cascode architecture is employed in this opamp, the DC gain of the amplifier is reduced by about 20 dB (DC gain is proportional to r_o^2). The estimated opamp DC gain is 46 dB.

Second, expanding the view of the output spectrum around the resonant frequency indicates that the notch is shifted by about 500 kHz, as shown in Figure 4.39.

In section 4.4.1, it was shown that a low opamp gain can cause a shift in the notch frequency. For a bandwidth of 1 MHz, the shift in notch frequency is $BW/2$, and thus according to (4-72), SNR is reduced by at least 15 dB. Using equation (4-73), the opamp gain is estimated to be 40 dB.

Third, a low opamp gain reduces the gain of the resonator. Using equation (4-76) and $A = 40$ dB, the gain of the resonator at resonance is about $H_{R0} = 6.25$. For an

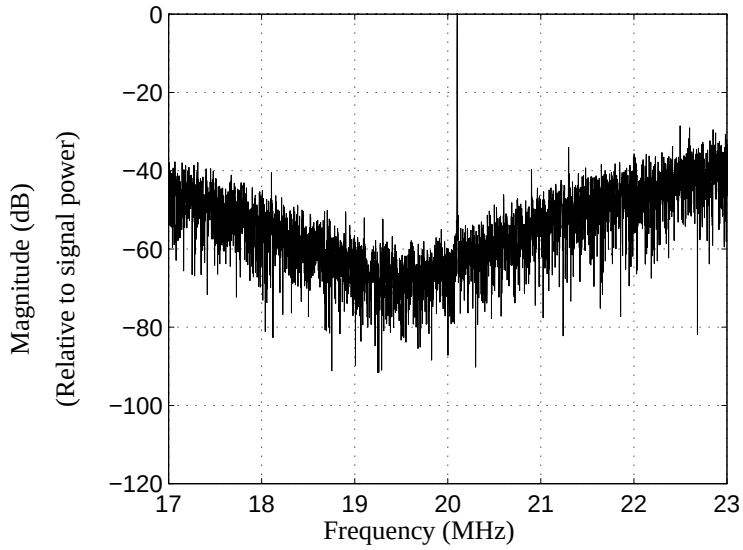


Figure 4.39: Expanded view of the output spectrum around the notch. Note that the notch frequency is shifted by about 500 kHz to the left (lower frequency)

oversampling ratio of 40, the ratio of the oversampling ratio to resonator gain is $(OSR)/H_{R0} = 6.4$. From Figure 4.25, in-band quantization noise increases by about 20 dB. That is in agreement with the measured SNR of 42 dB which is 20 dB lower than the expected 62 dB.

The fourth method of estimating the opamp gain indicates an opamp gain of 40 dB and is discussed in the next section.

4.7.2 Double-Sampled Fourth-Order SC Bandpass Sigma-Delta Modulator

The double-sampled bandpass SC ΣΔ modulator was tested at a clock frequency of 80 MHz. Thus, the effective sampling rate is 160 MHz. Figure 4.40 shows the output spectrum of the modulator for an input sinusoid at 40.8 MHz with an amplitude of 6 dB below full scale.

The output bit-stream was captured by a logic analyzer for 16384 clock cycles. In Matlab, a 16384-point FFT was carried out to compute the output spectrum. The image signal is at 39.2 MHz and is 39 dB below the signal. This suggests that the capacitor mismatch is about 1 %. The SNDR of this modulator is limited to 30 dB for a 5 MHz bandwidth.

Just as for the simple SC modulator, low opamp gain has shifted the notch frequency to a

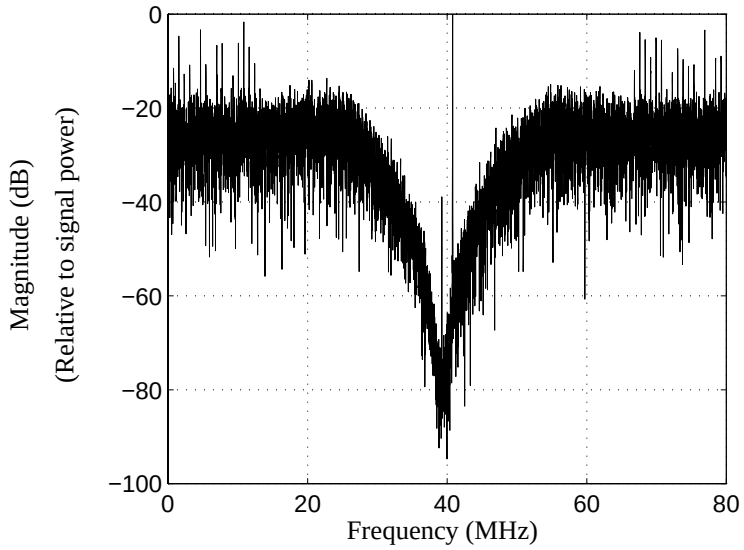


Figure 4.40: Measured output spectrum of the double-sampled fourth-order SC bandpass sigma-delta modulator for an input signal of 10 dB below full scale. Note that image signal is about 39 dB below the fundamental signal.

lower value than the expected 40 MHz. Figure 4.41 illustrates an expanded view of the output spectrum around 40 MHz.

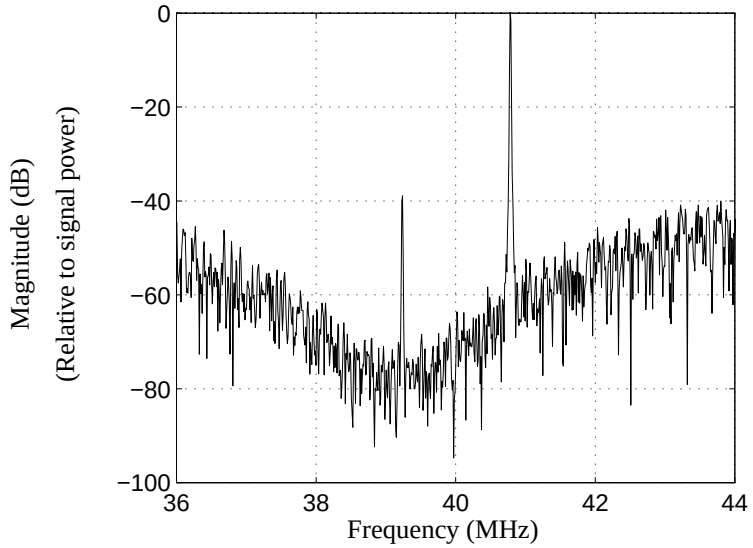


Figure 4.41: Expanded view of the output spectrum around the notch. Note that the notch frequency is shifted by about 1 MHz.

As we can observe in Figure 4.41, the notch frequency of the modulator is shifted to about $39\ \text{MHz}$, which is $1\ \text{MHz}$ below the expected value of $40\ \text{MHz}$.

Using equation (4-84), the opamp DC gain is calculated to be $40\ \text{dB}$. This is consistent with the estimated opamp DC gain obtained in the previous section.

4.8 Summary

This chapter considered a z-domain architecture for a fourth-order bandpass $\Sigma\Delta$ modulator. This modulator is a direct map of a second-order lowpass $\Sigma\Delta$ modulator to bandpass by transforming integrators to resonators.

In SC technology, an efficient method of implementing a resonator is to use two delay cells in a negative feedback loop. Half delay and full delay SC circuits were described and impacts of circuit non-idealities on the performance of these circuits were analyzed. Specifically, it was shown that finite opamp gain causes both a gain error and a phase error in the operation of a SC delay circuit. In a SC resonator, finite opamp gain causes a change in the resonant frequency.

Two fourth-order SC bandpass $\Sigma\Delta$ modulators were presented. The first one is a single-sampled SC circuit and is shown to be faster than a previously reported one. The second is a double-sampled SC circuit. Results of Eldo simulations for these modulators were presented.

Finally, the two bandpass modulators were designed and fabricated in a $0.5\ \mu\text{m}$ CMOS process. Both modulators operate at a clock frequency of $80\ \text{MHz}$. The SNR of the single-sampled modulator is $42\ \text{dB}$ in the bandwidth of $1\ \text{MHz}$. This is about $20\ \text{dB}$ less than the expected value of $62\ \text{dB}$. A low opamp DC gain appears to be responsible for the reduced SNR. Three indirect methods of estimating the opamp DC gain indicate a low opamp DC gain of $40\ \text{dB}$ to $46\ \text{dB}$. A SC amplifier circuit that is insensitive to low opamp gain such as [Martin87], would be a better choice for the next implementation. The double-sampled modulator exhibits an image signal as low as $-40\ \text{dB}$ relative to the signal. This is probably caused by capacitor mismatch in the first stage.

Chapter 5

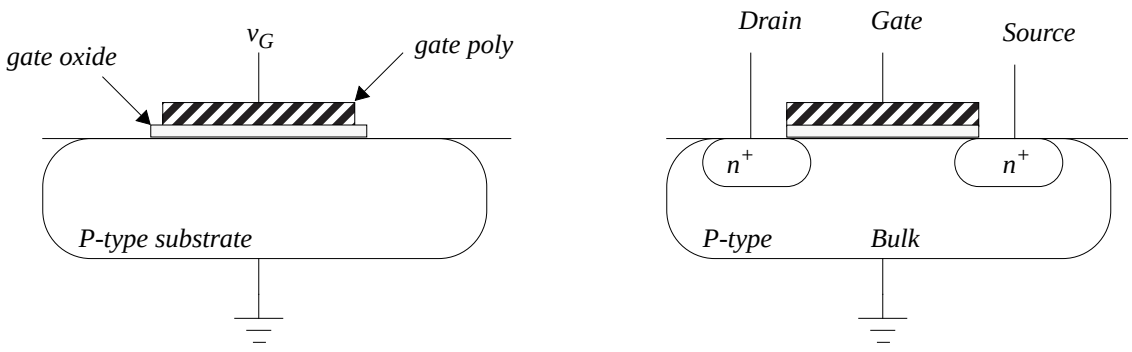
SC Bandpass Sigma-Delta Modulator Design In a Digital CMOS Process

As we discussed in Chapter 2, to be cost effective it is desirable to implement analog SC circuits in standard digital CMOS processes where linear poly-to-poly capacitors are not available. In a single-poly process, a relatively low specific value linear capacitor is formed using poly and metal as electrodes and field oxide as insulator. Another option is to use MOSFET gate capacitors in the strong inversion or accumulation regime.

In this chapter, the linearity of MOSFET gate capacitors in strong inversion and accumulation is studied first. Measured CV-plots in a 0.5 μm CMOS technology will show that MOSFETs biased in strong inversion are more linear than MOSFETs biased in the accumulation regime due to a gate-poly depletion effect. Distortion caused by non-linearity of capacitors in a SC amplifier is then analyzed and some simulation results are presented. Finally, the design of a fourth-order bandpass ΣΔ modulator, using a pMOSFET transistor as a linear capacitor, is described.

5.1 MOS Capacitor

A MOS capacitor uses polysilicon and semiconductor as the two parallel plates and silicon dioxide as insulator. In a CMOS process, gate poly and device well are used as electrodes and the thin gate oxide serves as the insulating layer. Figure 5.1a shows the structure of a MOS capacitor with p-well as the bottom plate. A MOSFET transistor is made by adding source and drain to the sides of the MOS capacitor, as shown in Figure 5.1b.



(a) (b)

Figure 5.1: Structure of (a) a MOS capacitor and (b) an nMOSFET transistor

MOS capacitance is dependent on the gate to bulk voltage and is strongly non-linear. For a negative gate voltage $v_G < 0$, holes will be attracted to the surface (Si-SiO_2 interface) of the p-type semiconductor. This mode is called accumulation and the MOS capacitor resembles a parallel plate capacitor with a capacitance per unit area of

$$C_{GB} = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad (5\text{-}1)$$

where ε_{ox} is the oxide dielectric constant and t_{ox} is the oxide thickness. When the applied gate voltage is $0 < v_G < V_t$, the holes are repelled from the surface and a negative depletion layer is formed near the surface. In this regime, called depletion, the MOS capacitor has two dielectrics (the gate oxide and the depleted silicon) in series. Thus, the MOS capacitance in depletion mode is given by the series combination of the gate capacitance (C_{ox}) and the depletion capacitance,

$$C_{GB} = \left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{d}{\varepsilon_{si}}\right)^{-1} . \qquad (5\text{-}2)$$

Here, ε_{si} is the semiconductor dielectric constant and d is the depletion layer width. As gate voltage is increased, the depletion layer width increases and hence the gate to bulk capacitance decreases.

If the gate voltage is increased beyond the threshold voltage $v_G > V_t$, the concentration of attracted electrons at the surface will be greater than the concentration of the holes at the

surface. This condition is called strong inversion. The inversion layer below the oxide provides the bottom plate of the capacitor, and the gate to bulk capacitance is given by the oxide capacitance (C_{ox}). In the two-terminal MOS capacitor, the inversion layer is formed by the thermal generation of carriers, which is a slow process. In a MOSFET capacitor, the source terminal will provide carriers for the formation of the inversion layer. Thus, the characteristic of a MOSFET capacitor at high frequency will be the same as the low frequency C-V characteristic of the two-terminal MOS capacitor.

The theoretical C-V characteristic of an nMOSFET, using analytical results in [Tsividis87], is shown in Figure 5.2.

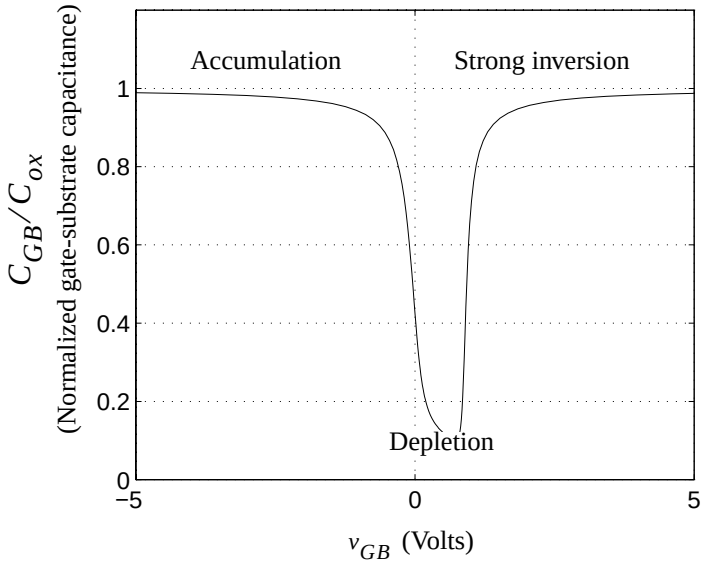


Figure 5.2: Analytical C-V characteristics of an nMOSFET transistor

As we can observe in the C-V plot, Figure 5.2, the MOSFET capacitance is relatively linear (or weakly non-linear) in the accumulation and strong inversion regimes.

The capacitance of a voltage-dependent non-linear capacitor can be expressed in Taylor series form by

$$C(v) = C_0(1 + \alpha_1 v + \alpha_2 v^2 + \ldots) \ . \qquad (5\text{-}3)$$

Typically, voltage coefficients of the cubic and higher terms are small and the capacitance can be approximated by the first three terms in equation (5-3).

The voltage coefficients of a MOSFET capacitance in strong inversion are given by [Behr92]

$$\alpha_1 = -\frac{2\phi_t}{\left|V_R - V_t\right|^2} \qquad (5\text{-}4)$$

and

$$\alpha_2 = \frac{2\phi_t}{\left|V_R - V_t\right|^3}. \qquad (5\text{-}5)$$

Here, ϕ_t is the thermal voltage and V_R is the bias voltage. In accumulation, the voltage coefficients are given by similar expressions with V_t being substituted with the flat-band voltage (V_{FB}). Therefore, the non-linearity of the MOSFET capacitor in strong inversion and accumulation regions are theoretically almost identical.

In the above analysis, it is assumed that the poly gate is degenerately doped. In some advanced processes, the poly gate is doped along with the source and drain diffusion. In this case, the gate is not doped degenerately. A positive voltage on the gate electrode will pull the electrons in the polysilicon to the top, and the bottom of the poly gate will be depleted. Therefore, the effective dielectric thickness of the capacitor will increase. This phenomenon, known as “poly depletion,” will cause a slight roll-off in the C-V curve in the strong inversion region near the supply voltage.

Figure 5.3 illustrates C-V characteristics for an nMOSFET transistor in a 0.5 μm CMOS technology obtained from silicon measurement (solid line) and simulation (dashed line) using the MISNAN model. Note the negative slope in strong inversion of the measured (solid line) C-V curves. As we can observe in this figure, poly-depletion is not modelled by MISNAN and linearity of a MOSFET in the accumulation regime is optimistically predicted to be high. Similarly, linearity of a MOSFET in the strong inversion regime is predicted pessimistically to be low by the MISNAN model. Gate-poly depletion appears to largely compensate the non-linearity of MOSFET capacitors in the strong inversion regime.

The C-V characteristic of pMOSFET is shown in Figure 5.4.

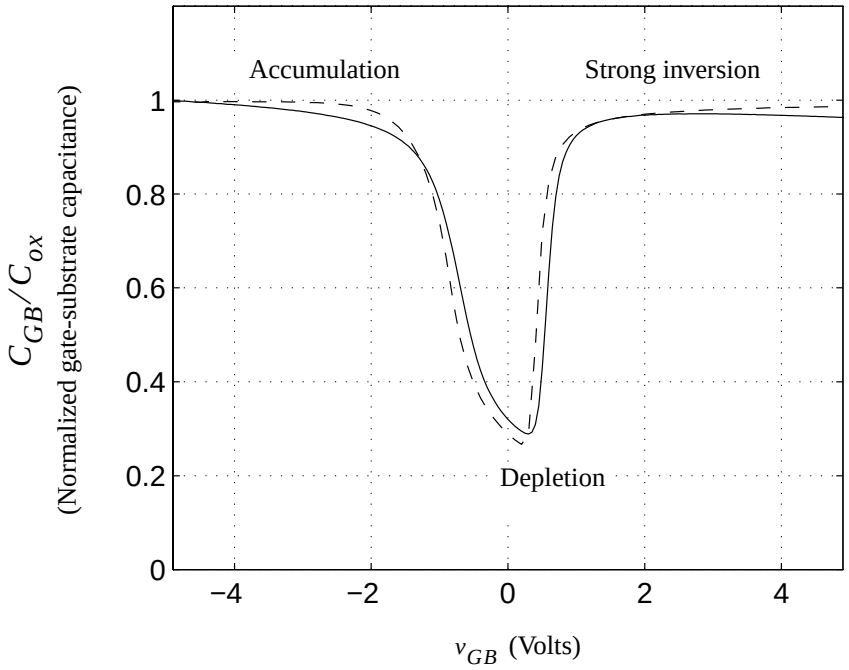


Figure 5.3: Measured (solid line) and simulated (dashed line) C-V plot of an nMOSFET

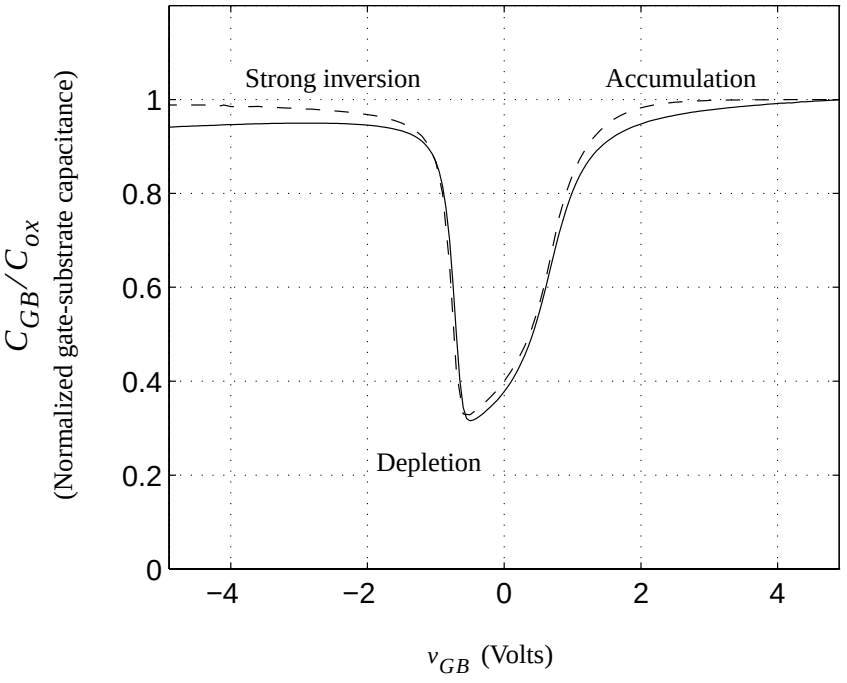


Figure 5.4: Measured (solid line) and simulated (dashed line) C-V plot of a pMOSFET

Both nMOSFET and pMOSFET are strongly non-linear in the $-2\ \text{V} < v_{GB} < 2\ \text{V}$ range and only weakly non-linear when MOSFETs are biased by more than $2\ \text{V}$ in either accumulation or strong inversion regimes. From the measured C-V plots, we can see that both MOSFETs exhibit a better linearity in the strong inversion regime than in the accumulation regime. This has been verified in Matlab and will be discussed below.

Using the *polyfit* feature in Matlab (least squares algorithm), the first (α_1) and second (α_2) order voltage coefficients of measured MOSFET capacitance are found for different ranges of v_{GS}. Table 5.1 and Table 5.2 summarize the results for the nMOSFET and pMOSFET transistors respectively.

Condition	Measured		Simulated	
	$\alpha_1(V^{-1})$	$\alpha_2(V^{-2})$	$\alpha_1(V^{-1})$	$\alpha_2(V^{-2})$
Strong Inversion ($2\ \text{V} < v_{GS} < 3\ \text{V}$)	0.0279	0.0050	0.0327	0.0045
Accumulation ($-3\ \text{V} < v_{GS} < -2\ \text{V}$)	0.125	0.0177	0.1457	0.0251
Strong Inversion ($3\ \text{V} < v_{GS} < 4\ \text{V}$)	0.005	0.0012	0.0162	0.0016
Accumulation ($-4\ \text{V} < v_{GS} < -3\ \text{V}$)	0.045	0.0049	0.0114	0.0014

Table 5.1: nMOSFET capacitance voltage coefficients

Condition	Measured		Simulated	
	$\alpha_1(V^{-1})$	$\alpha_2(V^{-2})$	$\alpha_1(V^{-1})$	$\alpha_2(V^{-2})$
Strong Inversion ($-3\ \text{V} < v_{GS} < -2\ \text{V}$)	0.0427	0.0077	0.0534	0.0079
Accumulation ($2\ \text{V} < v_{GS} < 3\ \text{V}$)	0.1264	0.0180	0.1079	0.0182
Strong Inversion ($-4\ \text{V} < v_{GS} < -3\ \text{V}$)	0.0162	0.0027	0.0499	0.0064
Accumulation ($3\ \text{V} < v_{GS} < 4\ \text{V}$)	0.0403	0.0036	0.0134	0.0017

Table 5.2: pMOSFET capacitance voltage coefficients

For similar gate to substrate voltages, MOSFETs biased in strong inversion consistently have a significantly better linearity than MOSFETs operating in accumulation regime.

For low-voltage linear SC circuits, it is desirable to extend the linear portions of the C-V

curve closer to the $v_{GB} = 0$ axis, so that less bias voltage will be required to operate the MOSFET in the strong inversion (or accumulation) regime. Low-V_t natural MOSFETs are suited very well for this purpose. Due to their low threshold voltage, natural MOSFETs have a wider linear range in the strong inversion regime. Figure 5.5 shows the C-V plots for both a natural MOSFET and a threshold adjusted MOSFET transistor.

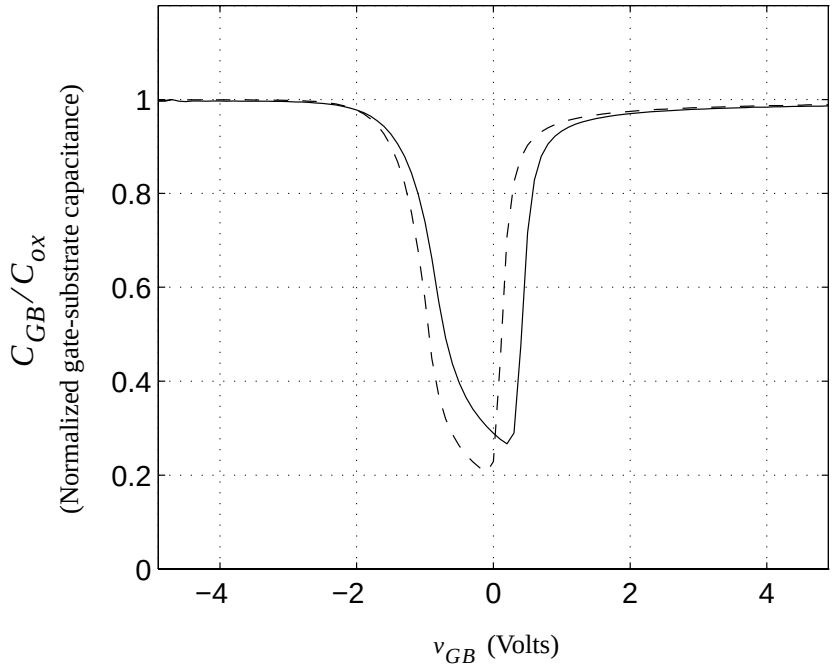


Figure 5.5: Simulated C-V characteristics of a low-V_t natural nMOSFET (dashed line) and a threshold adjusted nMOSFET (solid line)

Note that the linear range of natural nMOSFET capacitance is increased (compared to that of the threshold adjusted nMOSFET) in the strong inversion region at the expense of a reduced linear range in accumulation.

5.2 Distortion in SC Amplifier Caused by Non-linear Capacitors

Non-linear capacitors cause distortion in SC circuits. Consider a single-ended SC amplifier as shown in Figure 5.6. Capacitors are assumed to have a similar non-linearity and their capacitances are approximated by

$$C_S = C_{S0}(1 + \alpha_1 v + \alpha_2 v^2) \qquad (5\text{-}6)$$

and

$$C_H = C_{H0}(1 + \alpha_1 v + \alpha_2 v^2)\,. \qquad (5\text{-}7)$$

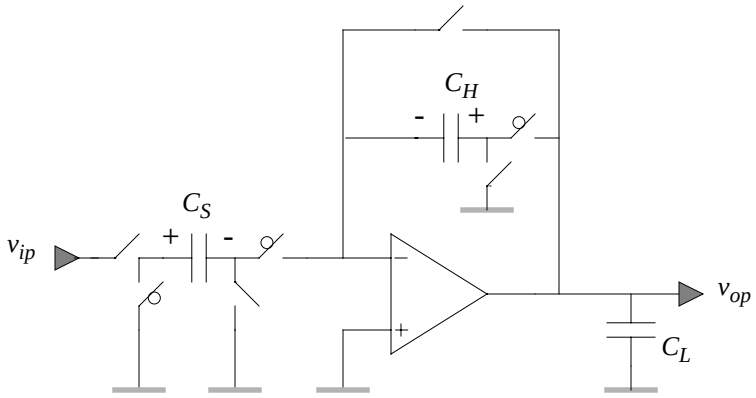


Figure 5.6: A single-ended SC amplifier

Assuming an ideal opamp, charge conservation on the sampling capacitor (C_S) and the holding capacitor (C_H) during ϕ_1 and ϕ_2 yields

$$v_{op}\left(n + \frac{1}{2}\right) = \frac{C_S}{C_H} \cdot v_{ip}(n)\ . \qquad (5\text{-}8)$$

If the capacitors are linear, the output of the SC amplifier is a scaled version of the input signal delayed by a half-clock period.

For non-linear capacitors, substituting (5-6) and (5-7) into (5-8), the above difference equation becomes

$$v_{op}\left(n + \frac{1}{2}\right) = \frac{C_{S0}}{C_{H0}} \cdot \frac{1 + \alpha_1 v_{ip}(n) + \alpha_2 v_{ip}^2(n)}{1 + \alpha_1 v_{op}(n + 1/2) + \alpha_2 v_{op}^2(n + 1/2)} \cdot v_{ip}(n)\quad . \qquad (5\text{-}9)$$

For $\alpha_1 \ll 1$ and $\alpha_2 \ll 1$, the input-output difference equation can be approximated by

$$v_{op}\left(n + \frac{1}{2}\right) = \frac{C_{S0}}{C_{H0}}\left\{v_{ip}(n) + \alpha_1\left[v_{ip}(n) - v_{op}\left(n + \frac{1}{2}\right)\right]v_{ip}(n) + \alpha_2\left[v_{ip}^2(n) - v_{op}^2\left(n + \frac{1}{2}\right)\right]v_{ip}(n)\right\} \quad . (5\text{-}10)$$

The above transfer characteristic indicates that a non-linear capacitor causes non-linear

errors at the output of the SC amplifier.

Let us assume that the input signal is a sampled sinusoid given by

$$v_{ip}(n) = V_{ip}\cos(n\omega T) \qquad (5\text{-}11)$$

If the non-linear coefficients are small, the output of the amplifier in the error terms of equation (5-10) can be approximated to the first order by the output of an ideal SC amplifier,

$$v_{op}\left(n+\frac{1}{2}\right) = \frac{C_{S0}}{C_{H0}} \cdot V_{ip}\cos(n\omega T)\ . \qquad (5\text{-}12)$$

Substituting (5-11) and (5-12) into (5-10) and using the following trigonometric identities

$$(\cos A)^2 = \frac{1+\cos 2A}{2} \qquad \text{and} \qquad (\cos A)^3 = \frac{3\cos A + \cos 3A}{4}\ , \qquad (5\text{-}13)$$

equation (5-10) becomes

$$v_{op}\left(n+\frac{1}{2}\right) = \frac{C_{S0}}{C_{H0}} \cdot \left\{ \frac{\alpha_1}{2}\left(1-\frac{C_{S0}}{C_{H0}}\right)V_{ip} + \left[1+\frac{3\alpha_2}{4}\left(1-\frac{C_{S0}^2}{C_{H0}^2}\right)V_{ip}^2\right]V_{ip}\cos(n\omega T) \right.$$
$$\left. + \frac{\alpha_1}{2}\left(1-\frac{C_{S0}}{C_{H0}}\right)V_{ip}^2\cos(2n\omega T) + \frac{\alpha_2}{4}\left(1-\frac{C_{S0}^2}{C_{H0}^2}\right)V_{ip}^3\cos(3n\omega T) \right\} \qquad (5\text{-}14)$$

The second term in the brace brackets on the RHS of the above equation is the output at the fundamental frequency. The first term is an offset, the third and fourth terms are the error terms containing the second and third harmonics of the signal. Using the following definition for k-th harmonics,

$$HD_k = \frac{\text{Signal Amplitude at } (k\omega)}{\text{Signal Amplitude at Fundamental } (\omega)} \qquad (5\text{-}15)$$

the second and third harmonics for the SC amplifier circuit are found to be approximately

$$HD_2 \approx \frac{\alpha_1}{2}\left(1-\frac{C_{S0}}{C_{H0}}\right)V_{ip} \qquad (5\text{-}16)$$

and

$$HD_3 \approx \frac{\alpha_2}{12}\left[1-\left(\frac{C_{S0}}{C_{H0}}\right)^2\right]V_{ip}^2 \ . \qquad (5\text{-}17)$$

In a fully differential circuit, the second harmonic component is rejected at the output.

Example 5.1: In the SC amplifier of Figure 5.6, the gain of the circuit is 0.5, opamp and switches are ideal, and capacitors are poly-poly capacitors with voltage coefficients of $\alpha_1 = 10$ ppm/V and $\alpha_2 = 10$ ppm/V^2. For a 2 V peak-to-peak input sinusoid, the second and the third harmonics are calculated from (5-16) and (5-17) respectively to be $HD_2 = -102.5$ dB and $HD_3 = -110$ dB. If capacitors are implemented with pMOSFETs in strong inversion with voltage coefficients of $\alpha_1 = 42$ kppm/V and $\alpha_2 = 7.7$ kppm/V^2, the distortions will be $HD_2 = -45.6$ dB and $HD_3 = -78.4$ dB for a 1 Vpp input signal.

5.3 A SC Delay Circuit Using pMOSFET Capacitors

In section 5.1, it was shown that pMOSFETs biased in strong inversion ($v_{GB} < |V_{tp}|$) exhibit a weakly non-linear behavior over a small gate-substrate voltage range. For instance, measured C-V characteristics show that for a 1 V signal swing in the range of $-3 \text{ V} < v_{GB} < -2 \text{ V}$, the voltage coefficients of the MOSFET capacitor are $\alpha_1 = 42$ kppm/V and $\alpha_2 = 7.7$ kppm/V^2. The schematic of a fully differential SC gain stage with unity gain during ϕ_1 and a gain of half during ϕ_2, using pMOSFET capacitors, is shown in Figure 5.7. The differential structure cancels even-order harmonics, reducing the importance of α_1.

Transistors $M1$ and $M3$ are equal size pMOSFETs and $M2$ is made of two pMOSFETs identical to $M1$. All pMOSFET capacitors are biased to operate in strong inversion by means of different input and output common mode voltages. The gates of the pMOSFETs are connected to the input common-mode level and the bulk terminals (which is shorted to the drain and the source) are connected to the (higher) output common-mode level. For a signal swing of v_{pp} with respect to V_{ocm}, the operating gate-to-substrate of the pMOSFET voltage is

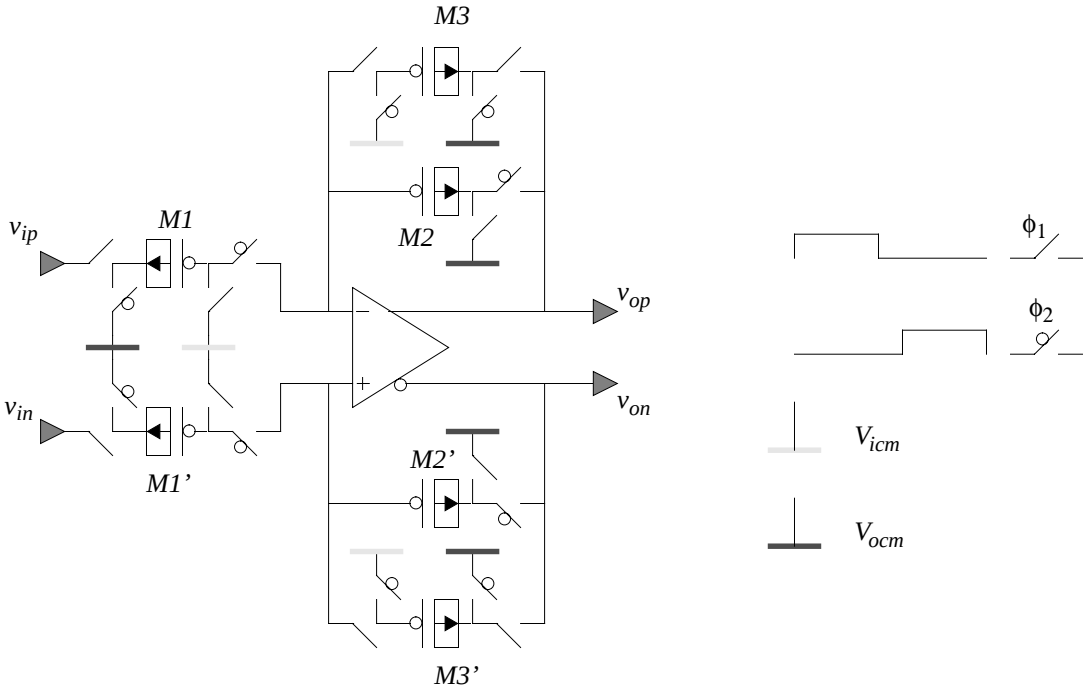


Figure 5.7: SC delay cell using pMOSFET capacitors

$$V_{icm}-\left(V_{ocm}+\frac{v_{pp}}{2}\right)<v_{GB}<V_{icm}-\left(V_{ocm}-\frac{v_{pp}}{2}\right). \qquad (5\text{-}18)$$

If the input common mode voltage is set to $1\ \text{V}$ and the output common-mode is set to $3.5\ \text{V}$, then with a $1\ \text{V}$ peak-to-peak signal the pMOSFET will operate in the strong inversion regime with a gate-to-bulk voltage of $-3\ \text{V} < v_{GB} < -2\ \text{V}$.

For a $1\ \text{Vpp}$ sinusoid input signal, the output signal will be $0.5\ \text{Vpp}$ during ϕ_2, with a delay of a half-clock period. Due to the weak non-linearity of the pMOSFETs in strong inversion, a third harmonic is also generated. The voltage coefficient α_2 that is responsible for the third harmonics was calculated (Table 5.1) to be $7.7\ \text{kppm/V}$ in the operating regime of $-3\ \text{V} < v_{GB} < -2\ \text{V}$. The third harmonic distortion is calculated from (5-17) to be $-78.4\ \text{dB}$.

This circuit was simulated in Eldo using an ideal opamp with a gain of $100\ \text{dB}$, ideal switches with an on-resistance of $1\ \Omega$, and a $W/L = 30\ \mu\text{m}/10\ \mu\text{m}$ pMOSFET as unit capacitor. The non-overlapping clock had a frequency of $100\ \text{MHz}$ and the input signal was a $1\ \text{Vpp}$ sinusoid with a frequency of $9.99\ \text{MHz}$. The output spectrum, Figure

5.8, has a tone at the input frequency (its fundamental frequency) and a third harmonic whose power is 80 dB below the output power at the fundamental frequency.

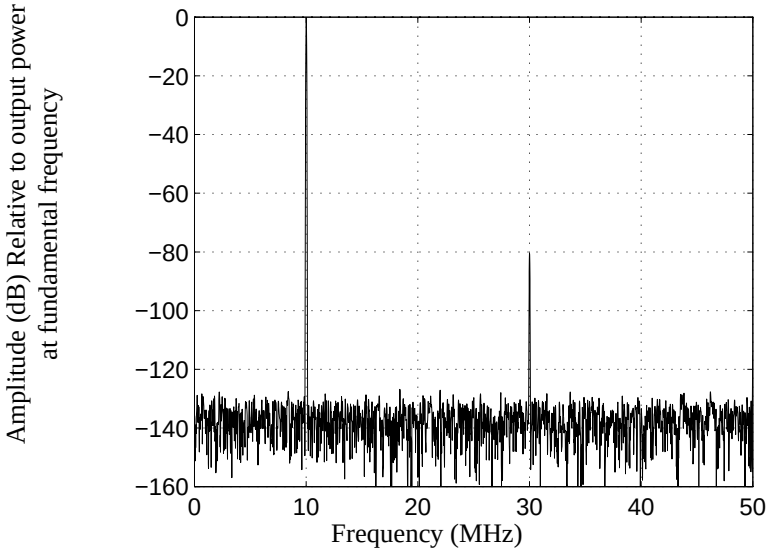


Figure 5.8: Output spectrum of the fully differential SC gain stage, Figure 5.7, during ϕ_2.

As we can see in Figure 5.8, no second harmonic is generated at the output due to fully differential implementation of this circuit. In a real implementation, mismatches and offsets would cause a non-zero HD_2.

During ϕ_1, the output is ideally an exact replica of the input delayed by a full clock period. Since the gate to source voltage of the pMOSFET capacitors $M1$ and $M3$ are the same, no distortion should appear at the output. This argument is verified by simulation and Figure 5.9 illustrates the output spectrum during ϕ_1.

5.4 A Fourth-Order SC Bandpass Sigma-Delta Modulator Using pMOSFET Capacitors

The fourth-order bandpass ΣΔ of Figure 4.21 can be implemented in a standard digital CMOS process by replacing all the poly-poly capacitors with pMOSFET capacitors. The modified schematic is shown in Figure 5.10, where pMOSFET capacitors are biased in strong inversion. In this circuit all the pMOSFET capacitors are identical with a gate area of WL, except for the two marked by asterisk which have a gate area of $2WL$.

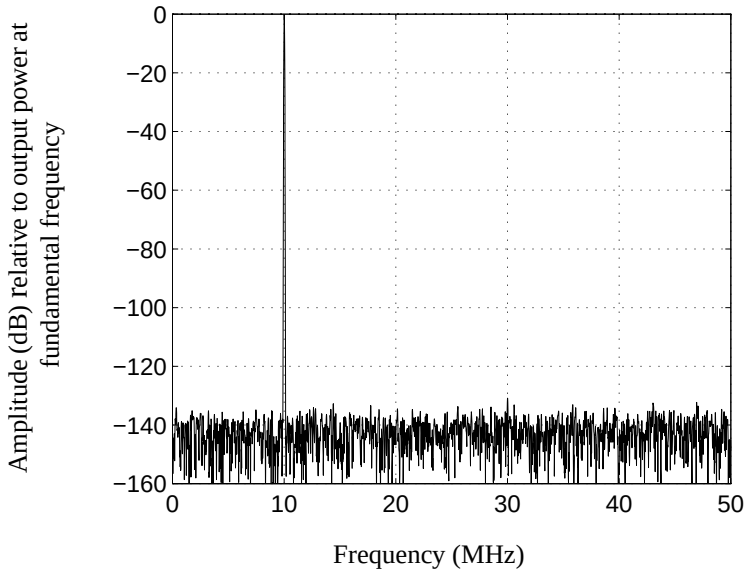


Figure 5.9: Output spectrum of the fully differential SC unity gain stage, Figure 5.7, during ϕ_1

As was mentioned in the previous section, a unity gain operation (not involving summation) does not produce any harmonics. Thus, operations involving distortion include transitions from ϕ_1 to ϕ_2 in the first and second delay cells, as well as transition from ϕ_2 to ϕ_1 in the third delay cell. The fourth delay cell has a unity gain (in both phases) and is not used in a summing configuration, and therefore is free from any distortions.

This circuit was simulated in the Eldo analog simulator using nearly ideal opamps (DC gain of 60 dB), ideal switches (1 Ω on-resistance), and the pessimistic MISNAN model for pMOSFET capacitors. All pMOSFET capacitors are biased 2.5 V into in strong inversion by selecting input and output common mode levels to be at 1 V and 3.5 V respectively. Figure 5.11 shows the output spectrum of the modulator for an input sinusoid of 6 dB below full scale amplitude and a frequency of 24.9 MHz. The non-overlapping clock frequency was set to 100 MHz. Simulated SNR is 97 dB and 63 dB for bandwidths of 200 kHz and 1 MHz respectively.

Design Considerations

In order to properly bias pMOSFET capacitors in the strong inversion regime, an opamp

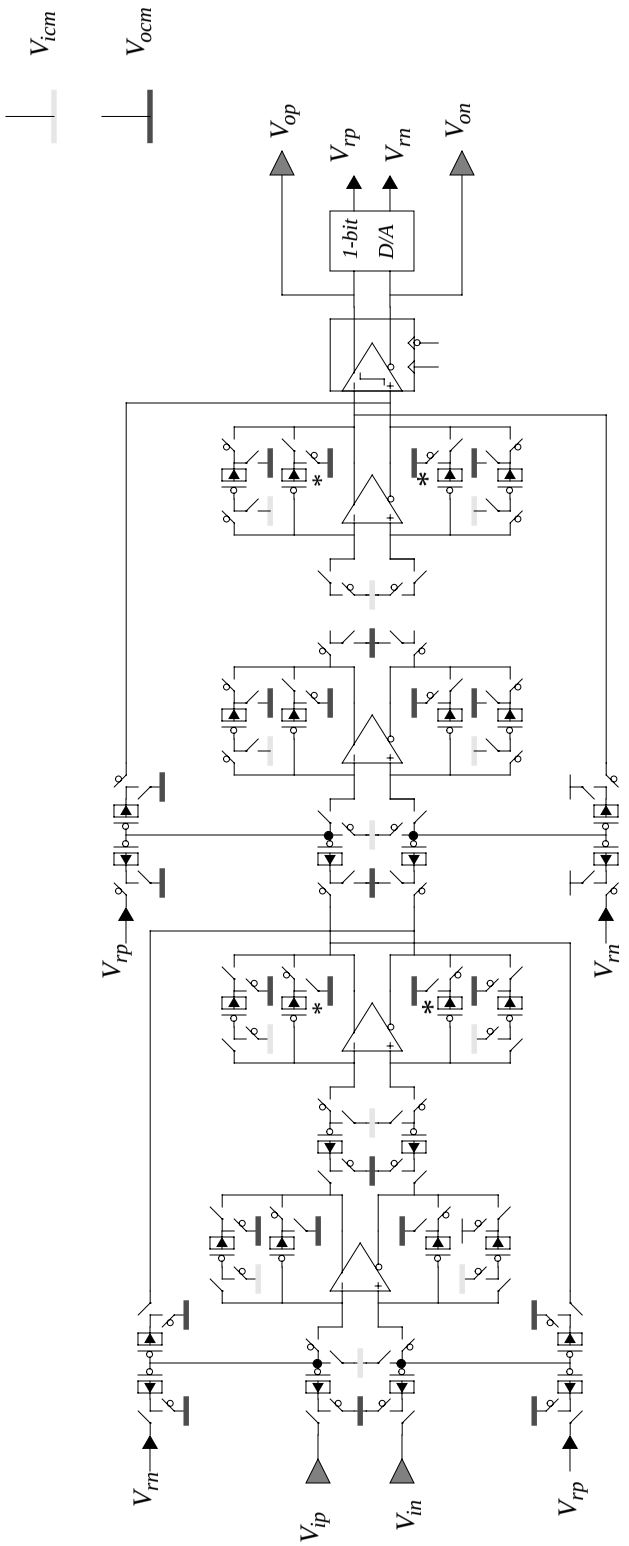


Figure 5.10: A fourth-order bandpass sigma-delta modulator using pMOSFET capacitors

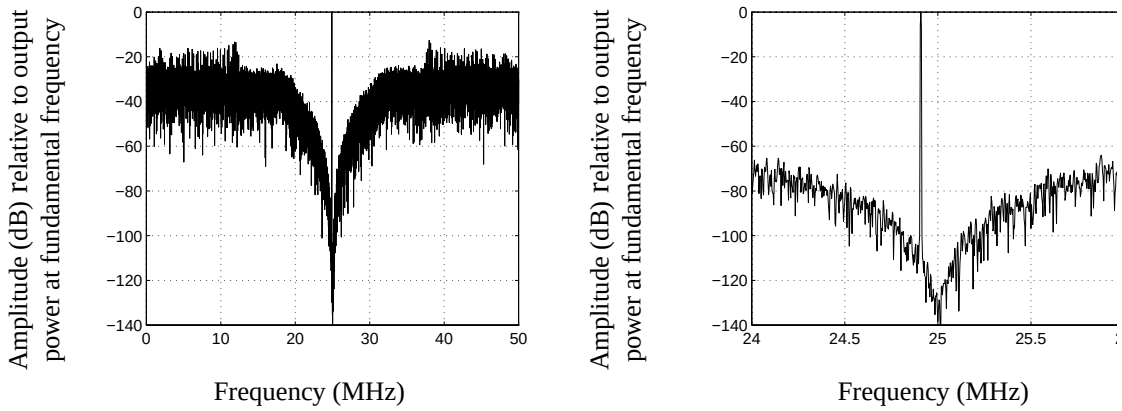


Figure 5.11: Output spectrum of the fourth-order SC bandpass sigma-delta modulator of Figure 5.10 for an input signal of *6dB* below full scale

with different input and output common mode levels is required. An efficient opamp architecture having different input and output common mode voltages is a non-folded cascode opamp, as discussed in section 4.6. The schematic of the opamp (not including the CMFB circuit) is repeated in Figure 5.12. The input common-mode level is 1 V and

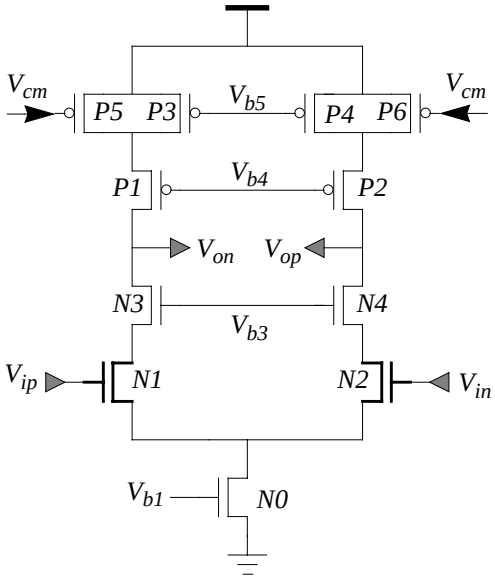


Figure 5.12: A fully differential cascode opamp

the output common mode voltage is at 3.5 V. The output signal swing range is ±0.5 V with respect to the output common-mode voltage. Simulated characteristics of the opamp

designed in the 5 V option of the HCMOS5a process (0.5 μm CMOS from SGS-thompson) are given in Table 5.3.

Parameter	Value
DC gain	61 dB
Unity gain frequency	360 MHz
Phase Margin	63°
Slew rate	500 V/μs
Differential Output swing	2 V
Power dissipation (not including CMFB circuit)	5 mW

Table 5.3: Simulated characteristics of opamp for 1pF load capacitance

Power supply voltage was 5 V and the tail current was 1 mA.

The design considerations for capacitor size and switch on-resistance are similar to those described in section 4.6 of the previous chapter.

If low threshold natural MOSFETs are available in the process, they can be used as switches, pMOSFET capacitors, and as input differential pair transistors ($N1$ and $N2$ in Figure 5.12) to further optimize the circuit. A lower threshold voltage helps reduce the on-resistance of switches, increases the linear region of the pMOSFET capacitor in strong inversion, and reduces the input common-mode level.

5.4.1 Linear Charge Processor Viewpoint

In section 2.5.3, it was shown that SC circuits are linear charge processors from input to output. To a first-order approximation, linearity of SC circuits in the charge domain is independent of the non-linearity of the capacitors. However, since external signals are typically in the voltage domain, a linear input V/Q and output Q/V converter are required.

The output of a SC ΣΔ modulator is a digital bit stream and as such no linear Q/V converter is needed at the output. Input capacitors are the only critical components that

must be linear.

A metal-metal capacitor seems to be a good choice for input capacitors. Mismatch between a metal-metal capacitor and a MOSFET capacitor is expected to be large, however, that causes a gain error which is not important in a ΣΔ modulator.

Our unity gain delay circuit is a special case of this charge domain principle where the circuit is also linear in the voltage domain.

5.5 Summary

In this chapter, non-linearity of MOSFET capacitors in a 0.5 μm CMOS process was studied. It was shown that MOSFETs biased in the strong inversion regime have a better linearity than MOSFET capacitors biased in the accumulation regime because gate-poly depletion partially compensate the non-linearity in strong inversion. The voltage coefficients of a pMOSFET biased 2.5 V in strong inversion are measured to be $\alpha_1 = 42.7$ kppm/V and $\alpha_2 = 7.7$ kppm/V^2, for a voltage swing of ± 0.5 V. The impact of capacitor non-linearity on the performance of SC delay circuit was then analyzed. Finally, the design of a fourth-order bandpass sigma-delta modulator tolerant to MOSFET capacitors was presented along with Eldo simulation results.

Chapter 6

Conclusions and Future Work

The rapid advance of CMOS technology into the deep submicron regime continues to improve the speed and packing density of integrated circuits. Device miniaturization, in deep submicron geometries, requires supply voltage down-scaling to ensure reliability. In the first part of this thesis, low-voltage circuits were considered in detail.

In deep submicron CMOS technologies, velocity saturation causes circuit speed improvement to slow down from 1.4X to about 1.2X every generation. Low voltage is also known to compromise circuit speed. The second part of this thesis therefore focused on high-speed SC circuit techniques.

Low cost implementation of a mainly digital mixed-signal circuit requires analog circuits to be implemented in a standard digital CMOS process where double-poly is not available. In the last part of this thesis, linear SC circuit techniques in a digital CMOS process were investigated.

6.1 Summary

In Chapter 2, CMOS scaling in deep submicron was reviewed. In deep submicron technologies, the supply voltage is being scaled down to assure device reliability. In conjunction with the supply voltage, threshold voltage of MOSFETs is scaling down to attain circuit speed. Low voltage analog and digital circuit techniques were reviewed. For low-voltage analog circuits, SC and SI circuits were compared and it was shown that the SC technique has advantages over the SI technique from a signal-to-noise ratio point of view.

Chapter 3 described low-voltage SC design techniques using low threshold voltage MOSFETs. Two methods for achieving low-V_t MOSFETs in current CMOS processes were discussed. In the first scheme, natural threshold voltage MOSFETs fabricated in a dual poly gate CMOS processes (with $V_t \sim 200 - 300$ mV) were proposed for low-voltage mixed-signal circuits. The second method took advantage of short-channel effects and used short-channel MOSFETs as low-voltage analog switches.

Low threshold voltage MOSFETs are leaky and a detailed analysis of the effects of leaky switches on the accuracy of SC circuits was provided. Methods of reducing the off-current through MOSFET switches were described. These methods are (1) limiting the signal swing, (2) adjusting the V_t by back bias, and (3) using novel low-leakage series transmission gate and composite switches.

Two experimental low-voltage SC sigma-delta modulators were presented. In the first design, an existing 3.3 V second-order ΣΔ modulator in a 0.8 μm BiCMOS process was modified to operate at 2.25 V. The modification involved reducing the channel length for all the switches from 0.8 μm to 0.6 μm. The new design operates at a clock frequency of 2 MHz and achieves a SNDR of 92 dB for an oversampling ratio of 256. In the second design, a 1 V first-order SC sigma-delta modulator using low threshold voltage natural MOSFETs was reported. This modulator was tested at a clock frequency of 1 MHz. For an oversampling ratio of 128 the measured SNDR is about 54 dB.

In Chapter 4, high-speed SC bandpass ΣΔ modulators were discussed. In the sampled-data domain, a direct implementation of resonators for bandpass sigma-delta modulator requires an efficient sample-and-hold circuit. A SC delay circuit was described and a novel double-sampled SC delay circuit was introduced. The impacts of circuit non-idealities on the performance of a simple SC delay cell and the double-sampled delay cell were analyzed. Two SC implementations for a fourth-order bandpass ΣΔ modulator were presented. The first design was a high-speed SC ΣΔ modulator based on a SC delay circuit and the second design was a double-sampled SC ΣΔ modulator, based on the double-sampled SC delay cell. Both designs were implemented in a 0.5 μm CMOS process. The single-sampled modulator was tested at an 80 MHz clock frequency. For an oversampling ratio of 40 the measured SNDR is about 42 dB. The modulator consumes 50 mW from a

3.3 V power supply. The double-sampled modulator was also tested at 80 MHz. The effective sampling frequency for this modulator is 160 MHz. Due to capacitor mismatch, the image signal was about 40 dB below the input signal. Measured SNDR is 30 dB (limited by the image) for an oversampling ratio of 16 (bandwidth of 5 MHz).

Chapter 5 explored the feasibility of using MOSFETs as linear capacitors in a SC circuit. It was shown that in a 0.5 μm CMOS process, MOSFETs biased in strong inversion are more linear than MOSFETs biased in the accumulation regime. An analysis of distortion due to non-linearity of MOSFET capacitor in a SC delay cell was presented. Finally, design of a SC fourth-order bandpass sigma-delta modulator using pMOSFET capacitor was described.

6.2 Conclusions

Through analyses, simulations, and measurements of some experimental circuits, we demonstrated that mixed-signal linear SC circuits

- will scale down to at least 1 V.
- can operate up to 160 MHz in a 0.5 μm CMOS using a double-sampled SC technique.
- are realizable in a standard digital CMOS process using MOSFET capacitors in strong inversion or accumulation.

6.3 Future Work

High-performance SC design from the perspective of this thesis, namely at low voltages, high speeds, and implemented in a digital CMOS process, needs further development. Some promising areas of research are as follows:

Low-Voltage SC

In this thesis, we showed that low threshold voltage MOSFETs are suitable for 1 V mixed-signal application. The next step is to integrate a second-order sigma-delta modulator with the decimation filter in order to demonstrate high resolution at 1 V and see if noise coupling from digital circuit will degrade the SNR performance.

High-Speed SC

A major limitation of a double-sampled SC circuit is image problems caused by mismatch between the two channels as well as non-uniform sampling. Architectures that are immune to mismatch would be an interesting area for research. In a ΣΔ modulator, the effect of channel mismatch might be compensated for by an LMS algorithm in DSP.

Linear SC in a Digital CMOS Process

In this dissertation, it was shown that poly-depletion causes MOSFETs to behave more linearly in strong inversion than in accumulation regime. Further investigation and implementation of some SC test circuits are required to verify this property.

In summary, analog SC circuit techniques remain viable and vital in the design of high-performance mixed-signal circuits in deep submicron CMOS technologies.

Appendix A

MOSFET Equations

The I_{DS}-V_{DS} characteristic of MOSFET in strong inversion ($v_{GS} > V_t$) can be approximated by an α-power law [Sakurai90] as follows:

$$i_{DS} = \beta(v_{GS} - V_t)^{\alpha} \qquad \text{(A-1)}$$

V_t is the threshold voltage of the MOSFET, α is the velocity saturation index which is a number less than 2, and β is:

$$\beta = \frac{1}{2}\mu C_{ox}\frac{W}{L} \qquad \text{(A-2)}$$

In this equation, μ is the carrier mobility, C_{ox} is the gate oxide capacitance, W is the MOSFET channel width, and L is the MOSFET channel length.

The delay time of an inverter (using results in [Burns64]) is then approximately

$$\tau_D = \frac{C_L V_{DD}}{\beta(V_{DD} - V_t)^{\alpha}}, \qquad \text{(A-3)}$$

where C_L is the load capacitance.

For $v_{GS} < V_t$, nMOSFETs operate in weak inversion (or subthreshold regime) with an exponential $i_{DS} - v_{GS}$ relationship as follows:

$$i_{DS} = I_{D0}\frac{W}{L}e^{\frac{v_{GS} - V_t}{n\phi_t}}\left(1 - e^{-\frac{v_{DS}}{\phi_t}}\right) \qquad \text{(A-4)}$$

Here, ϕ_t is the thermal voltage and I_{D0} the MOSFET specific current (the value of the drain current for unit transistor ($W/L = 1$) with gate to source voltage biased at threshold voltage), and n is the subthreshold slope factor. The equations for thermal voltage, the specific current, and subthreshold slope factor are:

$$\phi_t = \frac{kT}{q} \qquad \text{(A-5)}$$

$$I_{D0} = \mu C_{ox} \phi_t^2 \qquad \text{(A-6)}$$

$$n = 1 + \frac{C_D}{C_{ox}} \qquad \text{(A-7)}$$

Here, k is the Boltzman constant, T is temperature in degree Kelvin, and C_D is the depletion layer capacitance.

Appendix B

Natural MOSFET Characteristics

Low-V_t natural threshold voltage transistors can be fabricated as an option in a dual poly gate CMOS process. A process designed for 1V operation may be further simplified by eliminating the steps required for hot-carrier reduction i.e., LDD (Lightly doped Drain) implant and formation.

Natural threshold voltage MOSFETs were fabricated in a 0.5 μm CMOS process by removing the threshold adjust masks and implants. Figure B.1 and Figure B.2 show the measured I_D and G_m versus gate voltage for a 20 μm /0.5 μm nMOSFET and a 20 μm /0.5 μm pMOSFET biased at $|v_{DS}|$ = 0.1 V respectively. For 0.5 μm channel length, the threshold voltages are measured to be 202 mV and 197 mV for nMOSFET and pMOSFET respectively and subthreshold slopes are about 80 mV/decade.

Measured I_{DS}-V_{DS} characteristics for natural threshold nMOSFET and pMOSFET are illustrated in Figure B.3 and Figure B.4 respectively. In this technology, α for an nMOSFET is 1.27 and for a pMOSFET is 1.32.

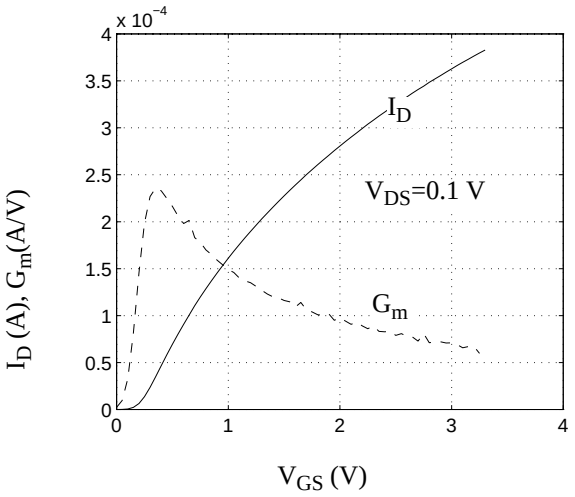


Figure B.1: Measured I_D (A) and G_m (A/V) versus V_{GS} (V) for "natural" nMOSFET

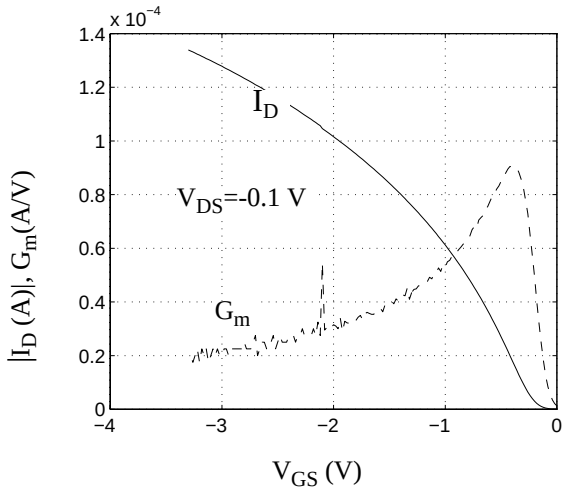


Figure B.2: Measured $|I_D$ (A)| and G_m (A/V) versus V_{GS} (V) for "natural" pMOSFET

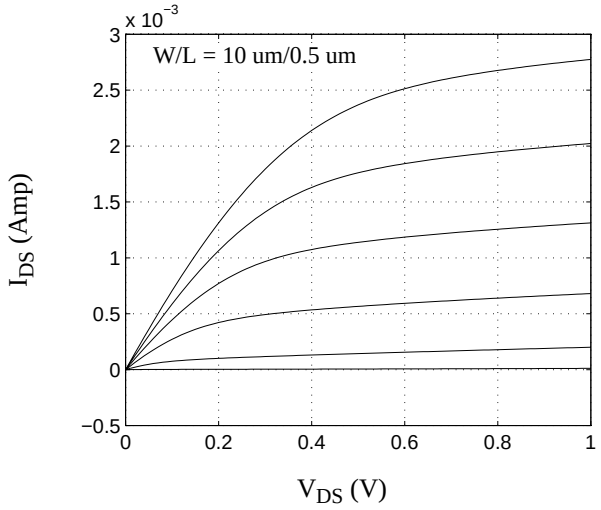


Figure B.3: Measured nMOSFET I_{DS}-V_{DS} characteristics. $I_{DS} \sim (V_{GS}-V_t)^{1.27}$

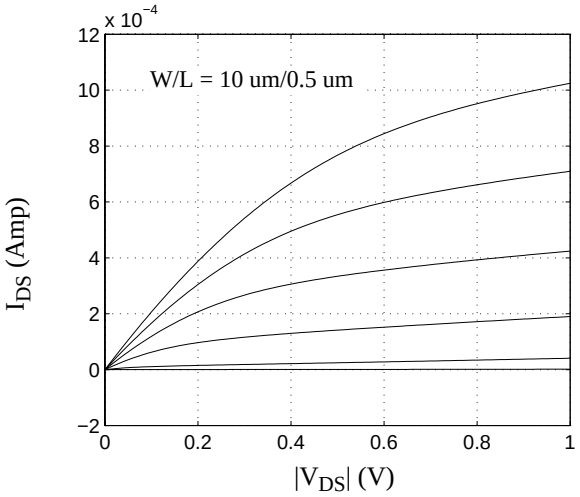


Figure B.4: Measured pMOSFET I_{DS}-V_{DS} characteristics. $I_{DS} \sim (V_{GS}-V_t)^{1.32}$

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