High-Order Bandpass Sigma-Delta Modulators

By

Stelian Mocanita

A thesis submitted to the

Faculty of Graduate Studies and Research

in partial fulfillment of the requirements

for the degree of Master of Engineering

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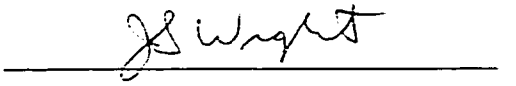

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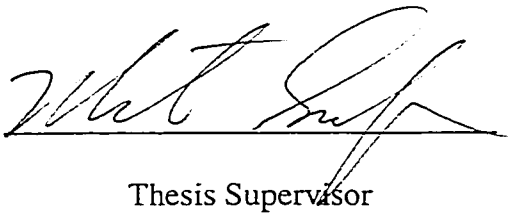

Thesis Supervisor

Carleton University

November 1998

Abstract

This thesis is part of the difficult taskwork to improve the effectiveness of the signal conversion between the complex analog world and the digital domain. A new switched-capacitor bandpass sigma-delta modulator structure, based on the sample-and-hold technique, that pushes the limits of speed in a given process, has been proposed. A new and fast switched-capacitor sample-and-hold resonator circuit has been presented. The $\Sigma\Delta$ modulator design is decomposed into Z-domain noise and signal transfer functions and further into building blocks of amplifiers/resonators, etc.

The sample-and-hold circuits with 'voltage driven at both ends' capacitors are used. While existing clock feedthrough cancellation techniques are not beneficial here, switch turn-off transient simulations and a detailed analysis for different switch topologies are presented. A new study of the charge injection dependence on clock turn-off slope and time delay demonstrates the dummy switch technique as the best solution.

Acknowledgments

I wish to acknowledge my profound appreciation to my supervisor, Martin Snelgrove, for his continuous support and guidance throughout the period of my master program.

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Table of Contents

List of Tables

List of Figures

List of Abbreviations and Symbols

a	Clock slope
A	Op-amp DC gain
α	Feedforward coefficient
ADC	Analog-to-digital Converter
β	Feedback coefficient
B	Vittoz switching parameter
BPΣΔ	Bandpass sigma-delta
C_G	Gate capacitance
C_H	Holding capacitor
C_{IN}	Op-amp input capacitance
CMFB	Common-mode feedback
C_{ov}	Overlapping capacitor
C_S	Sampling capacitor
D/A	Digital-to-analog
ϕ	Clock phase
FE	Forward Euler
f_s	Sampling frequency

g_{DS}	Drain-source conductance
GSM	Global System for Mobile (cellphone)
k	Quantizer gain
LDI	Lossless discrete integrator
LP	Lowpass
m	Magnitude error
MASH	Multi-stage noise shaping
NMOS	n-channel Metal Oxide Semiconductor
NTF	Noise transfer function
OSR	Oversampling ratio
PMOS	p-channel Metal Oxide Semiconductor
θ	Phase error
Q_{ch}	Channel charge
R_{EQ}	Equivalent resistance
$R(z)$	Resonator transfer function
R_{ON}	The "ON" resistance of a switch
SC	Switched-capacitor
$\Sigma\Delta$	Sigma-delta
S/H	Sample-and-hold

SNR	Signal-to-noise ratio
STF	Signal transfer function
τ	Time constant
t_d	Time delay
t_{onoff}	Time between a switch turns off and its dummy turns on
$\Delta V_{\text{charge injection}}$	The error voltage due to charge injection
V_{ON}	The "ON" voltage of a CMOS device
V_{sw}	The switched voltage
V_t	Threshold voltage
X-gate	Transmission gate
z	complex frequency in Z-domain

Chapter 1 Introduction

The most recent analog to digital (A/D) converter architecture, sigma-delta ($\Sigma\Delta$), maximizes the "performance/cost" ratio of an integrated circuit (IC) design (provides high resolution without trimming or high precision components, and reduces the cost of the antialiasing filter), and also makes possible a cheap monolithic integration of a whole radio circuit. For example, a bandpass $\Sigma\Delta$ modulator placed in the IF (intermediate frequency) stage of a radio reduces the stringency of specifications on the analog filters, and moves the digital signal processing closer to the front-end.

The key technical problem in this thesis is to use advanced circuit techniques and converter architectures to get high performance (in terms of speed, power, and resolution) from a low-cost technology. This work "scales" in the sense that it will guide later attempts to push more advanced technologies to their limits.

Combining the circuits designed in this thesis with architectural work [Brandt91, Lewis92] done by others, a modulator was designed and implemented in a 1.5μm CMOS

process [Mitel1.5]. It is sixth order and uses a tri-level quantizer rather than the two-level structures generally used. The use of a double sampling technique reduced the clock frequency by half. A two-delay loop was implemented with a single op-amp, and consequently the modulator needed only three op-amps instead of six. The combination of the above represents a novel architectural solution which allowed the best possible performance out of a given process at the expense of increased difficulty in design.

1.1 High-Order ΣΔ modulators

Because it is easier to understand and implement and it is always stable, the fourth order structure is preferred to higher orders in many practical applications of a bandpass ΣΔ modulator [Jantzi93, Norman96, Song95]. But with an analysis of the instability and tonal behaviour, and with proper design, a robust sixth, or even higher order bandpass modulator can be obtained.

The main advantages that high-order ΣΔ modulators offer are the high signal to noise ratios (SNR) for modest oversampling ratios and good tonal behaviour compared to low order modulators.

Since 1977, when Ritchie [Ritchie77] proved that a ΣΔ modulator can be built with an order greater than two, their performance has significantly increased, and commercial ICs have been designed with as many as 24 bits of resolution [Fujimori97]. The main structure for implementation of high-order ΣΔ modulators is the cascade of integrators with feed-

back signals from the digital to analog converter (DAC) at the input of each integrator to insure stability. Figure 1.1 shows this.

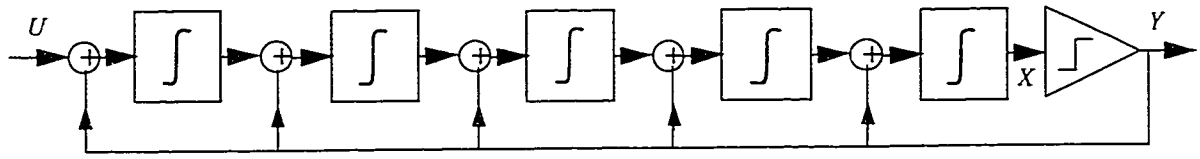


Figure 1.1 Single-loop high-order ΣΔ modulator structure.

Another approach is the MASH (multi stage noise shaping) [Hayashi86, Longo88] structure, shown in Figure 1.2, that consists of two modulators, one for processing the signal and the other one to digitize the quantization noise of the first one. The digital outputs of the two modulators are combined such that the quantization error of the first stage is cancelled. The problem here is the matching required between the filters in the two loops, analog and digital, but stability is guaranteed (first and second order ΣΔ modulators are inherently stable [Hein93]). Further improvement can be achieved if instead of a 1bit quantizer for the above high-order ΣΔ modulator a multi-bit one is used [Larson89]. The multi-bit modulators reduce the amount of quantization noise resulting in a much simpler loop filter function.The difficulty here is given by the nonlinearity of the D/A (digital to analog) part of the quantizer, compared to the one-bit quantizer that can be implemented to be very close to ideal. A solution to DAC nonlinearity is the "dynamic element matching" (or capacitor shuffling) technique [Carley89, Galton95, Schreier96] that consists of randomizing or noise-shaping the digital to analog conversion error such that it looks like

noise and not harmonics. Consequently the harmonic distortion is reduced. Nevertheless, multi-bit modulators require a more complex decimation filter.

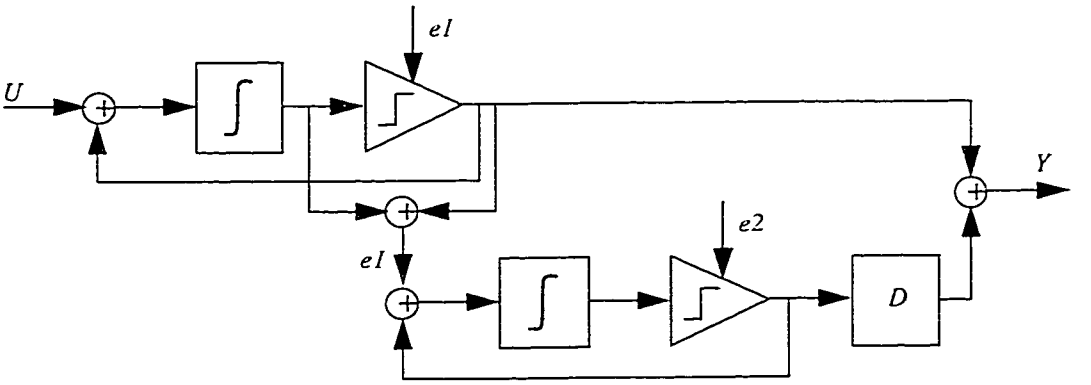


Figure 1.2 MASH ΣΔ modulator structure.

1.2 Clock Techniques

Given a particular CMOS technology, the performance of classical op-amps (DC gain, cutoff frequency, phase margin) is limited, and the design difficulty of such an op-amp depends on the particular circuit that it is used in. In switched-capacitor circuits one can exploit the fact that, sometimes, the op-amp isn't used on both phases of the clock. One can therefore double the sampling frequency by finding a circuit architecture where the op-amp processes signals on both clock phases.

Many switched-capacitor (SC) circuits known in the literature work as follows: a capacitor is charged from the input signal on phase 1 of the clock, and on phase 2 is discharged to create a signal sample at the output of an op-amp. The only thing that the op-amp did on

phase 1 was to store a previous charge, or worse yet, it did nothing. Figure 1.3.a shows such a circuit.

An efficient way to double the speed of SC circuits without imposing any other requirements on op-amps is the double-sampling technique, as shown in Figure 1.3.b. This implies the use of two capacitors such that, e.g. on phase 1 of the clock, one capacitor is charged from the input signal, and the other one is discharged to create a sample at the op-amp output. Phase 2 it is the same except that the two capacitors exchange their roles. The trade-off is that harmonic distortion is introduced due to mismatch paths.

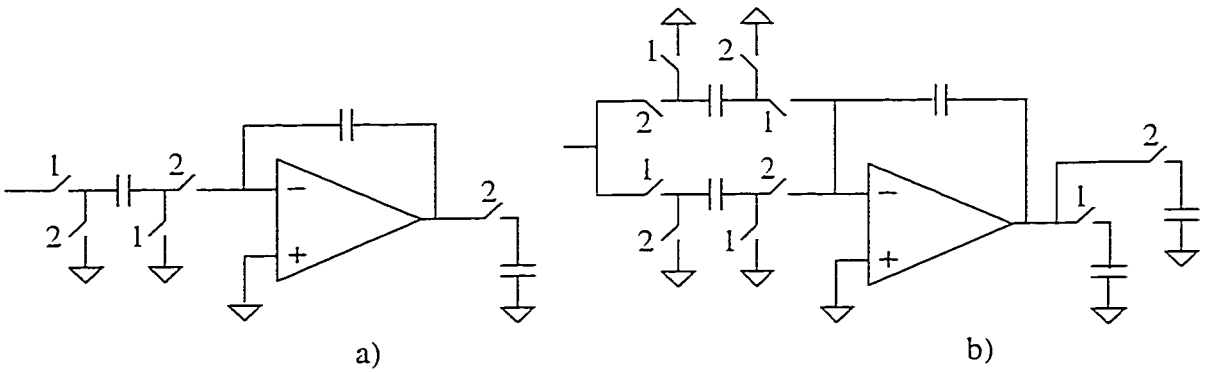


Figure 1.3 Typical a) single-sampled integrator, b) double-sampled integrator.

1.3 Thesis Outline

The next chapter is a review of existing ΣΔ modulator architectures and their constituent cells (or block components). Their advantages and disadvantages are shown, along with critical non-ideal effects and source of errors.

The noise transfer function (*NTF*) and signal transfer function (*STF*) for a sixth-order BPΣΔ (bandpass sigma-delta) modulator are studied and designed in chapter 3, and a novel architecture is proposed. Novel contributions of this thesis and their effects on the architecture's performance are presented next. The modulator architecture consists of a cascade of resonators that, in order to increase the bandwidth for a given OSR, has the feature of splitting the *NTF* zeros along the tangent to the unit circle, rather than along the unit circle. These zeros, because they are slightly outside the unit circle, will introduce a small amount of chaos into the modulator [Schreier93] and improve its tonal behaviour. A tri-level quantizer is used along with the SC four-phase sampling technique. The novelty consists in combining the double-sampling technique, the *NTF* zeros splitting technique and the tri-level quantizer. These innovations improve the SNR and the stability.

Chapter 4 deals with the circuit implementation. A new four-phase SC resonator is proposed together with a study of the component circuits (op-amps, quantizer, comparator, etc.). The resonator's novel structure doubles the sampling frequency without increasing the demands on op-amp performance.

By reason of charge injection effects, switch design is critical at high clock rates. Because sampling occurs at both ends of the sampling capacitors the conventional "bottom-plate sampling" approach is inapplicable. Therefore we have to investigate new ways to minimize charge injection effects. These effects are thoroughly studied in chapter 5. The transmission gate (X-gate), the NMOS switch, and the NMOS with dummy switches are

compared. The NMOS with dummy switch is proposed for the implementation of $\Sigma\Delta$ modulator circuit. The clock generator is also presented in this chapter.

Appendix A shows some practical problems in designing an SC circuit layout, and how to solve them. Only a carefully designed layout can ensure IC functionality close to the simulated behaviour. A chip has been submitted for fabrication (details in summary and final conclusions chapter 6).

Chapter 2 The State of the Art

The design of ΣΔ modulators relies on basic circuits like delay cells to implement integrators or resonators as building blocks. An integrator can be realized, when using a SC structure, by feeding back the output of a one-delay cell to its input. This way of realising an integrator offers innovative design solutions as compared to the one-op-amp-feedback-capacitor integrator. By using two delays and feeding back the inverted output, a resonator is obtained. Integrators are used to design lowpass ΣΔ modulators, and resonators for bandpass.

2.1 BPΣΔ, High-Order, (1.5μm CMOS)

The robust SC circuit technology was chosen for the sixth order modulator design in this thesis, due to its compatibility with standard double-poly CMOS processes. The *NTF* pole and zero locations are set by capacitor ratios, which are highly accurate (0.1% to 1%) [Lakshmikumar86]. In SC circuits, as long as full signal settling occurs, the exact shape of

op-amp settling doesn't matter, thus clock jitter is negligible except at the system input. By careful design and optimization, effects like $\frac{kT}{C}$ noise, aliasing of out-of-band noise because of the sampling nature of the SC circuits, and large spike currents drawn by the capacitors, can be diminished.

2.1.1 Topologies

A ΣΔ converter is characterized by two transfer functions: the noise transfer function (*NTF*), and the signal transfer function (*STF*). The number of topologies for a ΣΔ modulator is given by the number of ways you can build a filter corresponding to the required *NTF* and *STF*. Theoretically, this number is infinite.

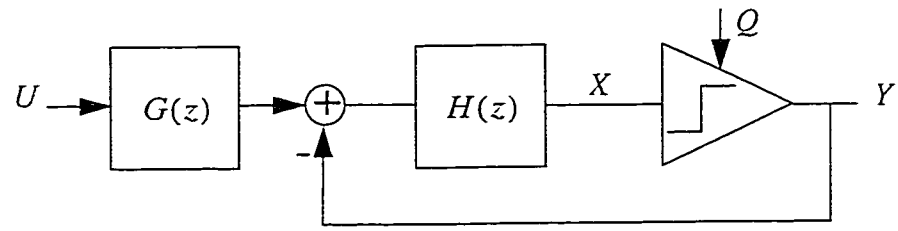


Figure 2.1 Structure of ΣΔ modulator (linear model).

By choosing the desired *NTF* for a particular application, one can verify that the *STF* shares poles with the *NTF*. The equations of these transfer functions are

$$NTF = \left.\frac{Y}{Q}\right|_{U=0} = \frac{1}{1+H(z)} \qquad \text{EQ 2.1}$$

$$STF = \left.\frac{Y}{U}\right|_{Q=0} = \frac{G(z)\cdot H(z)}{1+H(z)} \qquad \text{EQ 2.2}$$

The *NTF* is defined by $H(z)$, but the *STF* depends also on $G(z)$. The noise transfer function notch depth and its out-of-band gain are defined by the pole and zero locations. Once those are set, the remaining degree of freedom for the signal transfer function is adjusted by $G(z)$. Depending on the modulator architecture, sometimes $G(z)$ is 1. Then the *STF* zeros are determined only by $H(z)$, and the *STF* cannot be controlled independently of the *NTF*. This is not too stringent, because the main requirement for the *STF* is to be flat over the band of interest.

Some BPΣΔ topologies from the literature are presented next, where the modulator's band of interest is centered around π/2, or a quarter of the sampling frequency. Their lowpass versions can be obtained by replacing the resonators with integrators. The feedforward and feedback coefficients, and the numerators of the resonator gain can generally be considered to be of the form $Cz^{-n/2}$, where C is a constant, and n is an integer.

2.1.2 Cascade of Resonators with Feedforward Summation

For this type of structure, shown in Figure 2.2, the modulator has transfer functions given by EQ 2.3 and EQ 2.4, where N is the number of resonators.

$$NTF = \frac{(1+z^2)^N}{(1+z^2)^N - \alpha_1(1+z^2)^{N-1} - \alpha_2(1+z^2)^{N-2} - \ldots - \alpha_N} \qquad \text{EQ 2.3}$$

$$STF = \frac{\alpha_1(1+z^2)^{N-1} + \alpha_2(1+z^2)^{N-2} + \ldots + \alpha_N}{(1+z^2)^N - \alpha_1(1+z^2)^{N-1} - \alpha_2(1+z^2)^{N-2} - \ldots - \alpha_N} \qquad \text{EQ 2.4}$$

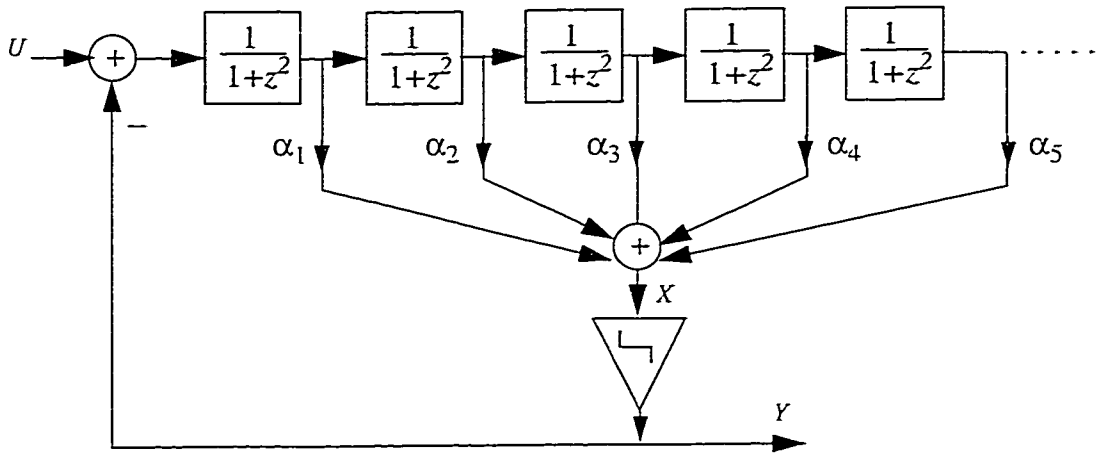


Figure 2.2 Cascade of resonators with feedforward coefficients.

The noise transfer function has all its zeros at $\pi/2$, with their conjugates at $3\pi/2$, or $z = \pm j$. In the design process, all the α coefficients are defined by the *NTF* only, and therefore the *STF* will be fixed.

2.1.3 Cascade of Resonators with Feedforward Summation and Local Resonator Feedback Coefficient [Welland89]

The difference between this topology and the previous one is the small coefficient, $-\beta_R$, around a pair of resonators, as shown in Figure 2.3.

Consider a loop of resonators with the small feedback $-\beta_R$, where one of the resonators has gain $\frac{z^2}{1+z^2}$, as shown in Figure 2.4.

This is a bandpass version of an "LDI-phased" resonator[Singor94]. The overall Z-domain function is:

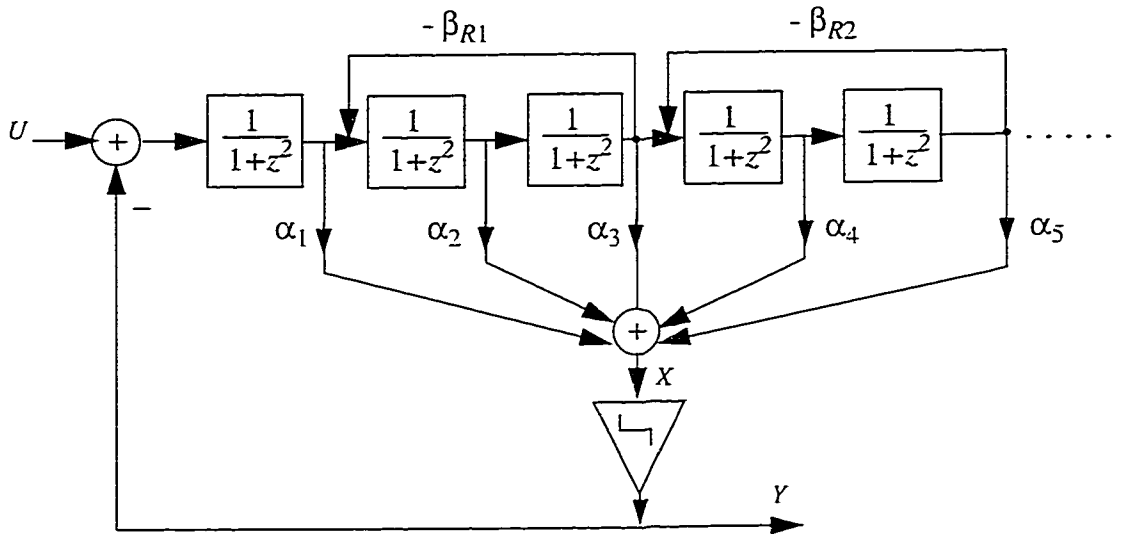


Figure 2.3 Cascade of resonators with feedforward summation and local resonator feedback coefficient.

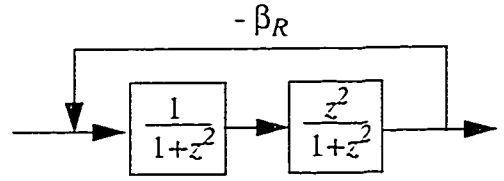


Figure 2.4 Cascade of resonators.

$$R(z) = \frac{z^2}{z^4 + (2 + \beta_R)z^2 + 1} \qquad \text{EQ 2.5}$$

The *NTF* zeros, which are the poles of $R(z)$, are split along the unit circle around $\pi/2$ with an angle equal to $0.5\ \cos^{-1}(1+\beta/2)$. Coupling resonators this way in a BPΣΔ modulator will spread the *NTF* zeros around the band of interest, such that there will be an improvement in SNR of several decibels [Jantzi91].

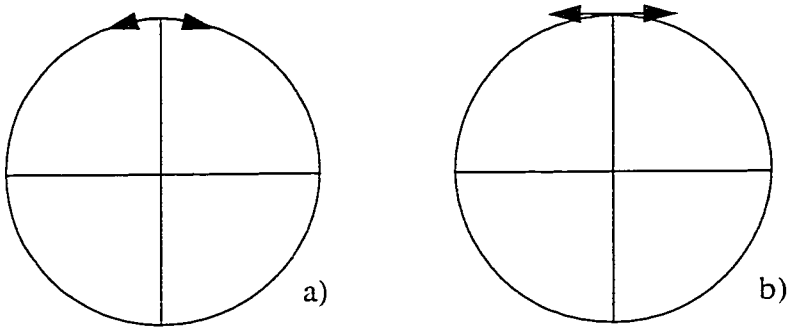


Figure 2.5 The *NTF* zeros split a) along the unit circle, b) along the tangent to the unit circle.

If both of the resonators have two delays, as in Figure 2.3, then the *NTF* zeros are split along the tangent to the unit circle at $\pi/2$, and this case will be studied in detail in chapter 3. Figure 2.5 shows the way in which the *NTF* zeros can split.

2.1.4 Cascade of Resonators with Distributed Feedforward, Feedback and Local Resonator Coefficients

With this type of structure, shown in Figure 2.6, the designer can choose the *STF* zeros independently of the *NTF* [Chao90]. The feedback coefficients are given by the desired noise transfer function, and the feedforward ones are calculated to flatten the signal transfer function over the band of interest, and attenuate as much as possible the out-of-band noise. The small coefficients, β_R, of the local resonators split the noise transfer function's zeros along the tangent to the unit circle. The *NTF* and *STF* have the following general form:

$$NTF = \frac{(1+z^2)^N - (\beta_{R1} + \beta_{R2} + \ldots)(1+z^2)^{N-2}}{(1+z^2)^N - \beta_1(1+z^2)^{N-1} - \ldots - \beta_{N-2}(1+z^2)^2 + (\beta_{N-1} + \beta_{R1} + \beta_{R2} + \ldots)(1+z^2) + \beta_N} \quad \text{EQ 2.6}$$

$$STF = \frac{\alpha_1 + \alpha_2(1+z^{-2}) + \ldots + \alpha_N(1+z^{-2})^{N-1}}{(1+z^{-2})^N - \beta_1(1+z^{-2})^{N-1} - \ldots - \beta_{N-2}(1+z^{-2})^2 + (\beta_{N-1} + \beta_{R1} + \beta_{R2} + \ldots)(1+z^{-2}) + \beta_N} \quad \text{EQ 2.7}$$

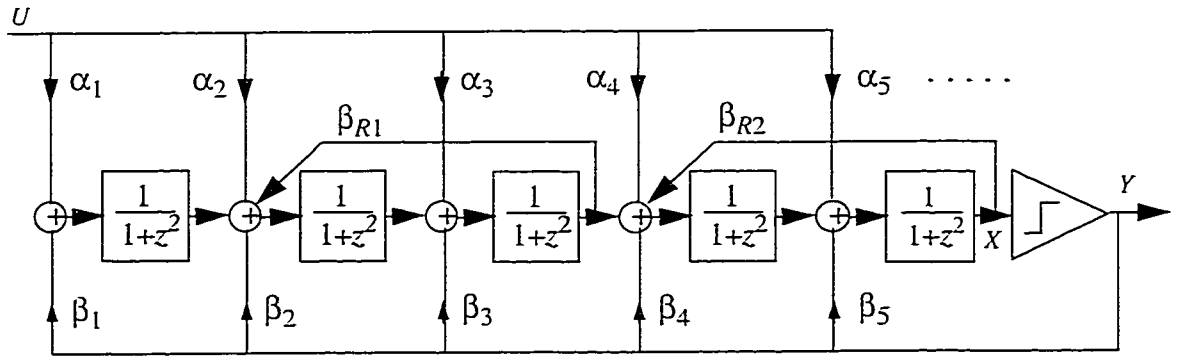


Figure 2.6 Cascade of resonators with distributed feedforward, feedback and local resonator coefficients.

2.2 Delay Cells for ΣΔ

SC circuits operate in discrete time, sampling an analog signal and then processing these samples. An arbitrary transfer function can be made by interconnecting weighted sums of unit delays, z^{-1}. An op-amp and at most a couple of capacitors can be sufficient to implement such a delay.

2.2.1 Half Delay Cell

There are many ways that a half delay cell can be realized. By using a two-phase non-overlapping clock, a half delay is obtained if on phase 1 the input signal is sampled, and on phase 2 the sample is delivered to the output. A particular delay circuit configuration is chosen depending on its sensitivity to non-ideal effects.

Two examples of half-delay cells are shown in Figure 2.7. The circuits are single ended to show the idea, but fully differential versions are generally used [Gregorian81, Hsieh81, Haug85, Ribner85, Roberts86].

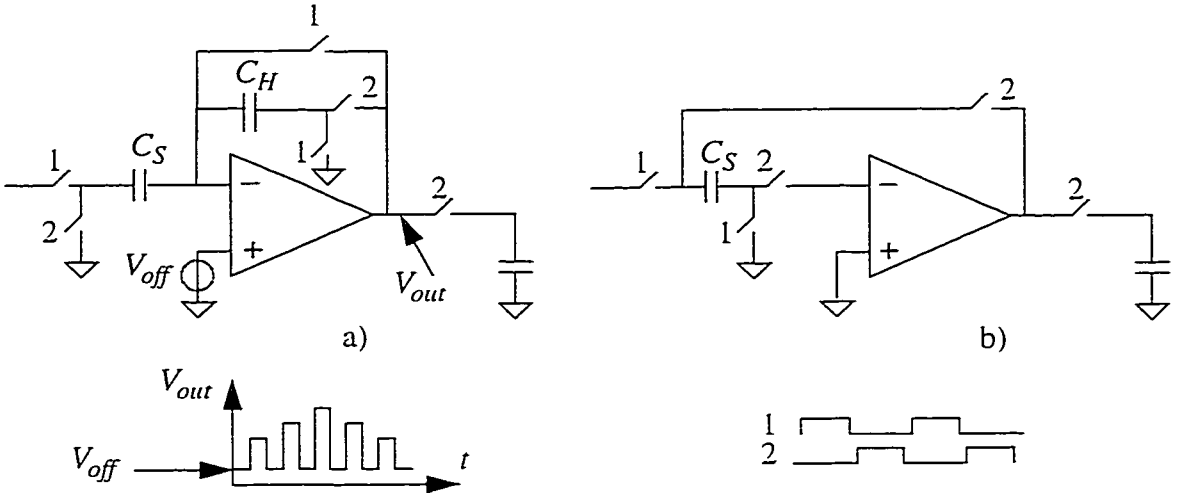


Figure 2.7 SC half-delay circuits: a) offset cancelled, b) capacitor mismatch insensitive.

The circuit type of Figure 2.7.a is used when offset-cancelling is needed (e.g. in lowpass ΣΔ modulators). On phase 1 the sampling capacitor C_S, charges to $(V_{in} - V_{off})$. where V_{in} is the input voltage and V_{off} is the op-amp offset. On phase 2 the charge transferred on the holding capacitor is $C_S(V_{in} - V_{off}) + C_S V_{off}$. The V_{off} term cancels out and the output voltage doesn't depend on op-amp offset. If $C_S = C_H$, the gain of this circuit is $z^{-1/2}$. If we assume a finite op-amp DC gain, A, then the circuit's gain is given by the formula:

$$G(z) = \frac{C_S}{C_H} \cdot \frac{1}{1 + \frac{C_H + C_S + C_{IN}}{A \cdot C_H}} \cdot z^{-1/2} \qquad \text{EQ 2.8}$$

where C_{IN} is the sum of the parasitic capacitances at the op-amp input, plus the internal op-amp input capacitance.

The half-delay cell of Figure 2.7.b is a capacitor-mismatch insensitive circuit. It flips the same capacitor C_S from the input to the output, and this means a perfect match between the two voltage samples. If one takes into account the finite op-amp DC gain, A, the circuit's gain is:

$$G(z) = \frac{1}{1 + \frac{C_S + C_{IN}}{A \cdot C_S}} \cdot z^{-1/2} \qquad \text{EQ 2.9}$$

Comparing EQ 2.8 to EQ 2.9 , the conclusion is that the delay cell of figure b) is less sensitive to finite op-amp DC gain.

2.2.2 Full Delay Cell

Figure 2.8 shows a one-delay cell using a single op-amp and three capacitors [Longo93]. On phase 1, C_S is charged from the input voltage, on phase 2 this charge is transferred to C_I, and on next phase 1, C_I transfers its charge to the holding capacitor C_H. The capacitor C_I is used to transfer the charge from C_S to C_H, and its value is solely defined by the op-amp swing and settling and thermal noise considerations.

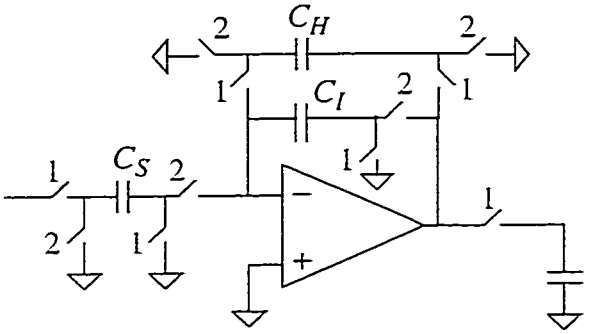


Figure 2.8 A full-delay sample and hold.

If we don't take into account the nonideal effects, the gain of the circuit is:

$$G(z) = \frac{C_S}{C_H} \cdot z^{-1} \qquad \text{EQ 2.10}$$

The finite op-amp DC gain and the non-zero input capacitance C_{IN}, introduce in the gain $G(z)$ an error component in both magnitude (m) and phase (θ)[Bazarjani96]. The gain formula that shows this, is

$$G(z) = \frac{C_S}{C_H} \cdot z^{-1} \cdot \{m \cdot e^{j\theta}\} \qquad where \qquad \text{EQ 2.11}$$

$$m = 1 - \frac{1}{A}\left(\frac{C_I + C_S + C_{IN}}{C_I} + \frac{C_H + C_I + C_{IN}}{C_H}\right) + \frac{\cos\frac{\omega T}{2}}{A}\left(2 + \frac{C_{IN}}{C_I} + \frac{C_{IN}}{C_H}\right) \qquad \text{EQ 2.12}$$

$$\theta = -\frac{\sin\frac{\omega T}{2}}{A}\left(2 + \frac{C_{IN}}{C_I} + \frac{C_{IN}}{C_H}\right) \qquad \text{EQ 2.13}$$

For example, if $A = 50\text{dB}$, $C_I = C_S = C_H = C_{IN}$, and at frequency $f_s/4$ where the passband is centered, we have $m = 0.990$ and $\theta = -0.0089$. Therefore, for the full delay cell, a 50dB DC gain op-amp causes a 1% gain error and 0.89% phase error.

2.3 Double-Sampling S/H

Figure 2.9 shows a double sampling circuit derived from the single-sampled version of Figure 2.7.b.

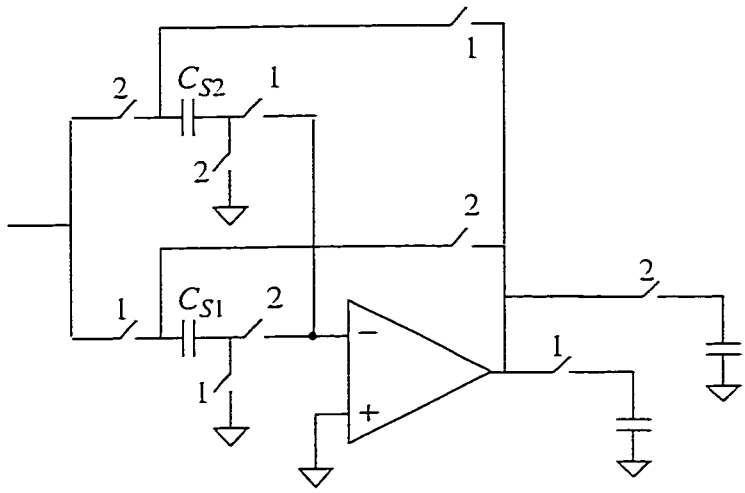


Figure 2.9 A full-delay double-sampling S/H (sample and hold).

C_{S1} and C_{S2} exchange their roles on each phase of the clock. As a result, an output sample is available on both phases. The maximum sampling frequency for this circuit is given by $1/T_{settle}$, where T_{settle} is the op-amp settling time. This sampling rate is twice as fast as the single-sampled S/H of Figure 2.7.b.

A limitation of this type of circuit is that finite op-amp gain combined with non-zero input capacitance C_{IN} causes magnitude and phase error in the output signal. This is due to the charge stored by the input capacitance at the end of each phase. Because the charge is conserved on the op-amp input node this charge contributes to the output on the next phase.

Using the double sampling technique, a second signal path is introduced. Mismatch between the two paths causes an inband image of the signal [Hurst90]. This can be reduced if architectural solutions are explored as in [Hurst92].

2.4 Switches and Charge Injection

The accuracy of SC circuits is limited due to charge injection [Gray80]. When the switch is on, it connects the signal-source node to the data-holding node, represented by the capacitor C_H of Figure 2.10. When the switch turns off, a significant part of the charge stored in the transistor channel is transferred to the holding capacitor, creating an error component, ΔV, in the voltage sample. Other parts of the channel charge go to the source and to the substrate.

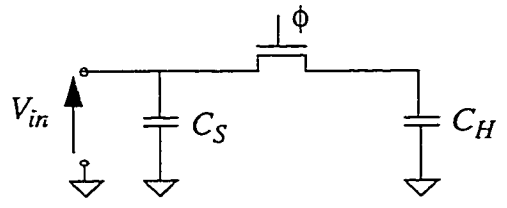


Figure 2.10 One-switch sample and hold circuit.

If the channel carrier intrinsic transient time is much smaller than the clock transient fall time, then the charge flow to the substrate is unsubstantial. The carrier intrinsic transient time is on the order of the gate capacitance times the on-resistance of the channel. Practical values for this are fractions of nanoseconds. The channel charge distribution between source and drain depends on the total values of C_S and C_H [Vittoz85], the fall-time of the clock, and also on the input source resistance [Shieh87]. For a slow fall time, the potential of the source and drain will be equalized, and the amount of charge on each side strongly depends on their impedances: more charge will leak into the low impedance side. For a fast clock the channel charge is equally distributed to both sides of the switch [Wegmann87]. If we define B, the switching parameter, as in EQ 2.14 below, then the dependence of the amount of injected charge on B is depicted in Figure 2.11.

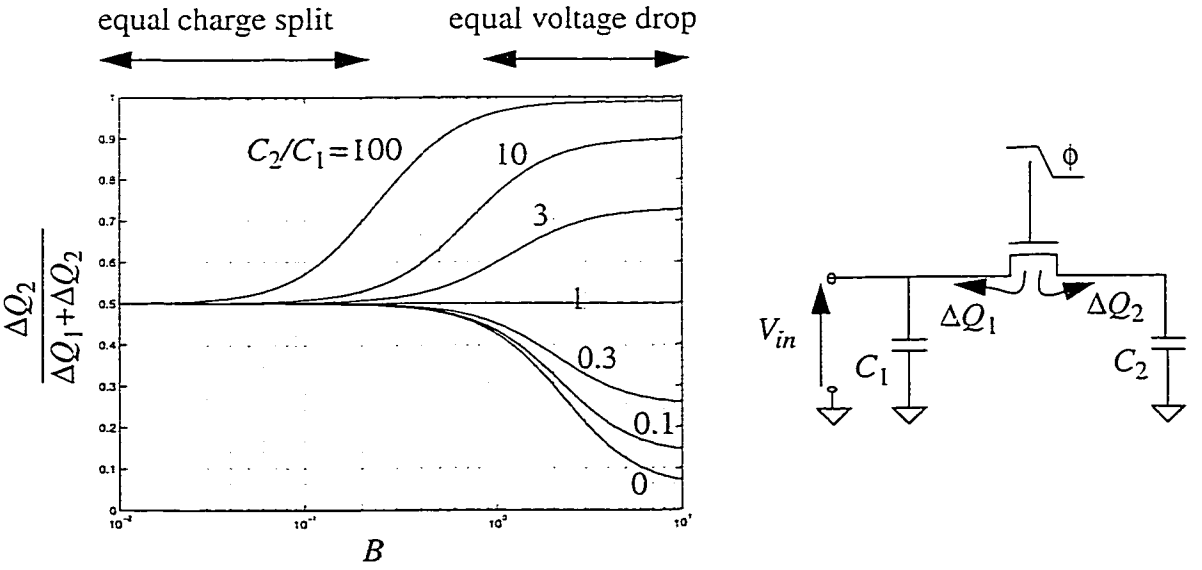


Figure 2.11 Vittoz curves.

$$B = (V_{DD} - V_{in} - V_t)\sqrt{\frac{\beta}{aC_2}} \qquad where \qquad \beta = \mu C_{ox}\frac{W}{L} \qquad and \qquad a = slope(V/ns) \quad \text{EQ 2.14}$$

Taking into account that the channel charge is $Q_c = C_{ox}WL(V_{GS} - V_t)$, and only a fraction α is transferred to the drain, the voltage across the holding capacitor is $V_{out} = V_{in} - \Delta V$ or:

$$V_{out} = V_{in} - \alpha\frac{C_{ox}WL(V_{DD} - V_{in} - V_t)}{C_H} \qquad \text{EQ 2.15}$$

ΔV is the accuracy error from the ideal of $V_{out} = V_{in}$.

To diminish the effects of charge injection, different type of switches and techniques can be used:

1. NMOS switches for low voltages, PMOS for high voltages, and transmission-gates (complementary switches) for voltages around $V_{DD}/2$ (this reduces the charge injection by minimizing the sizes of switches needed)
2. dummy switches for signal dependent charge injection [Eichenberger89]
3. bottom plate sampling [Gregorian86] with an early version of the clock signal
4. and, as a general rule, choose the minimum size switch that satisfies the settling requirements

These will be studied in chapter 5.

2.5 Conclusions

This chapter discussed several structures for BPΣΔ modulators and formulae for their transfer functions were provided. The cascade of resonators topology with distributed feedforward, feedback and local resonator coefficients allows one to design the *STF* independently of the *NTF*. The function of the local resonator is to split the *NTF* zeros in the band of interest thereby improving SNR by several dBs.

ΣΔ modulator building blocks were presented and, taking into account circuit non-idealities, their gain formulae were given.

Charge injection was outlined and the way it influences circuit performance was presented. A brief list of possible solutions to charge injection effects was given.

Chapter 3 The ΣΔ Design

Two questions that have no precise answer concern the idle tones and the stability of a ΣΔ modulator. For low-order ΣΔ modulators the main limitations are due to idle tones and low theoretical SNR, and for high-order modulators there are more sources of error due to circuit complexity, and/or the stability is critical. Practical implementations for lowpass second to sixth order, and second to sixth order bandpass ΣΔ modulators have been reported [Feldman98, Hairapetian96].

Although the sampling frequency is limited by the given process, using the high-order approach helps increase the SNR and/or the bandwidth of the ΣΔ modulators, and the idle tones are also reduced close to the noise floor level or even below.

The modulator of this thesis is intended to work at a sampling frequency of 20MHz (limited to this value by the slow 1.5μm CMOS process) and for a bandwidth of 200kHz (proper for GSM or FM broadcast specifications). This results in an oversampling ratio (OSR) of 50.

3.1 SNR vs OSR

Table 3.1 presents the performance of other SC bandpass (BP) or lowpass (LP) ΣΔ modulators of different orders and using different number of quantizer levels (Q-levels). We can notice the complexity vs performance trade-off. The performance was improved by increasing the order of the modulator and/or the number of quantizer levels, which translates into increasing the circuit complexity. Increasing the oversampling ratio is not always a solution because of the limited clock frequency in a given process.

Table 3.1 Complexity vs performance of other art.

Order-Type	Q-levels	SNR (dB)	OSR	BW (kHz)	f_s (MHz)	V_{DD} (V)	CMOS process	paper
4-BP	2	72	200	200	80	3.3	0.6μm	[Ong97]
6-BP	2	62	32	200	13	3	0.8μm	[Hairapetian96]
3-LP	9	79	25	100	5	2.7	0.6μm	[Yasuda98]
4-LP	2	90	24	1000	48	5	1μm	[Marques98]
4-LP	16	78	16	250	8	5	1.2μm	[Baird96]
6-LP	2	72	16	700	22.4	3.3	0.72μm	[Feldman98]
6-BP	3	>90	50	200	20	5	1.5μm	this thesis

Figure 3.1 shows SNR vs OSR curves collected from previous simulation results [Singor94]. They are for bandpass high-order ΣΔ modulators of order 4, 6, and 8 that use either a two-level or a tri-level quantizer. For oversampling ratios around 50, the 6^{th} order tri-level quantizer ΣΔ modulator gives a signal-to-noise ratio comparable to the 8th order two-level one. This SNR value is around 90 dB. These curves were found for optimized

noise transfer functions with zeros placed across the band of interest [Ouslis90, Jantzi91]. The gain in SNR due to the optimized placement of zeros is several decibels.

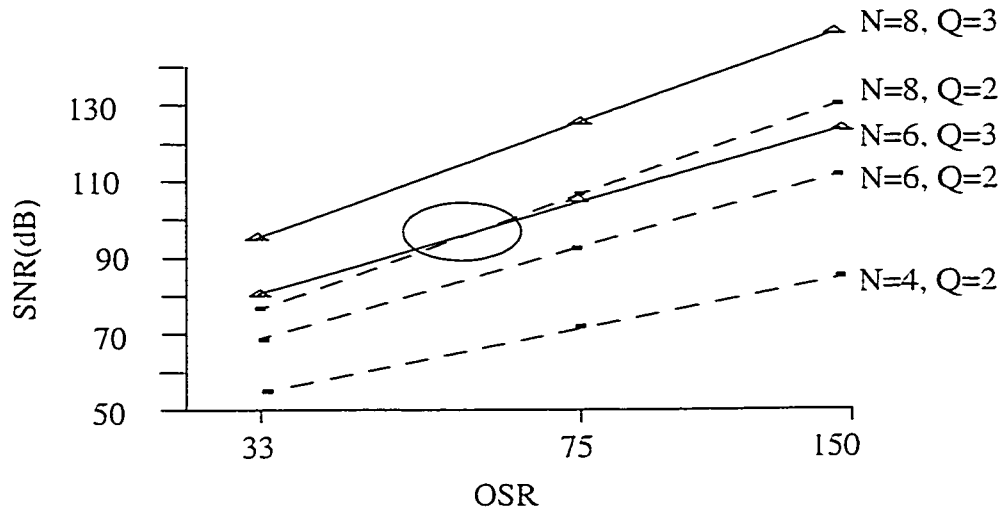


Figure 3.1 SNR versus oversampling ratio of a 4^{th}, 6^{th}, and 8^{th}-order $\Sigma\Delta$ modulator with a 2, respectively tri-level quantizer.

3.2 *NTF, STF* Design

From the previous section, from circuit complexity reduction considerations, the order of the modulator has been chosen to be six. The next step is to find the noise transfer function, as it is the function that will determine the SNR, and finally the signal transfer function will be set to the extent of its remaining degrees of freedom.

The noise transfer function design is restricted by causality and stability constrains. The system is causal if the loop around the quantizer doesn't contain any delay-free loops. This means that the loop gain, $H(z) = \frac{1}{NTF} - 1$, (see Figure 2.1, and EQ 2.1) must have at

least a z^{-1} delay, or its first discrete-time impulse response must be at $t \geq 1$ [Adams91]. This further implies that $\lim_{z \to \infty} H(z) = 0$, or $\lim_{z \to \infty} NTF = 1$ [Jantzi93]. Increasing the notch depth the *NTF* out-of-band gain accordingly increases, as shown in Figure 3.2.

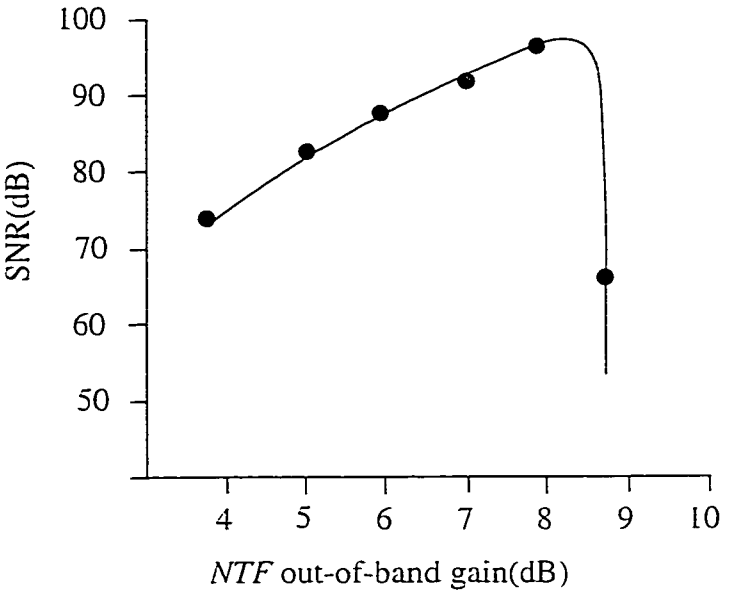


Figure 3.2 SNR vs *NTF*'s out-of-band gain for a 6^{th}-order tri-level quantizer ΣΔ modulator(OSR=50).

If the noise transfer function out-of-band gain is high, the quantizer input becomes large, and consequently the quantizer gain drops (because the quantizer output levels are fixed, 0 or ±1, while its input is increasing). This moves the *NTF* poles outside the unit circle and makes the modulator unstable [Ritoniemi90]. Due to the "pushing to the limits" nature of this thesis, the noise transfer function out-of-band gain has been chosen to be 7 dB. A small margin of safety was still maintained such that the high-risk stability edge is 1.5dB of dB away.

3.2.1 Lowpass to Bandpass Transformation

A convenient way to design a bandpass ΣΔ modulator is to design first a lowpass modulator, and then map its poles and zeros from DC to π/2 and 3π/2 using the transformation $z^{-1} \rightarrow -z^{-2}$. There are other similar transformations [Oppenheim89], but this one offers the advantage that it preserves the lowpass properties and performance (linearity, stability, SNR), and having the passband placed at $f_s/4$ allows for innovation in system design.

As discussed in chapter 2, the zeros of the noise transfer function are distributed through the signal band to lower the inband noise. FiltorX [Ouslis90] was used to optimally place the poles and zeros for both *NTF* and *STF*. The "least-pth" optimizer of filtorX adjusted the poles and zeros of *NTF* and *STF* such that their amplitude responses closely match the measures of ideality that we defined. These measures of ideality were set along the inband and out-of-band Z-plane contours and were individually weighted for their importance to the overall optimization. Figure 3.3 shows the result plots in Matlab [Matlab], and EQ 3.1 and EQ 3.1 represent the Z-domain transfer functions with precise coefficients.

$$NTF = \frac{b_0 + b_2 z^{-2} + b_4 z^{-4} + b_6 z^{-6}}{d_0 + d_2 z^{-2} + d_4 z^{-4} + d_6 z^{-6}} \quad where \quad \begin{array}{ll} b_0 = 1 & and \quad d_0 = 1 \\ b_2 = 2.99403 & d_2 = 1.54064 \\ b_4 = 2.99058 & d_4 = 0.990024 \\ b_6 = 0.996541 & d_6 = 0.146315 \end{array} \qquad \text{EQ 3.1}$$

$$STF = \frac{a_0 + a_2 z^{-2} + a_4 z^{-4} + a_6 z^{-6}}{d_0 + d_2 z^{-2} + d_4 z^{-4} + d_6 z^{-6}} \quad where \quad \begin{array}{ll} a_0 = 0 & and \quad d_0 = 1 \\ a_2 = -0.501538 & d_2 = 1.54064 \\ a_4 = -0.81582 & d_4 = 0.990024 \\ a_6 = -0.617331 & d_6 = 0.146315 \end{array} \qquad \text{EQ 3.2}$$

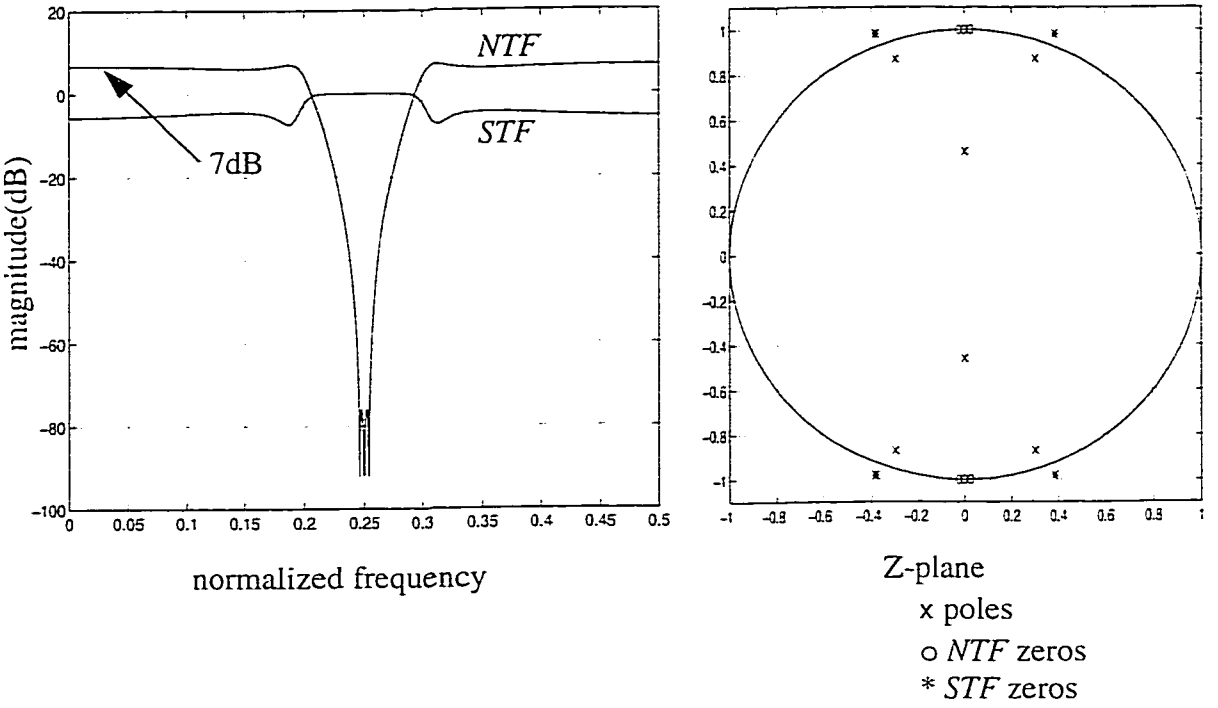


Figure 3.3 The magnitude of the 6th-order *NTF* and *STF*, obtained from filtorX, with their poles and zeros.

The *STF* couldn't be made more selective, therefore a narrow IF filter in front of the modulator will be required for FM radio applications.

3.3 Cascade of SC Resonators Structure

Comparing different types of single loop architectures (see section 2.1.1), the one of Figure 2.6 was the most beneficial in this case. Its advantages include splitting the *NTF*'s zeros across the passband, and the degree of freedom that allows us to flatten the *STF* in the band of interest by choosing appropriate feedforward coefficients α. Figure 3.4 shows

the block diagram of the BPΣΔ modulator, where A_1, A_2, A_3 are resonators with gain $\left(\frac{1}{1+z^{-2}}\right)$. A_2, A_3 and β together give a transfer function

$$R(z) = \frac{1}{z^4 + 2z^2 + 1 + \beta} \qquad \text{EQ 3.3}$$

The noise transfer function zeros, which are the poles of $R(z)$, are split along the tangent to the unit circle around π/2 and 3π/2 with an angle equal to Δθ each side (EQ 3.4).

$$\Delta\theta = \frac{1}{2}\text{acos}\left(\frac{1}{\sqrt{1-\beta}}\right) \qquad \text{EQ 3.4}$$

Splitting the zeros brings an improvement in SNR of several dBs, and the fact that the zeros are slightly outside the unit circle makes the system chaotic [Schreier93]. This, in general, reduces the inband idle tones.

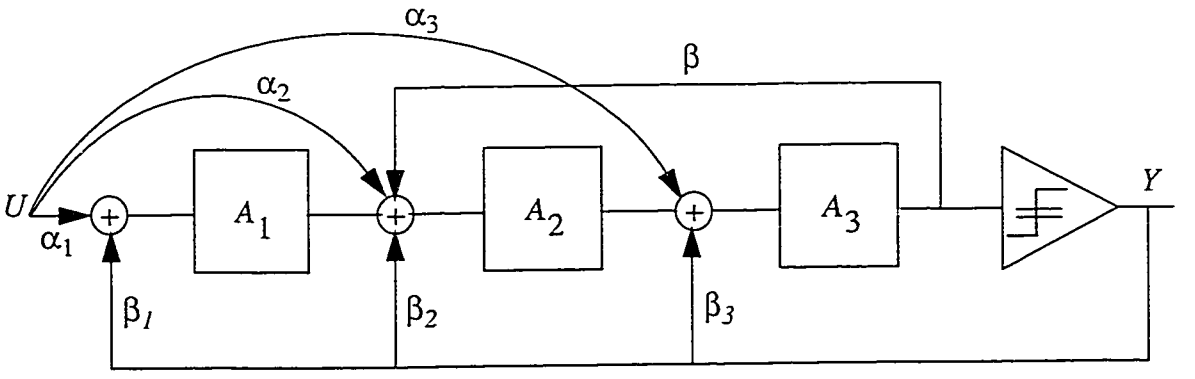


Figure 3.4 Block diagram of the 6th-order bandpass ΣΔ modulator.

3.3.1 *NTF, STF* equations

The noise and signal transfer functions of the modulator of Figure 3.4 are:

$$NTF = \frac{1-\beta A_2 A_3}{1-\beta_1 A_1 A_2 A_3-(\beta_2+\beta)A_2 A_3-\beta_3 A_3} \qquad \text{EQ 3.5}$$

$$STF = \frac{\alpha_1 A_1 A_2 A_3+\alpha_2 A_2 A_3+\alpha_3 A_3}{1-\beta_1 A_1 A_2 A_3-(\beta_2+\beta)A_2 A_3-\beta_3 A_3} \qquad \text{EQ 3.6}$$

Notice here that if A_1, A_2, A_3 are integrators$\left(\frac{1}{1-z}\right)$, the modulator is lowpass. Identifying the expressions of *NTF* and *STF* obtained from filtorX (EQ 3.1, EQ 3.1) with the ones of EQ 3.5, EQ 3.6, the values of the feedback and feedforward coefficients were found:

$$\begin{array}{lll} \alpha_1 = -0.303053 & \beta_1 = 0.303076 & \beta = -0.0025 \\ \alpha_2 = 0.18726 & \beta_2 = -0.90625 & \\ \alpha_3 = -0.501538 & \beta_3 = 1.4534 & \end{array} \qquad \text{EQ 3.7}$$

The small coefficient β was calculated by making the angle of EQ 3.4 equal to $\frac{\pi}{125}$ as in the numerator of EQ 3.1. This is shown in Figure 3.5.a. Due to its small value, β was implemented as a T capacitor as in Figure 3.5.b. Its accuracy is not critical, and simulations show that the modulator's SNR changes negligibly if β is off by 25%. Even 50% error in β degrades the SNR by only a couple of dBs. Therefore it is believed that the parasitic capacitances will not have significant effects.

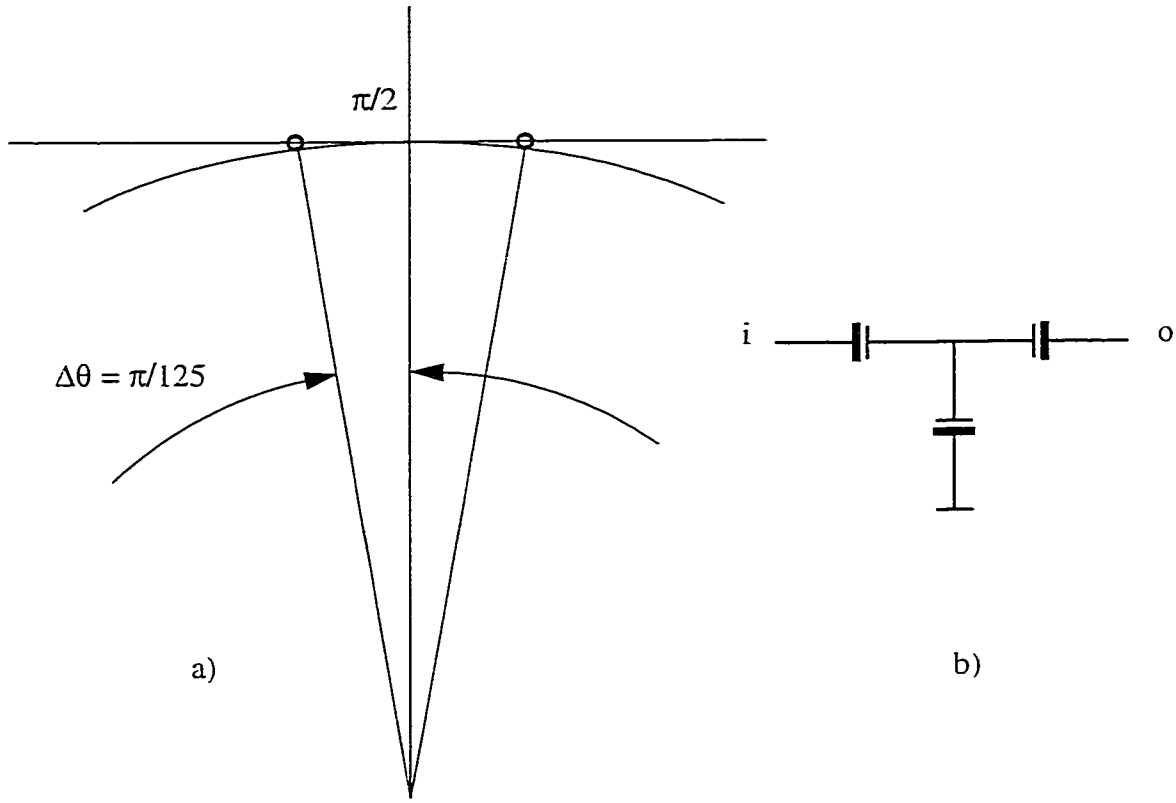


Figure 3.5 a) The *NTF* zero locations around π/2; b) implementation of the capacitor corresponding to β = - 0.0025

3.3.2 Stability by root locus

A high-order single-loop modulator is prone to instability. A method to investigate the stability of a ΣΔ modulator is the "root locus" method [Stikvoort88]. It consists of modelling the quantizer with a variable gain, *k*, as shown in Figure 3.6, and then analysing the root locus of the denominator *D(z)* of the transfer function *Y/U*, that is given by EQ 3.8.

$$D(z) = z^3 + (k\beta_3 - 3)\cdot z^2 + (3 - 2k\beta_3 - k\beta_2 - \beta)\cdot z + k\beta_3 + k\beta_2 + k\beta_1 + \beta - 1 \quad \text{EQ 3.8}$$

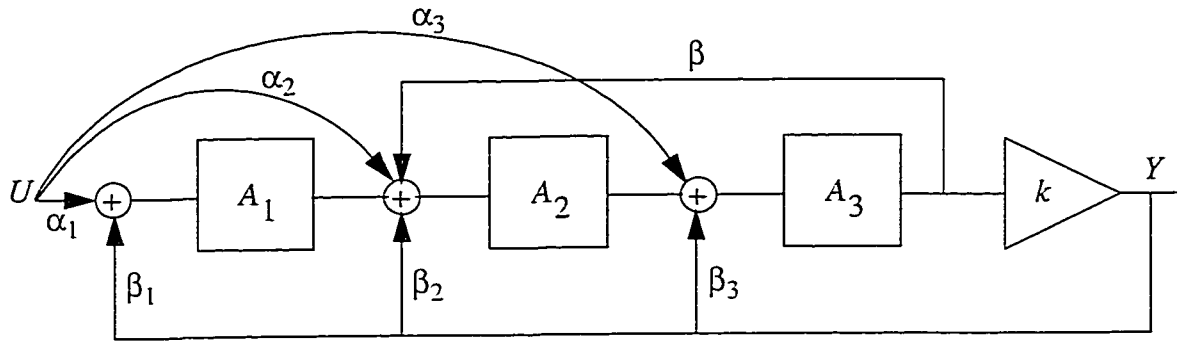


Figure 3.6 Single loop ΣΔ modulator with the quantizer modelled as variable gain.

Taking into account the inherited properties of ΣΔ when transforming from lowpass to bandpass using $z^{-1} \rightarrow -z^{-2}$, the stability analysis was done for the lowpass version of the modulator. The results are presented in Figure 3.7.

For $k > 0.59$ the complex roots move inside the unit circle, in other words the modulator model is stable. If k becomes too large ($k > 1.85$), then the real root will go outside the unit circle, accordingly the input to the quantizer will increase, and this means decreasing the effective quantizer gain, k, which will moves the root back inside the unit circle. This leads to stable operation of the modulator.

In the other case, when $k < 0.59$, the input to the quantizer becomes large, and this will move the complex conjugate roots outside the unit circle. The input to the quantizer will become larger and the modulator goes unstable.

For stability reasons k should be greater than 0.59. The value $k = 1.85$ is irrelevant since the modulator recovers by itself to a stable state whenever $k > 1.85$.

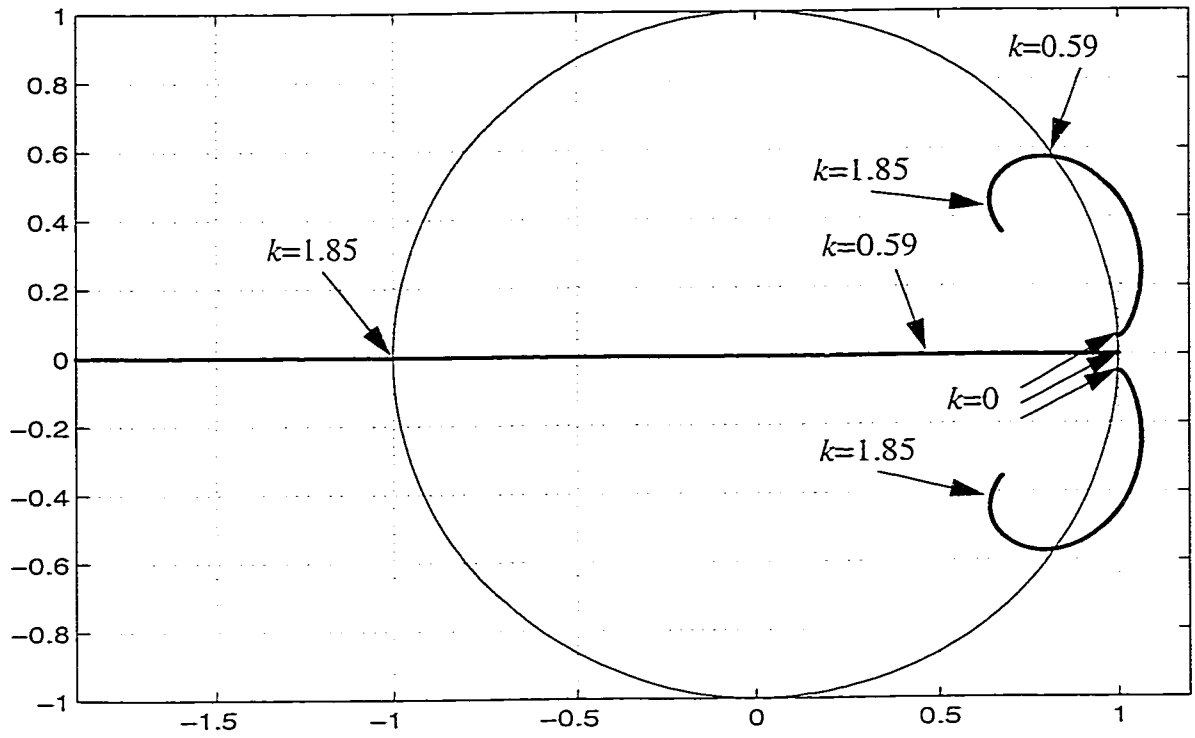


Figure 3.7 Root locus of the third order lowpass ΣΔ modulator.

Hence the root locus indicates that a modulator remains stable as long as the quantizer input is not too large. Simulations showed that the maximum input level to the system should be less than approximately 0.3 (-10dB) relative to the DAC feedback level of 1 (a safety margin was taken into account, the actual number is approximately 0.45 or -7dB).

3.3.3 Simulation Results

For a better accuracy, 131k points were used to plot the graphs of this section (an enhanced spectral resolution can reveal more tones because the noise floor is lowered). Figure 3.8 shows the typical output spectrum of the modulator. The right-hand side graph

shows the inband portion of the spectrum that contains 1310 points (corresponding to an OSR of 50). The input signal is a tone at -20dB relative to the DAC levels applied off center in the passband. (Notice here the three notches of the inband spectrum due to the three zeros of the modulator's *NTF*).

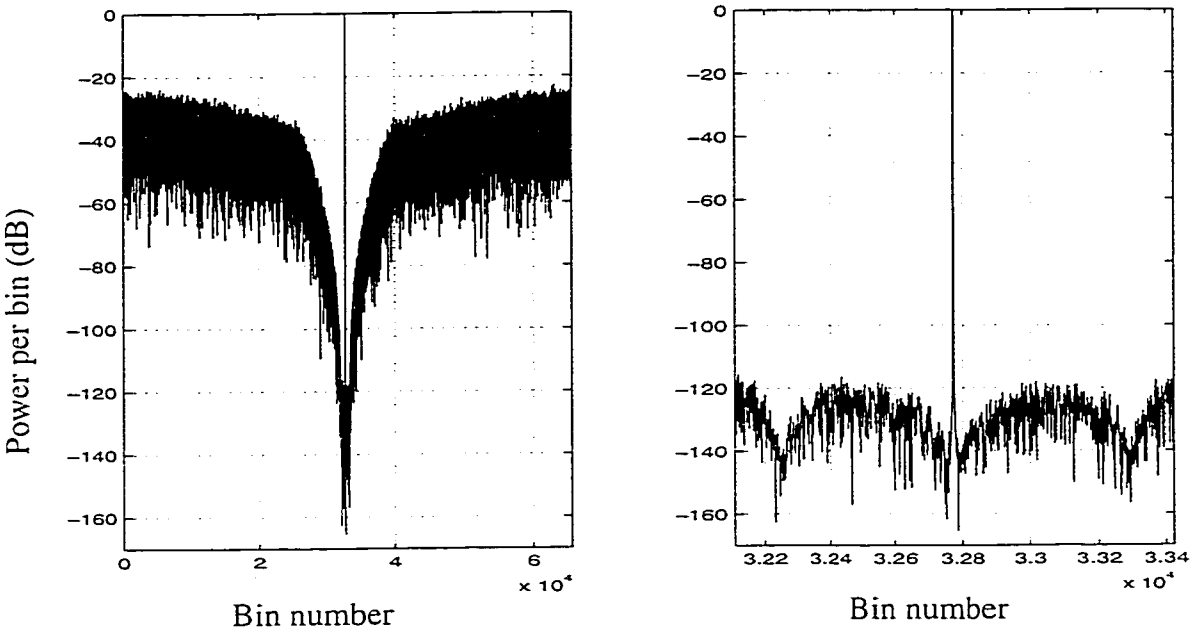


Figure 3.8 131k points whole and inband spectra with input tone near $f_s/4$.

The curve of Figure 3.9 shows how SNR varies with the modulator's input signal. At around a -60dB input signal the SNR curve exhibits a slightly nonlinearity. This is attributed to the tonal behaviour of the modulator [Gray90]. Discrete tones in any spectrum corresponds to time periodicity, therefore it is logical to relate tones in ΣΔ modulators to their limit cycle behaviour. If a limit cycle is long enough, it will have power in the band-of-interest. The tones frequency is proportional to the input signal level. The amplitude of a tone is inversely proportional to the oversampling ratio. For small input signals, around

u_{max}/OSR (u_{max} is the maximum amplitude of the input signal just before the modulator goes unstable), the idle tones lie the band-of-interest and degrade the SNR.

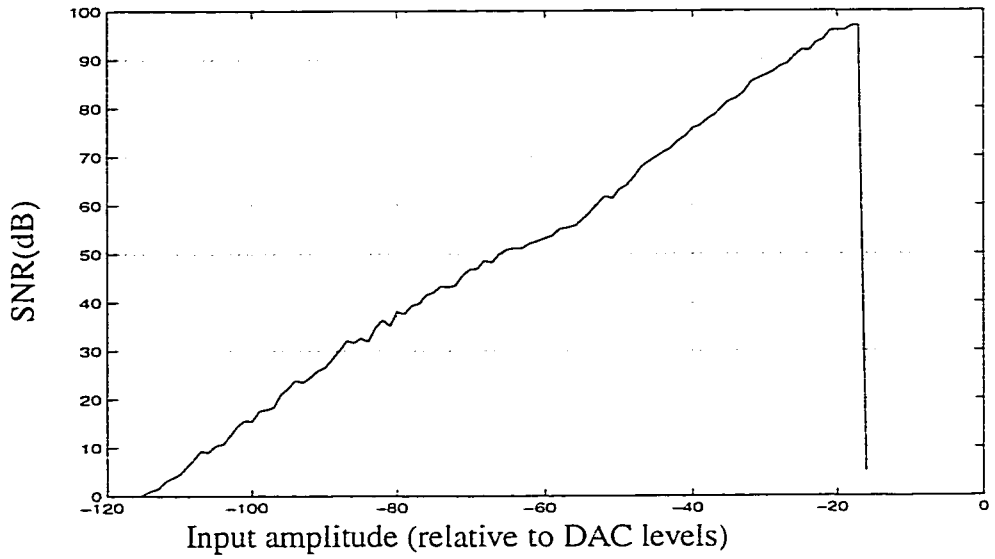


Figure 3.9 SNR vs input signal level for a bandwidth of 200kHz if clocked at 20MHz.

Because the high-order ΣΔ modulators are less prone to idle tones than the low-order ones, it is difficult to see an improvement in the tonal behaviour of a sixth-order BPΣΔ modulator if the *NTF*'s zeros are just slightly outside the unit circle. Figure 3.10 shows the spectra of two sixth-order modulators, one with all zeros on the unit circle, and the other one with the split zeros pushed outside the unit circle (1.0053 absolute value as compared to 1.00125 for our designed modulator). The location of the zero at $f_s/4$ wasn't changed. The input signal is -60dB (where the inband tonal behaviour is most noticeable) and perfectly centered in the passband. The tones are (barely noticeable) smaller for the case with zeros outside the unit circle, and, as expected, the SNR dropped from 54.2dB (as in the "all unit circle zeros" case) to 53.4dB. This shows that splitting the poles outside the unit circle

doesn't significantly improve the tonal behaviour (improved already by choosing a high-order modulator), and the main purpose of this technique is to increase the bandwidth of interest (as initially considered). A bigger zero scaling (1.05) is necessary to suppress the tones below the noise floor [Risbo95], but this drastically reduces the SNR and the modulator becomes too unstable for any practical purpose.

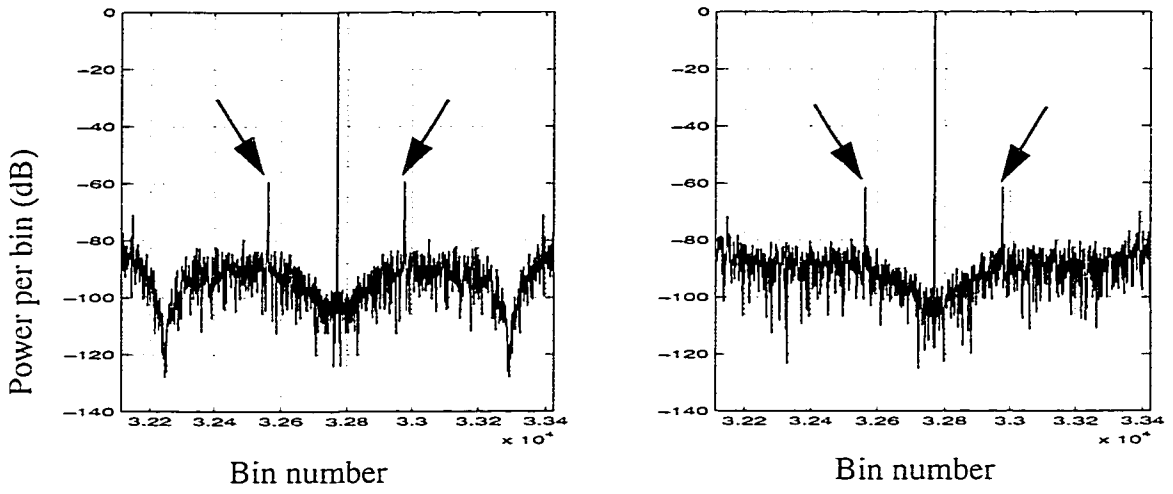


Figure 3.10 Tonal behaviour for an input of -60dB relative to DAC levels (*NTF*'s zeros are on the unit circle for the left-hand side inband spectrum, and outside the unit circle for the right-hand side one).

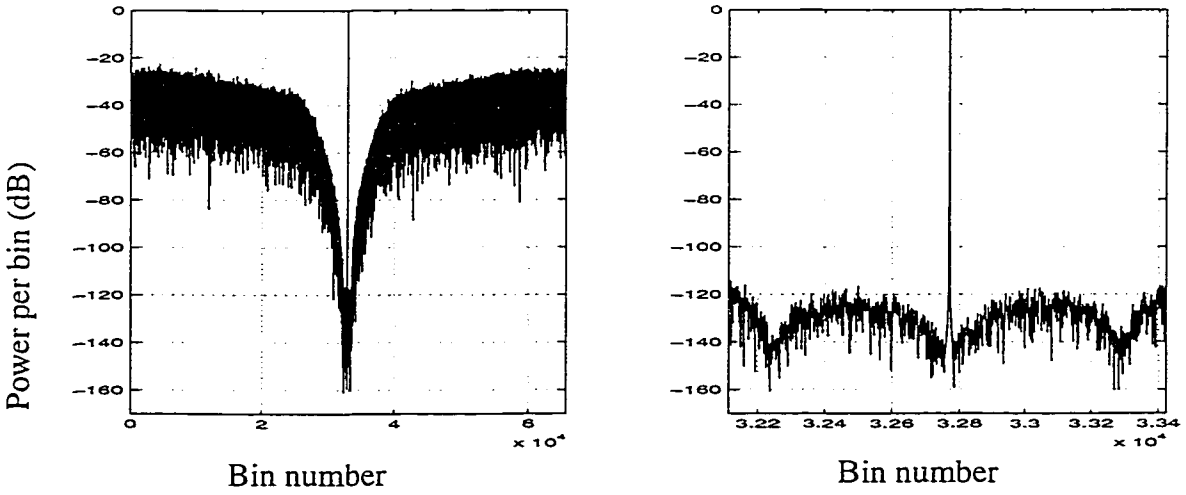


Figure 3.11 Whole and inband spectrum for 1% mismatch coefficients.

Matlab simulations (with 131k points) showed that 1% coefficient mismatches don't significantly affect the modulator's SNR. Figure 3.11 shows the spectrum of a modulator that has coefficients off by 1%. The SNR barely change from 96.5dB, as in Figure 3.8, to 96.3dB.

3.4 Conclusions

In this chapter the order, the *NTF*, the *STF*, and the structure of the modulator were determined according to the modulator's specifications (90dB SNR in the 200kHz band of interest, with a 20MHz maximum sampling frequency in the given technology) and it was shown to have stability and good tonal behaviour. Thus a sixth order, single loop, bandpass $\Sigma\Delta$ modulator with a tri-level quantizer was designed from its third order lowpass equivalent.

The SNR of the modulator was increased several dBs by splitting the *NTF*'s zeros in the band of interest. Simulation results showed that the designed modulator loses little SNR if the coefficient mismatches are as large as 1%, except the small coefficient β of the loop of resonator that can vary as much as 25%.

Chaos is not much of an issue at this level, nevertheless it was introduced in the modulator at no expense.

Chapter 4 The ΣΔ Circuit Implementation

ΣΔ ADCs are tolerant of component mismatch and circuit non-idealities as compared to Nyquist rate converters. They do not require front-end sample-and-hold circuits, but just an antialias filter with a relaxed frequency-response characteristic.

Single loop ΣΔ modulators are quite tolerant of finite op-amp DC gain, especially for the op-amps after the first stage. Non-ideal effects are most critical for the first stage op-amps which require less distortion than the others. Noise, offset and harmonics in the second and subsequent op-amps stages are attenuated by the in-band gain of the previous ones. Hence, designing the first op-amps is the most difficult.

Using a fully differential architecture presents numerous advantages: it allows easy implemention of negative coefficients; attenuates the supply and substrate noise; partially cancels out the effects of clock feedthrough and charge injection from switches; and reduces the even-order harmonic distortion.

4.1 Fully Differential SC Resonator

4.1.1 Existing SC BPΣΔ modulator circuits

Different bandpass sigma-delta modulators have been reported, and some of them will be presented in this section. The approach in [Singor94] uses the op-amps in the configuration of Figure 4.1 to design LDI (Lossless Discrete Integrator) and FE (Forward Euler) modulators. The circuit of Figure 4.1.b) settles faster than the one of Figure 4.1.a) because, on both phases of the clock, the op-amp drives only two capacitors (sampling and integrating on phase 2, integrating and loading on phase 1 whereas all three capacitors are connected on phase 2 for the circuit of figure a).

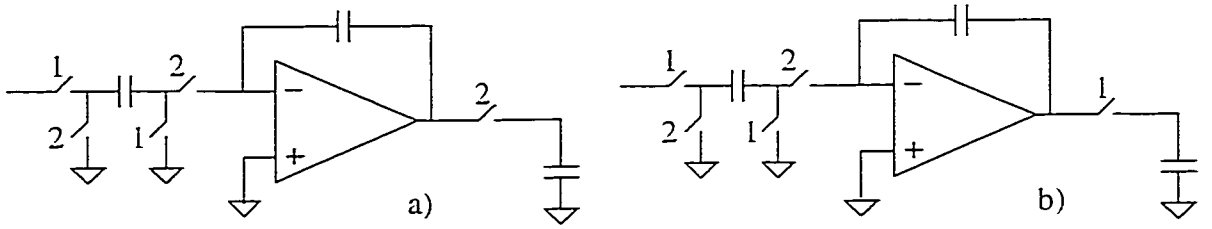


Figure 4.1 Op-amps of LDI and FE structures of [Singor94].

The circuit of Figure 2.8 was used in [Longo93]. Using just one more capacitor than the above circuits realises a full delay. The settling time is comparable to the circuit of Figure 4.1.b.

The circuit of Figure 4.2 is a single sampling SC resonator that uses a four-phase non-overlapping clock to be able to realize two delays using just a single op-amp [Hairapetian96]. On phase 1 the sampling capacitors charges from the input signal. The

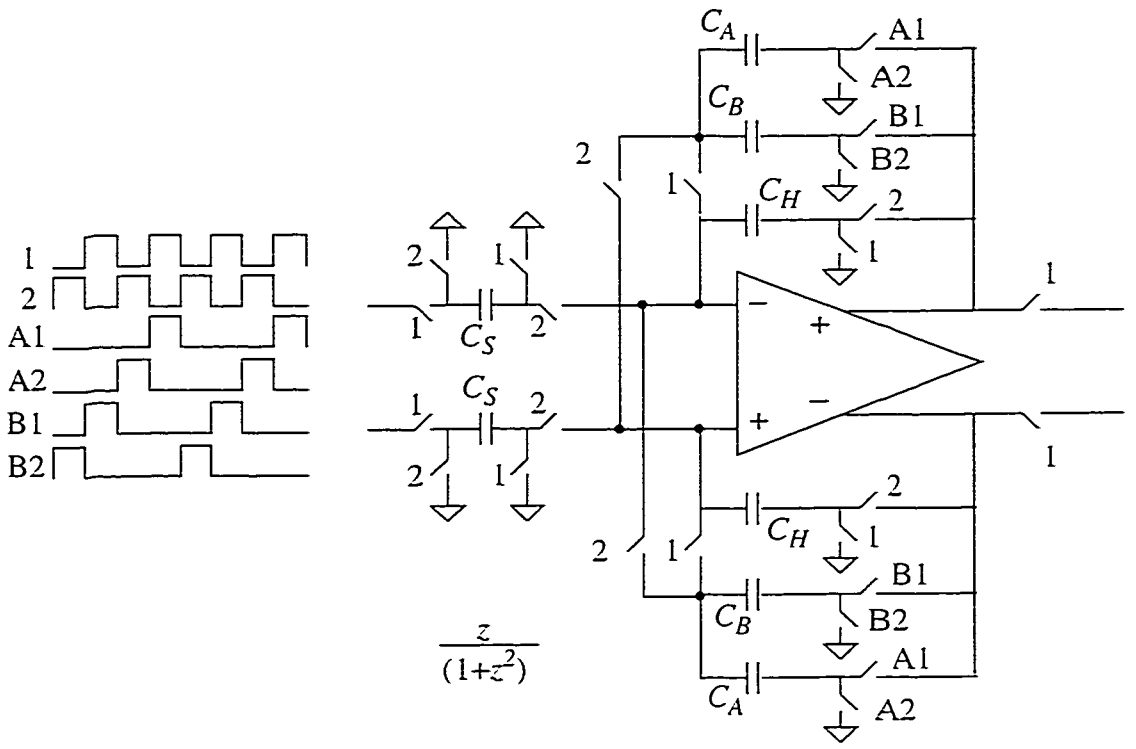


Figure 4.2 Pseudo-two-path resonator.

holding capacitors C_H, that were previously charged at the input voltage one clock earlier minus the output voltage two clocks before, transfer their charge to one of the pair capacitors C_A or C_B, (depending on which of phases A1 or B1 is high). Next, on phase 2 the sampling capacitors transfer their charge (stored on previous phase 1 from the input voltage) to the holding capacitors. Simultaneously, one of C_A or C_B, (again depending on which of phases B1 or A1 is high) that previously (3/2 clocks earlier) stored the output voltage charge, transfer their charge (with negative sign: notice the inverted connection) to C_H. For more clarity, lets consider just the case of only one capacitor pair: on phase A1

the capacitors C_A store the output from C_H, on B2 and B1 they float, and on A2 they transfer their charge to the output that subtracts from the charge due to the sampling capacitors discharge to C_H. In this way a two-clock delay is realized for the output voltage (across C_A). The capacitors C_B do the same thing but on later phases (B1 $\rightarrow$ A2 $\rightarrow$ A1 $\rightarrow$ B2). The output voltage is available on phase 1. Writing this out, one can find the relation $V_{out} = V_{in} \cdot z^{-1} - V_{out} \cdot z^{-2}$ that describes a one-delay resonator.

4.1.2 Four-path Resonator

The circuits of section 4.1.1 are single sampled. The one we propose for the sixth-order ΣΔ modulator is a novel four-path circuit using a four-phase non-overlapping clock. The clock waveforms are shown in Figure 4.3. The resonator and its connections on each phase of the clock (ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B}) are shown in Figure 4.4; the input of the modulator and the quantizer are also represented to show the way the feedback and forward coefficients are implemented.

The op-amp configuration of Figure 4.4 implements one of the resonators blocks A_1, A_2, or $A_3 \left(= \frac{1}{1+z^2}\right)$ of Figure 3.4. The resonator's equation is given by EQ 4.1, where V_i and V_o are respectively the input and the output differential voltage of the resonator.

$$V_o \cdot z^2 = V_i - V_o \qquad \text{EQ 4.1}$$

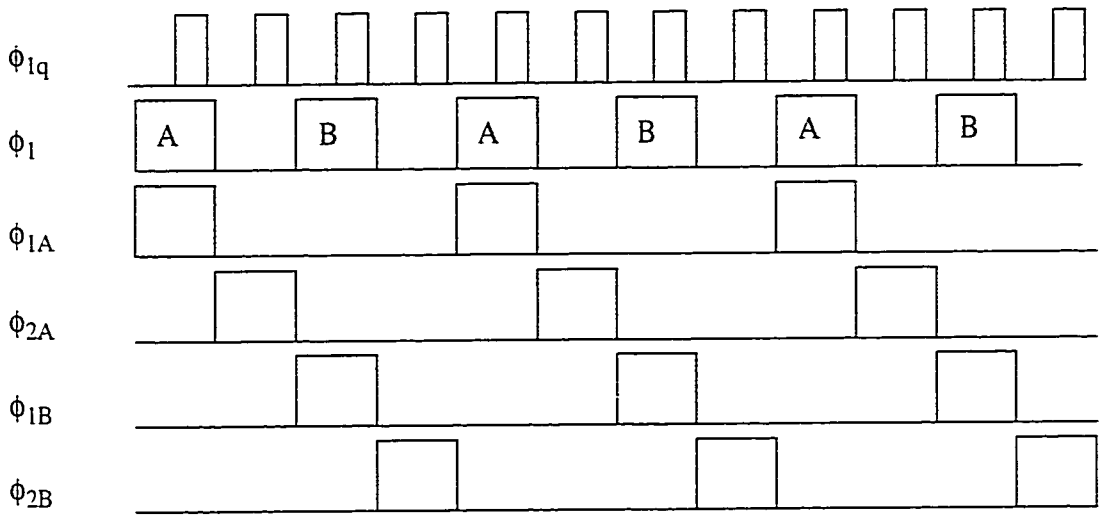


Figure 4.3 Clock waveforms for: quantizer (ϕ_{1q}), op-amp CMFB (ϕ_1), resonator (ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B}).

This means that one output sample should be equal to the input minus the output sample two clocks earlier. This is realized by charging a capacitor between the input and the output voltage of the resonator, then keeping it floating for one clock period, after which the capacitor is flipped and connected between the output and the input of the op-amp (the bold plate is solely to show the connection of the capacitor).

To implement the resonator four pairs of capacitors C_i, C_i', are needed, where i=1,2,3,4. On each phase of the clock (ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B}) only two capacitor pairs are connected, while the other two are floating. Of those that are connected, one is between the input and the output of the resonator, and the other one is between the input and the output of the op-amp.

For example on ϕ_{1A} the capacitors (C_1, C_1') are charged to $(V_i - V_o)$, on ϕ_{2A} they are floating, and on ϕ_{1B} they are flipped (notice their bold plate as compared to their connection on ϕ_{1A}) and connected between the input and the output of the op-amp. The capacitors (C_2, C_2'), (C_3, C_3') and (C_4, C_4') do the same things but on later phases ($\phi_{2A} \rightarrow \phi_{1B} \rightarrow \phi_{2B}$), ($\phi_{1B} \rightarrow \phi_{2B} \rightarrow \phi_{1A}$) and ($\phi_{2B} \rightarrow \phi_{1A} \rightarrow \phi_{2A}$).

For more clarity, this is what happens only on phase ϕ_{1A} : the capacitors C_1 and C_1' are charged to $(V_i - V_o)$, C_3 and C_3' are flipped and connected between the input and the output of the op-amp, while C_2, C_2', C_4, C_4' are floating.

To implement a forward (α_1 , α_2 or α_3) or a feedback coefficient (β_1, β_2, β_3 or β), four sets of capacitors C_{ai}, C_{ai}', or C_{bi}, C_{bi}' are needed, where i=1,2,3,4. For example, for a forward coefficient, on ϕ_{1A} the capacitors C_{a1} and C_{a1}' are charging from the differential input voltage of the ΣΔ modulator, C_{a3} and C_{a3}' are transferring their charge to C_3 and C_3', while C_{a2}, C_{a2}', C_{a4}, C_{a4}' are floating. On the next clock phases things are the same if you circularly rotate the indices i=1,2,3,4 of all the capacitors. The implementation for a feedback coefficient is the same as for a forward one with the difference that we don't charge from the input voltage of the ΣΔ modulator, but from the differential reference voltage of the quantizer's DAC.

To implement a negative coefficient simply invert the differential input. The α_1 forward coefficient can be more easily implemented if the input signal is directly connected to the

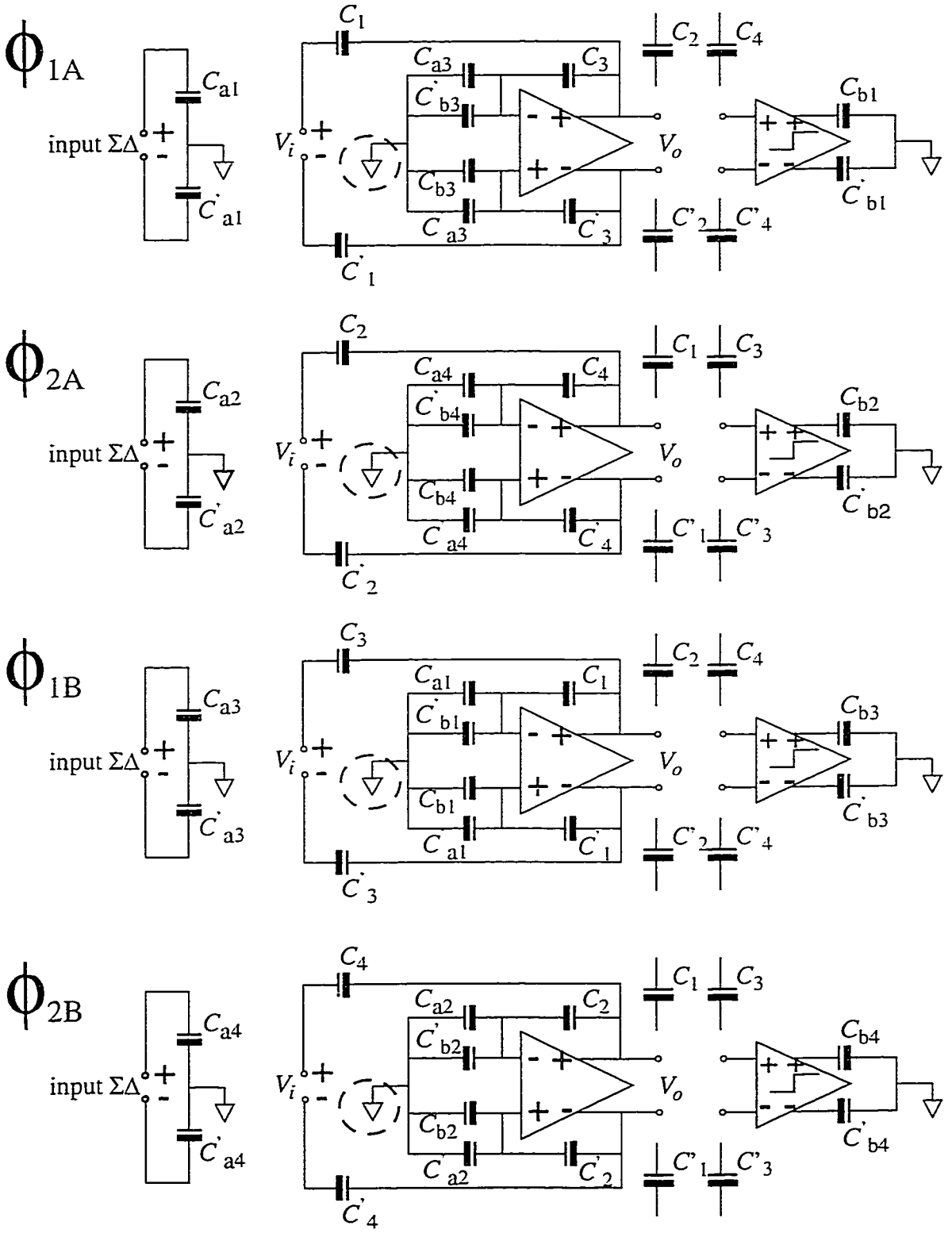


Figure 4.4 Four-path two-delay resonator.

first resonator, and not using the sampling capacitors. This saves the eight capacitors corresponding to α_1 implementation. Consequently, all the forward coefficients will be scaled to the values given by EQ 4.2. The signal transfer function is still flat in passband, but its level is shifted from 0 dB to 10 dB. Because of this the maximum signal allowed to the input of the modulator accordingly decreased by 10dB.

$$\alpha_1 = \frac{-0.303053}{0.303053} = -1$$
$$\alpha_2 = \frac{0.18726}{0.303053} = 0.6179117 \qquad \text{EQ 4.2}$$
$$\alpha_3 = \frac{-0.501538}{0.303053} = -1.65495$$

The analog ground, shown in Figure 4.4 and encircled by a dashed line, is redundant because the common mode at the op-amp's input is defined by its output common mode. It is expected that the modulator will work better without it because disconnecting an analog ground removes a source of noise.

Finite Op-amp Gain and Input Op-amp Capacitance Effects

Because the resonator is implemented with non-ideal analog components, its real transfer function is different from $\frac{1}{1+z^{-2}}$. The finite op-amp gain and the input capacitance of the op-amp will be considered next. For simplicity the single ended versions of the resonator circuits on phases ϕ_{1A} and ϕ_{1B} are shown in Figure 4.5. The capacitors C_1, C_{IN} and C_{b1} are represented with a bold plate to highlight their polarity, and the remaining capacitors are solely shown for the clarity of the circuits. C_{IN} is the capacitance at the input negative

node of the op-amp (internal + parasitics). The capacitors C_{b1} and C_{b3} are connected in this circuits to show the effects mentioned above in the case of a feedback coefficient considered. V_{ref} is the reference voltage from the quantizer's DAC.

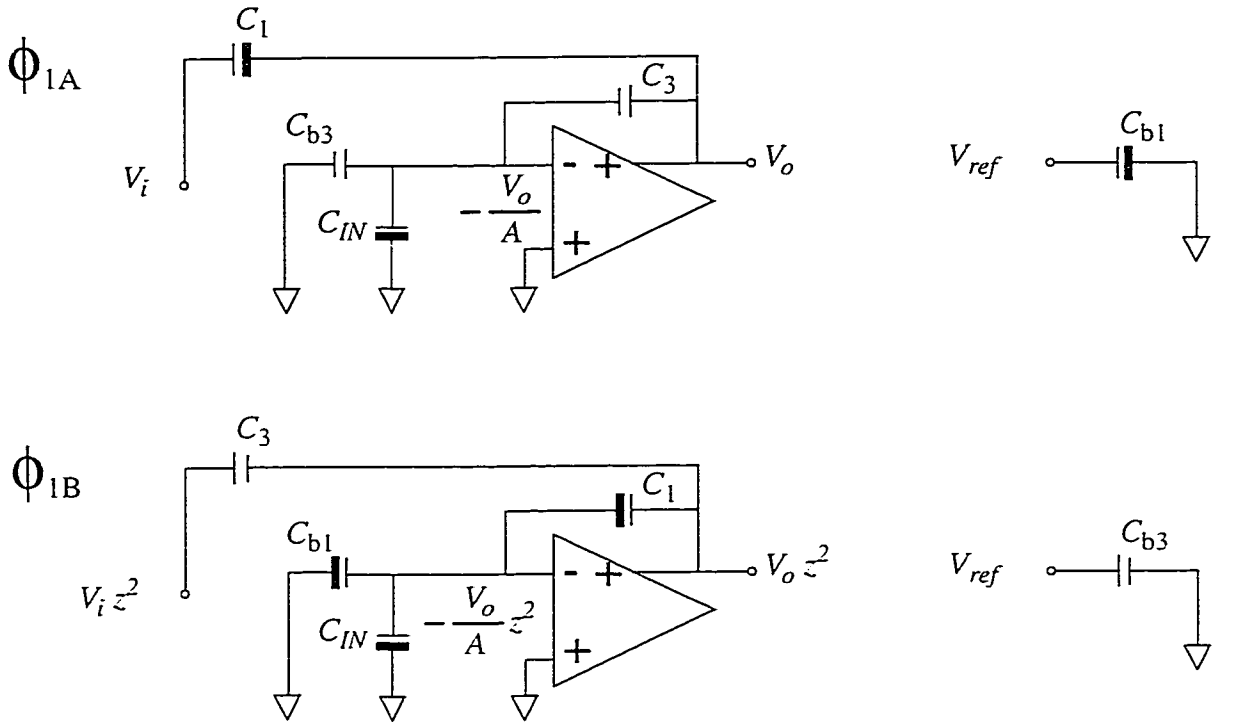


Figure 4.5 Resonator's circuits on ϕ_{1A} (top) and on ϕ_{1B} (bottom).

The finite gain of the op-amp, A, causes the voltage at its negative input to be non-zero, namely $-\frac{V_o}{A}$. The charge conservation law applied at the end of ϕ_{1A} and ϕ_{1B} gives the Z-domain equation of EQ 4.3.

$$C_1\left(-\frac{V_o}{A}z^2 - V_o z^2 - (V_o - V_i)\right) + C_{IN}\left(-\frac{V_o}{A}z^2 + \frac{V_o}{A}\right) + C_{b1}\left(-\frac{V_o}{A}z^2 + V_{ref}\right) = 0 \qquad \text{EQ 4.3}$$

An equation similar to the ideal EQ 4.1 can be written:

$$V_o z^2 = \frac{V_i - V_o + bV_{ref} + \frac{C_{IN}}{C_1}\frac{V_o}{A}}{1 + \frac{1}{A} + \frac{b}{A} + \frac{C_{IN}}{C_1}\frac{1}{A}} \qquad \text{EQ 4.4}$$

where $b = \frac{C_{b1}}{C_1}$ is one of the feedback coefficients (β_1, β_2, β_3 or β). If we don't take into account this coefficient, the resonator's transfer function is

$$\frac{V_o}{V_i} = \frac{M}{z^2 + N} \quad where \quad M = \frac{1}{1 + \frac{1}{A} + \frac{C_{IN}}{C_1}\frac{1}{A}} \quad and \quad N = \frac{1 - \frac{C_{IN}}{C_1}\frac{1}{A}}{1 + \frac{1}{A} + \frac{C_{IN}}{C_1}\frac{1}{A}} \qquad \text{EQ 4.5}$$

One can see from EQ 4.5 that the finite op-amp gain and non-zero op-amp input capacitance introduce a gain and phase error in the resonator transfer function. Substituting $z = e^{j\omega T}$ in EQ 4.5 one can find the gain and phase error:

$$\left|\frac{V_o}{V_i}\right|_{error} = \frac{M}{\sqrt{(N + \cos 2\omega T)^2 + (\sin 2\omega T)^2}} - \frac{1}{\sqrt{(1 + \cos 2\omega T)^2 + (\sin 2\omega T)^2}}$$
$$\angle\frac{V_o}{V_i}\Big|_{error} = -\tan^{-1}\frac{\sin 2\omega T}{N + \cos 2\omega T} + \tan^{-1}\frac{\sin 2\omega T}{1 + \cos 2\omega T} \qquad \text{EQ 4.6}$$

Matlab simulations (131k points) showed that for a 50 dB op-amp gain and C_{IN}=C_1, the modulator's SNR (95dB) changes insignificantly (less than 1.5% relative value for an OSR of 50 and input tone of -20dB). Notice that for the frequency $f_s/4$, where the passband is centered, the phase error is zero. This indicates that the finite op-amp gain and the non-zero input capacitance don't change the position of the passband.

Capacitor Mismatch and Mismatch Paths Effects

Because the same capacitor (e.g. C_1) is used for both sampling and holding, the resonator is insensitive to capacitor mismatches and mismatch paths. This is one of the main advantages of this type of resonator. The other important advantage is its increased speed due to the four-path technique that makes the op-amp active on each phase of the clock. This double the sampling frequency of the $\Sigma\Delta$ modulator the same way as the double-sampling technique.

4.2 Op-amps

The major trade-off of analog circuits is speed versus accuracy. An op-amp is designed to meet these requirements in a proportion depending on its application. For SC circuits the accuracy is determined by the settling time behaviour of the op-amp. High unity gain frequency is required for speed, and high DC gain is necessary for accurate settling. One difficult task is to design an op-amp that combines both of them. High DC gain can be achieved if two or more op-amp stages are used, and/or more cascoding levels with longer channel transistors and lower bias currents are added [Martin81]. Speed requires high bias currents and minimized channel length.

4.2.1 Choices Comparison: telescopic, folded-cascode, two-stage op-amps

The two-stage operational amplifier was not considered to implement the modulator because a very high DC gain is not required (see section 4.1.2). Also only an op-amp that

uses a minimum number of transistors in the signal path can provide a high-speed implementation.

For high speed with a reasonable gain, the folded and telescopic cascode op-amps are suitable for the modulator. They are shown in Figure 4.6. Assuming similar dynamic characteristics for the two types of amplifiers, the folded cascode op-amp requires twice the bias current ($2I_o$) as compared to the telescopic cascode (I_o), and a larger number of transistors, therefore a bigger die area.

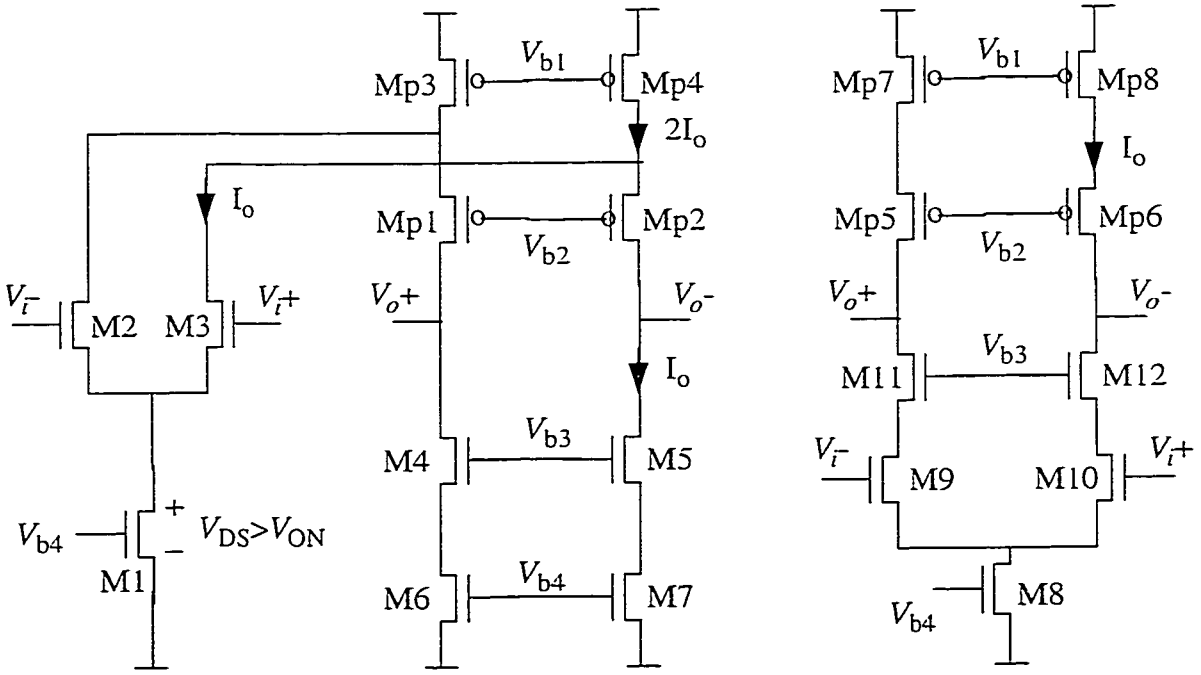


Figure 4.6 Folded cascode (left) and telescopic (right) op-amp schematics.

The dominant pole location of the folded cascode and telescopic op-amps mostly depends on the output impedance R_o and load capacitance C_L:

$$s_{dom} = -\frac{1}{R_o C_L} \qquad \text{EQ 4.7}$$

The non-dominant pole locations depend on parasitic and device capacitances at the nodes where the drains of transistors M2, M3 and M9, M10 are connected. Actually the parasitic and device capacitances at all the other nodes contribute with non-dominant poles, and their location is very difficult to estimate. The bigger the distance between the dominant and non-dominant poles, the greater the phase margin of the op-amps. This means that, if increasing the load capacitance, the phase margin increases and the amplifiers are more stable.

The principal reason to choose the folded cascode op-amp over the telescopic one is for its higher input common mode voltage range. Any value between $V_{b4}+V_{ON}$ and V_{DD} can be used to define the input common mode voltage. For the telescopic cascode op-amp the input common mode depends on the biases V_{b3} and V_{b4}, where V_{b4} is adjusted by the feed-back from the output common mode voltage. It can range between $V_{b4}+V_{ON}$ and V_{OCM} - $V_{ON}+V_t$.

4.2.2 The Differential Folded-Cascode Op-amp

The resonator of Figure 4.4 can work only if the input and the output common mode voltages have equal values, or $V_{ICM}=V_{OCM}$. Therefore the folded cascode op-amp was chosen.

The op-amp was designed for the maximum speed that can be achieved in a given CMOS process. An NMOS type input differential pair with minimum length devices was chosen

for this purpose, at the expense of phase margin. The DC gain was insured by increasing the length of the output devices. The unity gain frequency needed was obtained by choosing the right on-voltage of the transistors. The phase margin and stability were achieved by setting the load capacitance to 2pF.

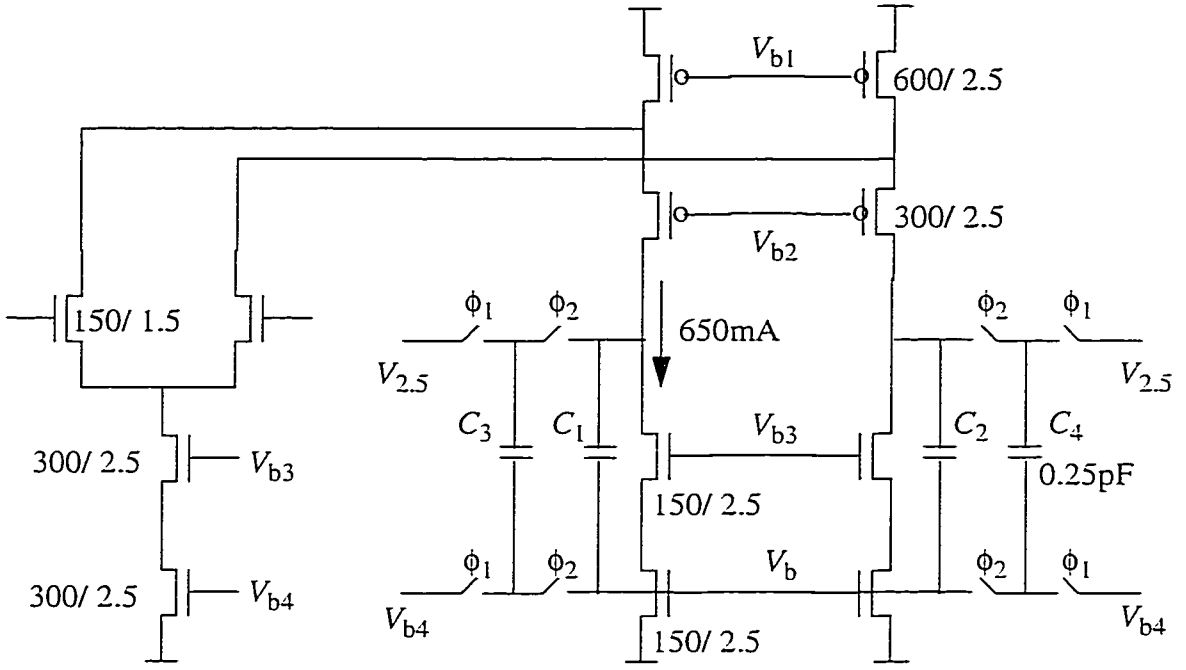


Figure 4.7 The differential folded cascode op-amp and its SC common mode feedback.

Figure 4.7 shows the folded cascode op-amp used in the modulator, along with the transistor sizes. Its common mode feedback circuit consists of the capacitors C_1, C_2, C_3 and C_4 with their switches, and it is described in section 4.2.3. The open loop gain and phase of the op-amp are shown in Figure 4.9. The DC gain is 61dB, with a phase margin of 64, and a unity gain frequency of 170MHz. The op-amp testing schematic for the settling time is shown in Figure 4.8.

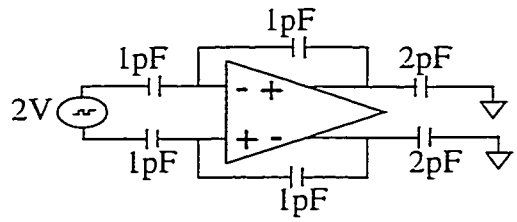


Figure 4.8 Op-amp test circuit for settling time.

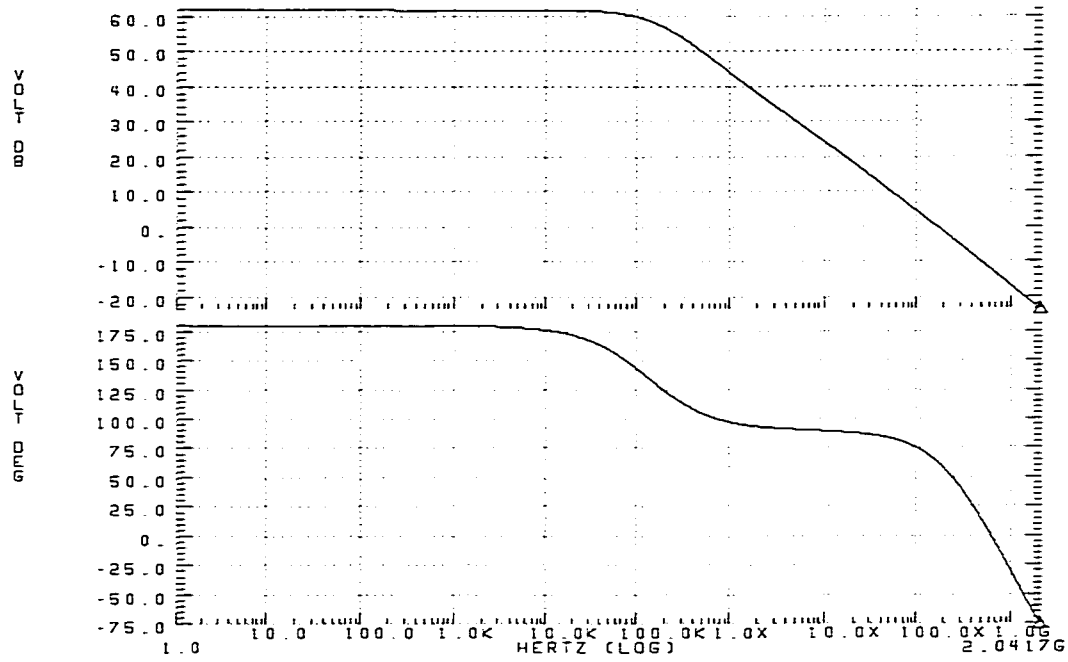


Figure 4.9 The folded cascode op-amp gain and phase for a 2pF load.

From slewing considerations the op-amp needs a 0.65mA bias current in both its output branches. The op-amp output voltage swing is 2V differential, the slewing time is 10ns and the exponential part of settling time to 0.1% of the final value is 30ns. Figure 4.10 shows the HSPICE simulation for slewing and exponential settling.

The power consumption reduction is not a goal of this thesis, therefore the same op-amp design is used in all three resonators.

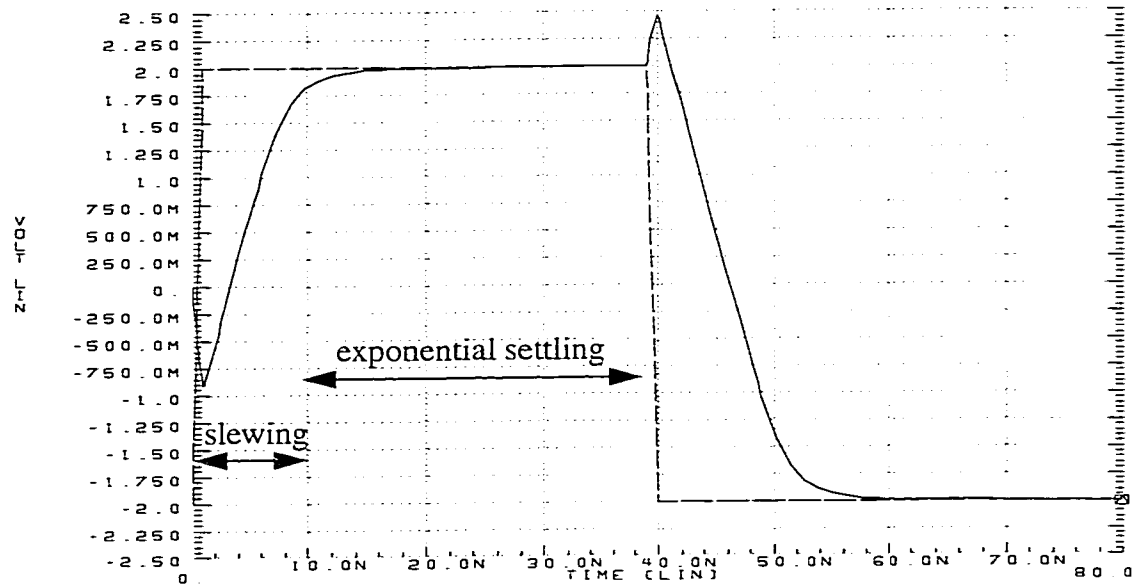


Figure 4.10 HSPICE simulation for the settling time.

4.2.3 CMFB

Figure 4.7 shows the folding cascode op-amp along with its SC common mode feedback (CMFB) [Senderowicz82, Castello85], where ϕ_1 and ϕ_2 are the two phases of the non-overlapping clock (ϕ_1 is shown in Figure 4.3). This type of CMFB is robust and doesn't require a common mode feedback amplifier.

On ϕ_1 the capacitors C_3 and C_4 are precharged from the biases voltages $V_{2.5}$ and V_{b4} ($V_{2.5}$ is the analog ground), and on ϕ_2 they provide feedback. The capacitors C_1 and C_2, that are permanently connected between the output and the gates node V_b, maintain the feedback while C_3 and C_4 are precharged.

The value of CMFB capacitors, C_{CMFB}, should be chosen such that it is neither so big as to slow down the op-amp, nor so small as to be ineffective in controlling common-mode. These capacitors should be smaller than the load capacitance to avoid significant loss of speed. The ratio C_{CMFB}/C_G sets the common mode feedback loop gain, therefore C_{CMFB} should be larger than the transistors gate capacitance (C_G) they drive. An appropriate value for the CMFB capacitors might be geometrically midway between the load and gate capacitances, so that ratios $C_{LOAD}/C_{CMFB} = C_{CMFB}/C_G$. The trade-off is difficult when designing for high speed where the capacitor loads value is close to that of the device gate capacitance, and a compromise must be made between settling and CMFB.

The op-amp of Figure 4.7 works with a load of 2pF and the gate capacitance of an output NMOS transistor is 0.35pF. The trade-off was made in favor of fast settling and all the CMFB capacitors have been chosen to be of 0.25pF, that is a minimum reasonable value for matching capacitors in the 1.5μm CMOS Mitel process. All the CMFB switches were realized with n-channel transistors of minimum size to diminish the effect of charge injection that causes a common mode voltage offset. Large transistors are unnecessary because we are setting a DC bias.

4.2.4 Biasing Scheme

There are four bias voltages and an analog ground that are generated by the simple circuits of Figure 4.11. To add flexibility for testing, these voltages can be overridden by off-chip references (the black squares of the figure are connected to pads). The transistors are

scaled from the op-amp such that the current through them is half the op-amp bias current. One such circuit provides bias for all three op-amps of the modulator. This distributed type of bias offers the advantage of saving power over the "each op-amp with its bias circuit" approach. The disadvantage is that more noise is coupled from the substrate, but eventually this can be eliminated by overriding the bias voltages from off-chip references. If three bias circuits are used for the three op-amps, the number of required overriding pads would be triple, and this can be an issue when pad-limited (as in the case of the sixth-order modulator chip designed).

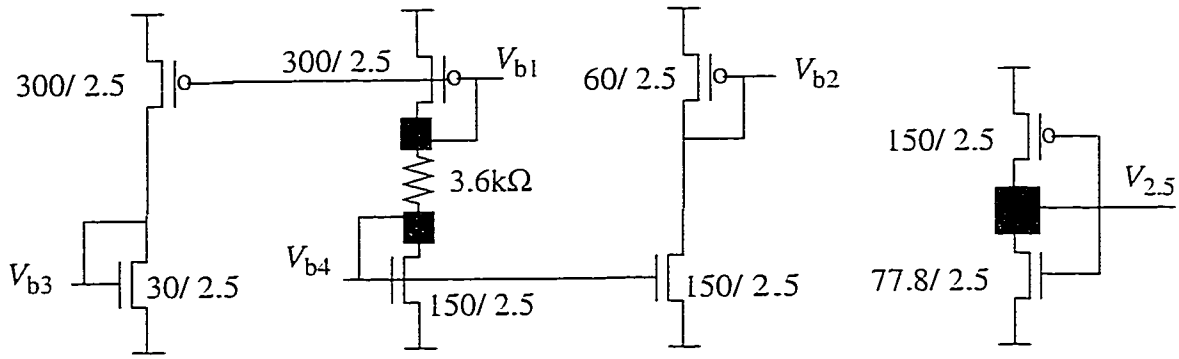


Figure 4.11 Op-amp bias circuits.

4.3 Tri-level Quantizer

Using a tri-level quantizer [Paulos87] in a sixth-order ΣΔ modulator presents advantages as compared to 1b quantizer. The SNR is increased by several decibels. As we move toward multi-bit modulators the stability is improved. The circuit is not much more complicated than a 1b quantizer, and, similarly, it isn't much more difficult to implement the

decimator that follows the modulator. The tri-level quantizer requires two comparators to divide the compared voltage range into three portions corresponding to the output levels { -1, 0, +1 }. If the +1 and -1 reference levels are not perfectly matched, even-order harmonics can occur (the conventional two-level quantizer produces only an offset between the input and output of the ΣΔ modulator).

4.3.1 Tri-Level Flash ADC

The quantizer for a ΣΔ modulator is in fact an ADC. The parallel or flash architecture of Figure 4.12 was chosen to implement the tri-level quantizer. The performance of ΣΔ modulators doesn't require a very high accuracy quantizer because the errors that appear at the input of the quantizer are noise shaped by the modulator's loop gain.

The flash ADC is an adapted version of that of [Lewis87]. It uses a non-overlapping clock with phases ϕ_{1q} and ϕ_{2q}, as shown in the Figure 4.12. On phase ϕ_{1q} the capacitors are charged from the references of the resistor string, and on ϕ_{2q} they are connected to the input (at the last op-amp's output). The comparison is then made.

While the op-amp is settling, the quantizer has to charge its capacitors from the reference voltages, subtract from the differential input voltage and do a comparison at the end, when the op-amp is settled. Therefore, the quantizer runs at twice the op-amps clock frequency. This is not a problem because the comparator can be designed to run at a much higher speed than the op-amp.

From thermal and quantization noise considerations [Thompson94], an optimal value of 0.3 was chosen for the quantizer threshold. Due to the differential structure, the tri-level quantizer is perfectly linear even if the references are slightly off-value.

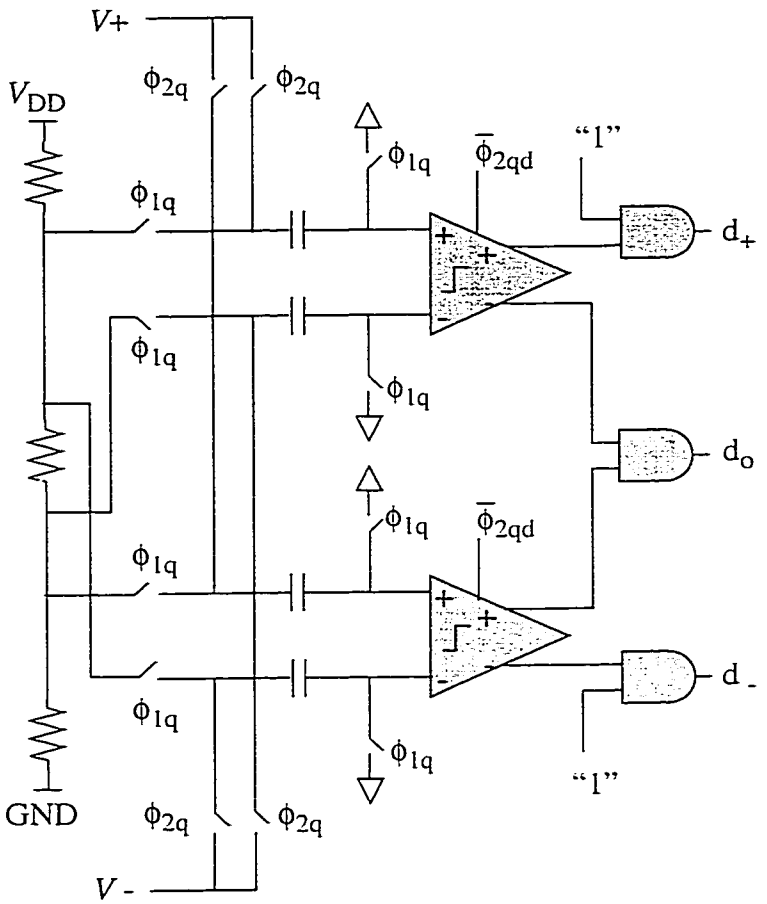


Figure 4.12 Tri-level flash ADC schematic.

4.3.2 Comparators

The comparator offset and hysteresis don't affect ΣΔ modulator performance, hence their design is not critical. The fully differential folded cascode structure [Lewis92] of Figure 4.13 consists of a folded cascode amplifier where the output bottom current sources

were replaced by a latch configuration. The comparator device sizes and its bias are also shown (biases V_{b7} and V_{b8} can be overridden from off-chip references). The input differential pair and the latch are using NMOS devices because they are faster than PMOS.

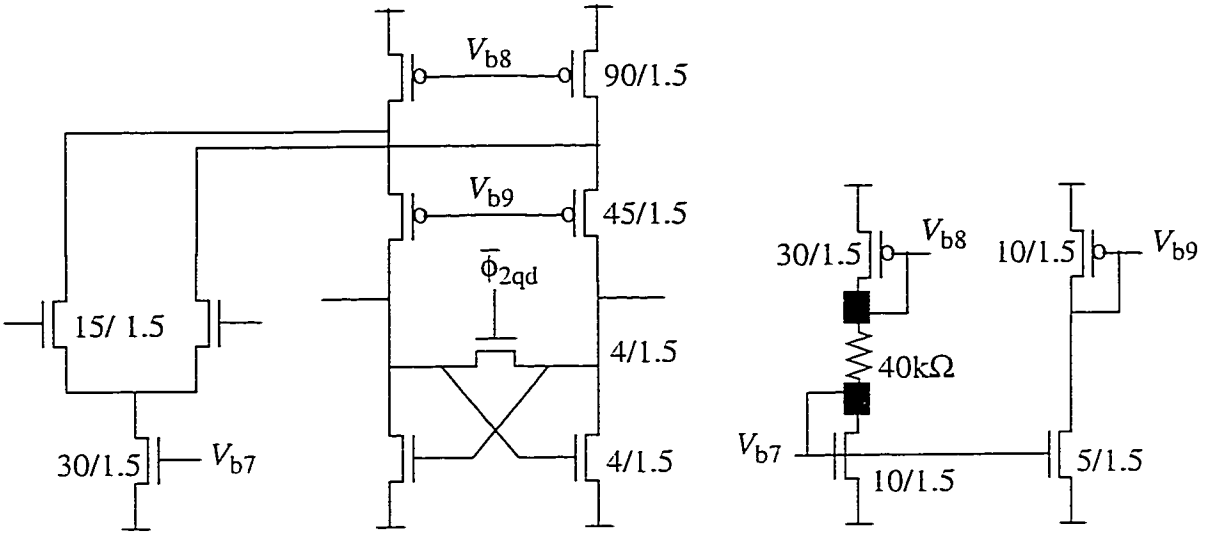


Figure 4.13 Comparator and its bias schematics.

4.4 The D/A

The feedback coefficients implementation require a D/A converter that transforms the digital output of the quantizer back into an analog signal. This can be easily achieved by the nearly ideal tri-level D/A convertor of Figure 4.14. The voltage drop across the middle resistor is V_R and this will be supplied to the feedback coefficient capacitors according to the output of the quantizer (d_+, d_o, d_-). If d_+ is high V_R will be fed back, if d_- is high the D/A differential outputs are inverted (notice the switches driven by d_-) and $-V_R$ is available for feedback, and if d_o is high the capacitors are connected to analog ground, hence 0V is

in the feedback. The reference voltage can be off-chip overridden. This allows us to test the chip for the effect of different ΣΔ loop signal levels.

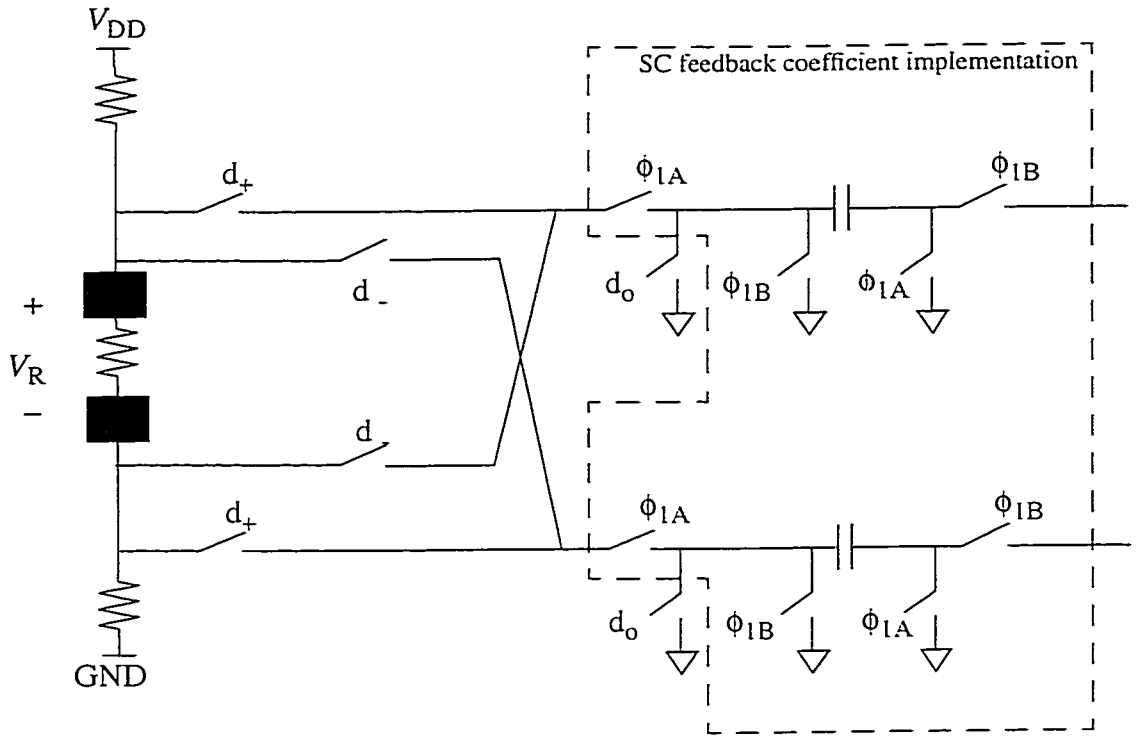


Figure 4.14 Tri-level differential D/A.

4.5 Conclusions

This chapter presented component level schematics of the modulator's building blocks: the resonator, op-amp, bias, CMFB, quantizer and comparator.

A novel double sampling four-phase resonator was presented in comparison to the existing circuits known in the literature. It offers the advantages of doubling the sampling frequency (a four-path technique is used) without more stringent requirements for the op-

amps, and it is capacitor-mismatch and path-mismatch insensitive because the same capacitor is used to transfer the charge from the input to the output, and not two different capacitors that transfer the charge from one to another as in the other existing circuits. The four-phase technique allows us to implement a two-delay circuit and therefore only three op-amps (instead of six) are required for the sixth order BP$\Sigma\Delta$ modulator.

A tri-level quantizer brings the benefit of improving the modulator's SNR and stability without introducing significant complexity in the quantizer circuit and in the decimation filter that follows the $\Sigma\Delta$ modulator.

The op-amps were optimized for speed because in a high-order modulator a very high DC gain is not required. Matlab simulations showed that a 50dB op-amp gain is enough to get nearly ideal SNR.

Chapter 5 Switches and Clock Generator

The switch is an important source of errors in SC circuits. For MOS switches the key errors are due to charge injection. Part of this charge injection is due to the overlap capacitance C_{ov} of the MOS transistor that makes the clock see a capacitor divider $\left(\frac{C_{ov}}{C_H}\right)$ with the holding capacitor C_H as shown in Figure 5.1.

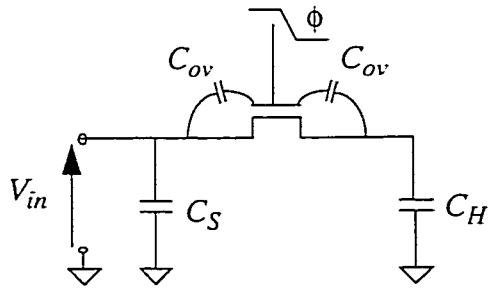


Figure 5.1 The overlapping capacitance of an NMOS switch.

This error is usually small compared to the charge injection due to the charge stored in the transistor channel, but in the Mitel process the effects are comparable (because the over-

lapping capacitors are approximately 30% of the total gate capacitance). Other sources of error in the switch operation are due to sampled thermal noise on the holding capacitor and the leakage current associated with the drain-to-bulk junctions. These are also small compared to the charge injection, nevertheless their effect is still important for high resolution circuits (≥14bits) because they are AC noise in the passband. The thermal noise from the first stage of the ΣΔ modulator has the largest contribution to circuit noise. For the next stages the thermal noise is shaped by the previous ones. This is another reason why the first stage should be the most carefully designed. The flicker noise (1/f) of the ΣΔ modulators is of little concern as it is well below the passband and will be removed by the decimation filters together with the out-of-band quantization noise.

The charge injected into the holding capacitor depends on the switch size and topology (i.e. NMOS gate, transmission gate, dummy switch), clock skew (delay and slope), circuit configuration (single-ended, fully differential, bottom plate sampling), the input voltage value, and the impedances seen on both sides of the switch. Nothing can offer perfect charge injection cancellation over all signal levels, but, by choosing among the switch circuits, one can minimize the effect on circuit's performance. This is a key issue for the ΣΔ modulator of this thesis because the three resonators of the modulator contain capacitors that are voltage driven at both ends preventing use of bottom plate sampling. Because the modulator was designed to work at the maximum clock frequency allowed by a given CMOS technology the switches are large relative to the sampling capacitors and their injected charge is accordingly significant.

5.1 Switches Configuration for Charge Injection Analysis

The resonator of Figure 4.4 uses a fully differential structure. If the charges injected to the differential capacitors are equal, then the resulting voltage is rejected as a common mode signal. But this is not the case for real circuits and the switching problem is complicated because the charge injection depends on the speed, slope and delay of the clock phases and on signal levels and impedances. Following the simulations and comparison, the main purpose of this chapter is to provide a framework for choosing the right delays and slopes of the clock phases and the best switch type such that the charge injection effect is minimized.

Three types of switches, recommended in the literature, were selected for testing charge injection into the resonator capacitors of Figure 4.4 (C_i, C_i', where i=1,2,3,4). These are shown in Figure 5.2 in a simplified single-ended version.

a) The first type of switch, shown at the top of Figure 5.2, assumes two matched NMOS switches. One might expect equal charge injection, Q_{inj}, from both switches which would cancel each other out. This is not true because, in general, the voltages $V_1 \neq V_2$ and there is more charge under the gate of the lower voltage side. Also, due to the finite slope of the clock, the higher voltage side switch turns off first; the first switch off sees a lower impedance on the sampling capacitor side and therefore it will inject more charge. This effect causes a strong S-shaped nonlinearity about $V_1 = V_2$.

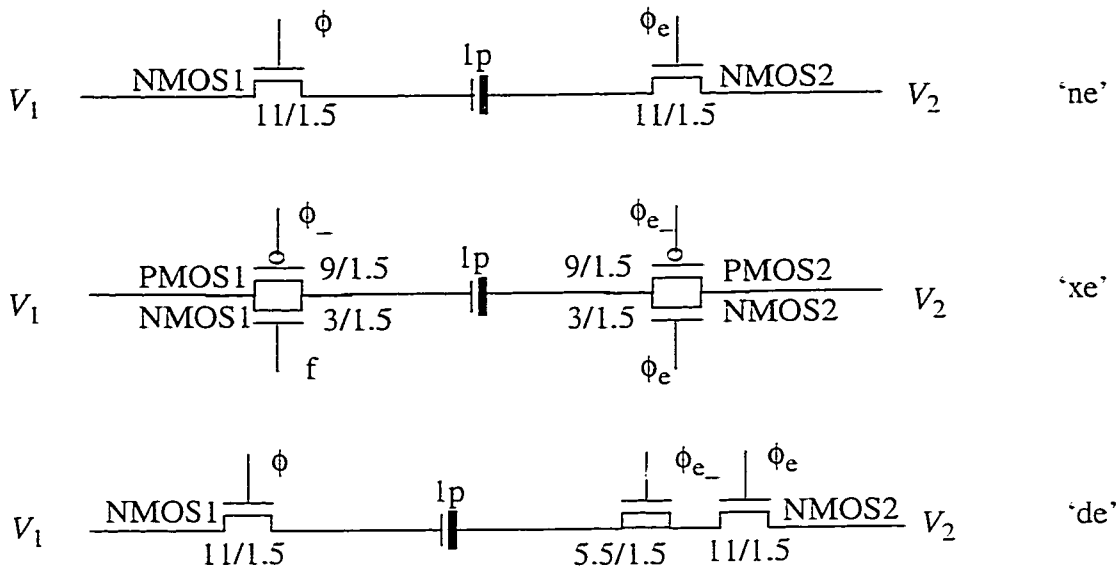


Figure 5.2 Simplified circuits for analysis of switches charge injection for NMOS (top), X-gate (middle), and NMOS with dummy (bottom) switches. The suffix 'e' denotes that an early version of clock is used. The 'bold' capacitor bottom plate has a parasitic capacitance of 100fF and a top plate parasitic capacitance of 10fF.

One method to solve the problem is to use an early version of the clock, ϕ_e, that turns off one side, say the right hand side, first. If V_2 is constant this is called "bottom-plate sampling" and the charge injection effect is only an offset voltage.

Because the NMOS switch is not good close to V_{DD} where it is strongly non-linear and has big "ON" resistance that results in loss in the dynamic range, we moved down the common-mode voltage from $V_{DD}/2 = 2.5V$ to 2.3V.

The switches were designed for $\tau = 2R_{ON}C \leq 40ns/7$, so that their on-resistance $R_{ON} \leq 2.85k\Omega$ (or $g_{DS,N} \geq 350\mu S$) which resulted in a 11μm/1.5μm NMOS transistor (see the

upper curve $g_{DS.N}$ of Figure 5.3). This gives a gate-channel capacitance of approximately 20fF, or 2% of the sampling capacitor.

b) The second switch type, shown in the middle of Figure 5.2, uses a smaller 3µm/1.5µm NMOS switch in parallel with a 9µm/1.5µm PMOS which compensates the poor behaviour at high voltage of the n-channel device. The result is a transmission gate or X-gate. Figure 5.3 shows how the g_{DS} of the PMOS and NMOS devices add to form $g_{DS.X}$ of the X-gate.

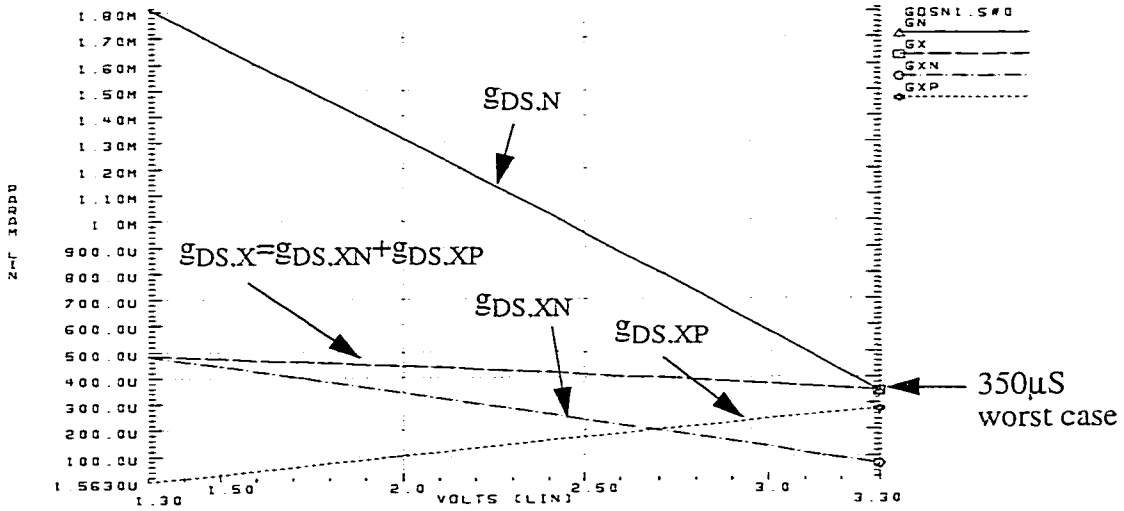


Figure 5.3 g_{DS} vs voltage(1.3V to 3.3V) for NMOS and X-gate of Figure 5.2

Since there are two opposing clock charge injections it might be anticipated that the claim for the X-gate is that the PMOS channel charge cancels the NMOS one. This is not true in general because of the opposite voltage dependence of channel charge of the two complementary devices. Charge injection cancels out only at one voltage. Also the transistors turn off at different times, which results in different injected charges.

c) The third switch type, shown at the bottom of Figure 5.2, attempts charge injection cancellation by adding a half-size dummy switch to cancel the charge injected in the sampling capacitor by the main switch. The dummy switch works ideally for an infinite-speed clock where half of the channel charge goes in each direction, but this is not the practical case. With finite clock slope, injection is a function of impedances at the source and drain, which are different for the switch and dummy.

The simulations were carried out in HPICE for a fully differential test circuit that models the impedances at the switch terminals for the difficult case of signals on both V_1 and V_2. Figure 5.4 shows the case of two op-amps of the modulator where the switches are simple NMOS gates. The op-amp circuits are those of Figure 4.7 and they realize the driving impedances seen by the switches in the sixth order ΣΔ modulator designed. This is significant because the charge injected by a switch depends on its impedances [Vittoz85].

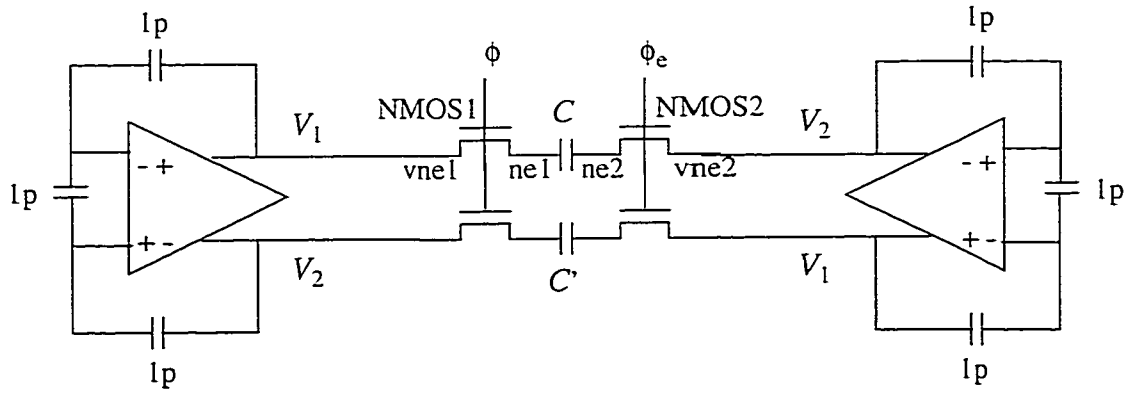


Figure 5.4 Fully differential test circuit for the NMOS switches charge injection.

All the capacitors are taken to be 1pF, a typical value for the capacitors of the modulator designed. The switch sizes were calculated for the worst case conductance such that they

can charge the 1pF capacitor to 0.1% of the final value. This error value (0.1%) is much smaller than that due to charge injection and comparable to the finite op-amp gain error. The conductances for the 11µm NMOS switch and 9µm-PMOS/3µm-NMOS transmission gate are shown in Figure 5.3.

The clock phases ϕ, $\phi\_$, ϕ_e and $\phi_{e\_}$ are generated using inverters, as shown in Figure 5.5, that model those used in the modulator's clock generator. A study of the effect of slope and time delay of the clock phases is required in order to choose and implement the best possible modulator design strategy. For this the W_{PMOS}/W_{NMOS} widths transistor ratios in inverters were chosen to be all 15/5 for a high slope (≅25V/ns). To generate clock phases with a lower turn-off slope (≅5V/ns) inverters corresponding to ϕ and $\phi\_$ were designed with a 150/5 ("weak NMOS") or 15/50 ("weak PMOS") ratio. The clock generator and the waveforms for the higher slope case are shown in Figure 5.5.

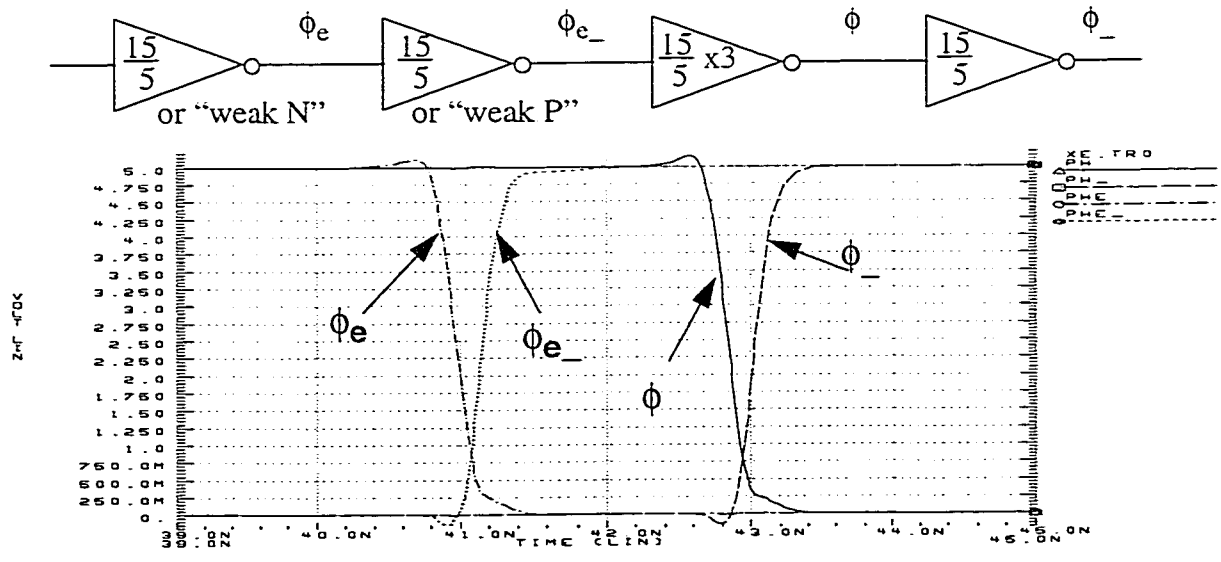


Figure 5.5 Clock circuit and waveforms for "higher slope" clock phases.

The voltages V_1 and V_2 of Figure 5.2 corresponds to the differential ones, V_i and V_o, of Figure 4.4. The switches are turned off for swept values of V_1 and V_2 in the 1.3V-3.3V range with a fixed 2.3V common mode as shown in Figure 5.6. For example, when V_1 is 1.3V, V_2 is 3.3V; when V_1 is 1.31V V_2 is 3.29V, and so on. For each such measurement the voltage due to charge injection effect was recorded. The final voltage across the 1pF capacitor is

$$V_{final} = V_1 - V_2 - \Delta V_{\substack{charge \\ injection}} \qquad \text{EQ 5.1}$$

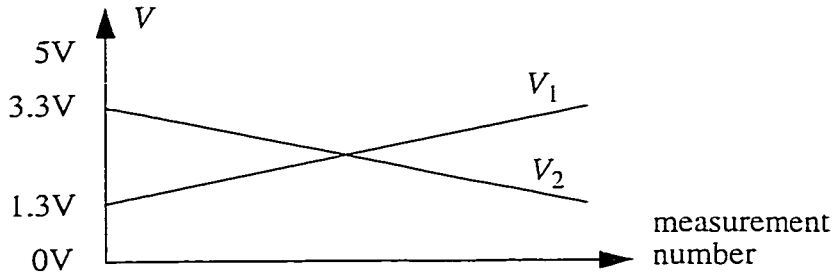


Figure 5.6 The voltages V_1 and V_2 that charge the capacitor.

Doing the test this way highlights the charge injection effects so they can be better understood. When increasing the voltage on one side, the voltage on the other side is equally decreased, therefore the switches are turned on and off in a different manner (they have different on-resistances and gate-to-source voltages). When a switch is strongly turned on, the other side switch is just weakly on. They turn off at different times due to their different threshold voltages. Thus the extreme situations are reached and this is a worst-case study.

The case where one side has a constant voltage or both voltages are equal (and vary in the same way) are already studied in the existing literature and don't represent the worst case for the resonator of Figure 4.4.

5.2 The Switch Analysis

An important role is played in this analysis by the threshold voltage dependence of the switched voltage V_{sw} (either V_1 or V_2) due to the body (or backgating) effect:

$$V_t \approx V_{to} + 0.12 \cdot V_{sw} \qquad \text{EQ 5.2}$$

where $V_{to} = 0.85\text{V}$ is the threshold voltage for $V_{sw} = 0$; (this is a rough formula for the Mitel NMOS transistor). This dependence reflects in the expression of the voltage error of EQ 2.15. The charge stored in the transistor channel is

$$Q_{ch} = C_G(V_{DD} - V_{sw} - V_t) \qquad \text{EQ 5.3}$$

where C_G is the gate capacitance and V_{DD} is the highest value of the clock.

Figure 5.7 shows the phases, ϕ_e and ϕ, turning off NMOS switches. Defined are the times, $t_{off,NMOS1}$ and $t_{off,NMOS2}$, at which the transistors turn off after the beginning of the falling clock edge. The switches turn off when their V_{GS} is less than their threshold voltage, that is when the clock reaches $V_{sw}+V_t$. The time between the moments when the transistors turn off is Δt. This signal dependence of turn-off time affects both the sampling instant and charge injection.

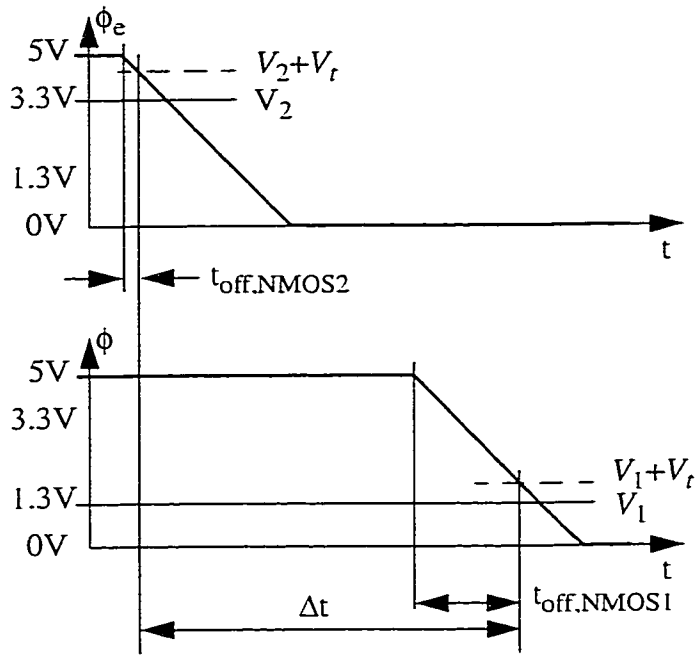


Figure 5.7 The clock phases for the NMOS switches defining the off-times.

The NMOS Switch

In this section an analysis is done for an NMOS switch that is turned off by a slow clock. Figure 5.8 was obtained from a series of HSPICE simulations of the circuit of Figure 5.4. The vertical axis is the voltage error $\Delta V_{\substack{\text{charge} \\ \text{injection}}}$ due to the charge injected in the top capacitor C (connected between nodes 'ne1' and 'ne2'). Due to circuit symmetry the charge injection curve for C' can be found by flipping the curve for C from left to right. The time delay between ϕ and ϕ_e is approximately 2ns. The differential injected charge (from C- C') is symmetrical referred to the origin and, though small, is signal-dependent and nonlinear as shown in Figure 5.8.b. The common mode part of the total charge injection (from C and C') is rejected by the fully-differential structure, so the even terms of the charge injection

are cancelled by the fully-differential structure. The gain of the single-ended test circuit is 0.25% high (10mV/4V from the simulated charge injection curve for *C*) with a small non-linearity of approximately 1mV, that is 0.025%. The curves are corrupted by simulator numerical "noise" at about the 1mV level.

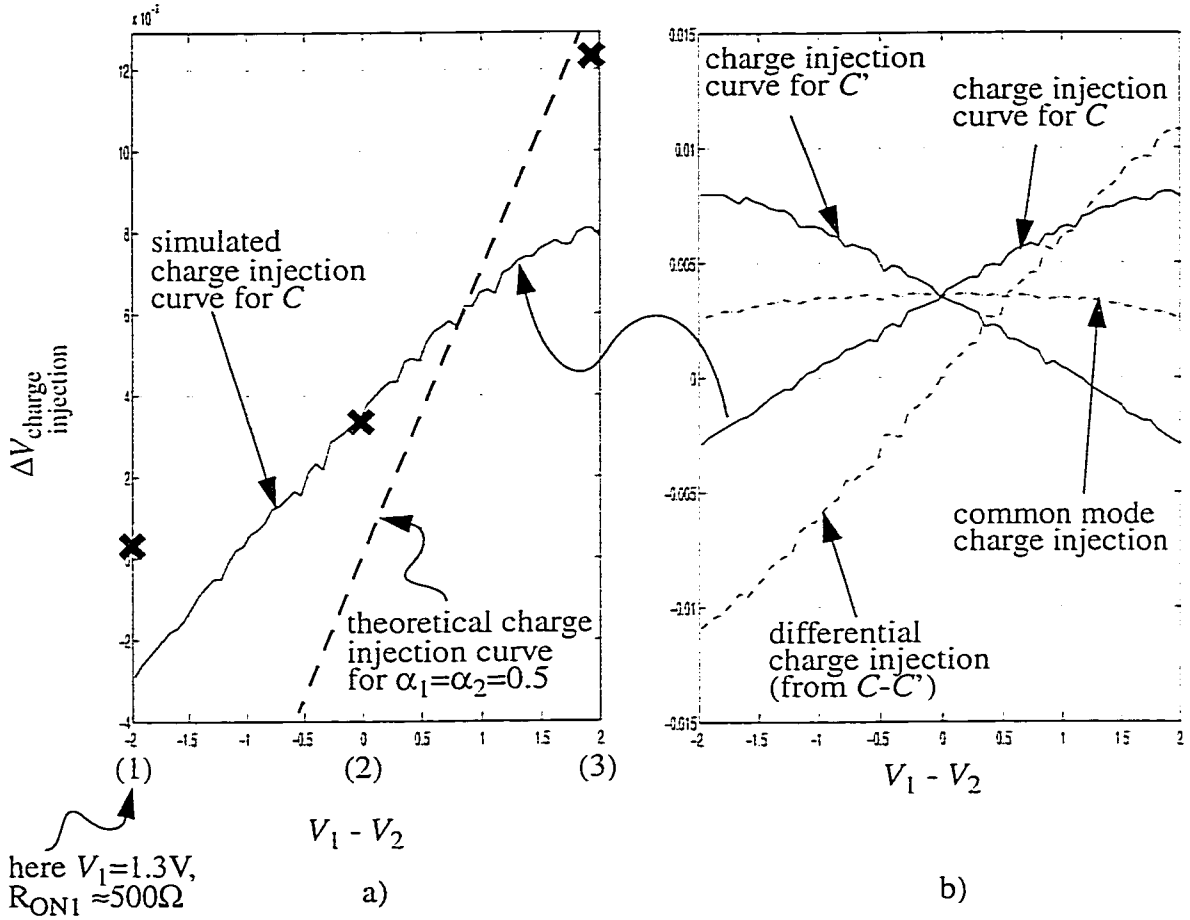


Figure 5.8 The charge injection voltage due to NMOS switches. The points marked '**x**' are theoretical estimates based on the charge-sharing model of Vittoz.

Figure 5.8 summarizes the results of a collection of transient simulations like that of Figure 5.9, for which V_1-V_2 = 2. Node names are defined as in Figure 5.4. The detailed

behaviour is quite complex, with a net error (8mV in Figure 5.8.a) formed as a difference of several terms. We will show an approximate analysis to help in design.

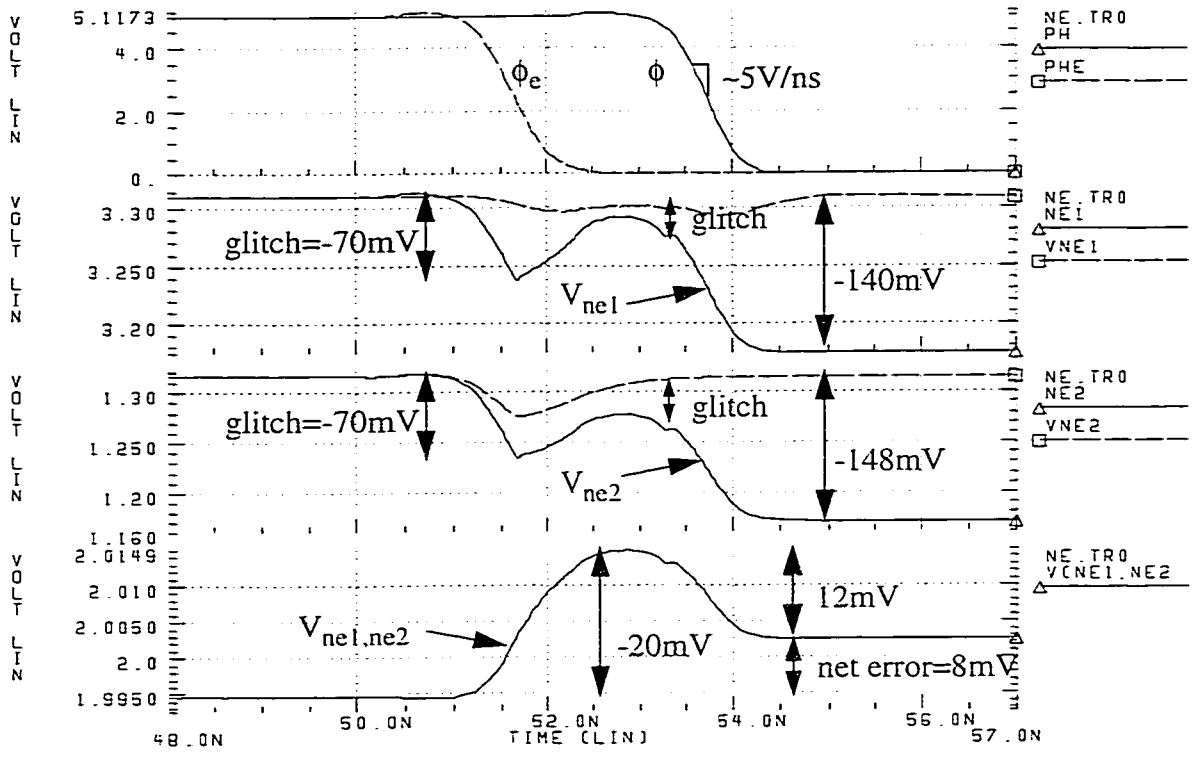


Figure 5.9 HSPICE waveforms for case (3) where V_1=3.3V and V_2=1.3V (clock is the top curve). This case was shown because the glitches are the most noticeable.

We model a transient as having four regions, two for each switch turn-off. The behaviour of the switch as the gate voltage drops from V_{DD} to (V_{DD}-V_{sw}-V_t), at which point it is just "off", is modelled accordingly to the charge-injection model of [Vittoz85] (see section 2.4); its behaviour as the gate voltage drops the rest of the way to V_{SS} is modelled as a simple capacitor divider between overlap capacitance and the load.

Table 5.1 Models and formulae used for charge injection prediction.

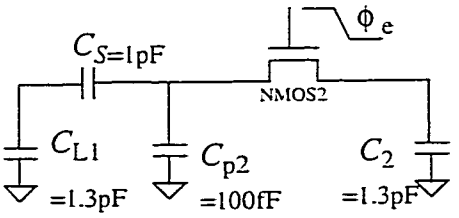
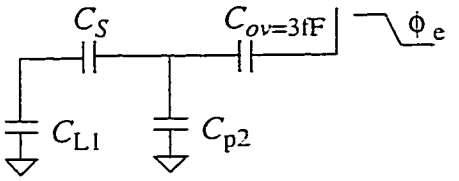
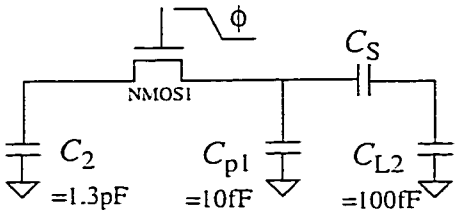
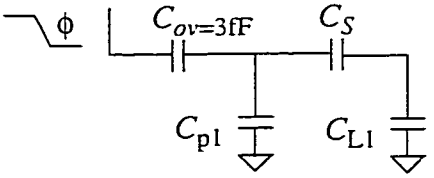
Switch states	**circuits**	**charge injection**
ϕ_e -ON		$\alpha_2 C_G(V_{DD}-V_{t2}-V_2)/1.1$ $=\alpha_2$ [75 fC- (20 fF) V_2]
ϕ_e -OFF		$C_{ov}(V_{t2}+V_2)/1.1$ =2.3 fC + (3 fF) V_2
ϕ -ON		$\alpha_1 C_G(V_{DD}-V_{t1}-V_1)/1.1$ $=\alpha_1$ [75 fC- (20 fF) V_1]
ϕ -OFF		$C_{ov}(V_{t1}+V_1)/1.1$ =2.3 fC + (3 fF) V_1
net		(-75 fC) (α_1 -α_2) + (20 fF) ($\alpha_1 V_1$ - $\alpha_2 V_2$) - (3 fF) (V_1 - V_2)

Table 5.1 shows the models used and formulae for the predictions of components of charge injection, where α_i is the charge injection ratio on the y-axis of Figure 2.11 in each

case.The "1.1" denominator in the charge injection formulae reflects charge splitting between parasitics and the sampling capacitor. For the particular values of the parasitics, which were estimated as 10% of C_S for the bottom plate and 1% for the top plate, this makes a split of roughly 90:10 to the sampling capacitor. Figure 5.8.a includes a theoretical curve, represented with a dotted line, obtained with these formulae when $\alpha_1 = \alpha_2 = 0.5$. It exaggerates the slope by a factor of about 2.

Table 5.2 contains the calculated values for α_i according to [Vittoz85] or Figure 2.11. The three corresponding theoretical values for net charge injection are marked ("x") on Figure 5.8.a., and improve the fit substantially.

Table 5.2 Charge splitting coefficients from [Vittoz85].

case#	V_1-V_2	α_1	α_2
1	-2V	0.21	0.497
2	0V	0.37	0.485
3	+2V	0.465	0.46

The theoretical model is very sensitive to α_i and the right values to match the transient simulations is hard to estimate. The theoretical predictions are high, because the impedances seen by the switch are not the simple capacitors of [Vittoz85].

A better model, Figure 5.10, shows that the impedance at the left of NMOS2 is intermediate between C_{1B} and C_{1A}+C_{1B}, depending on the relative time constants for NMOS2 and $R_{EQ1}C_{1A}$. This in turn affects the proportion α_2 of charge injected by NMOS2. Because R_{EQ1} is function of V_1, this is also signal-dependent.

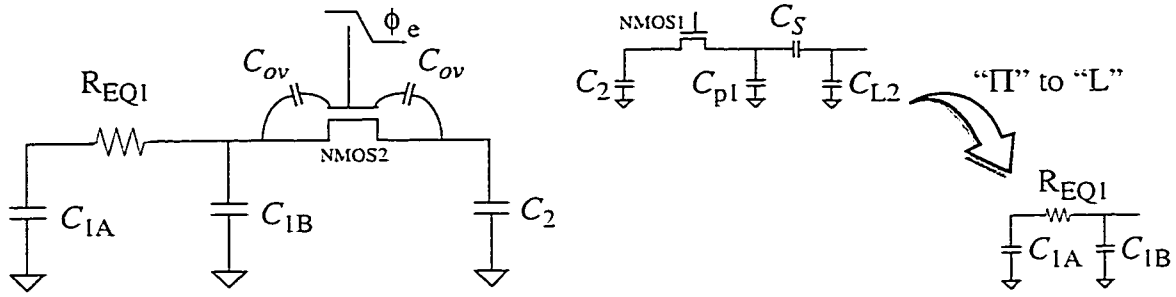


Figure 5.10 Realistic model for the side impedances. The "Π" to "L" transformation of [Romanowitz71] makes equivalent the left-hand-side circuits of NMOS2 as shown by the arrow.

Figure 5.11 is from a transient simulation similar to that of Figure 5.9 with the difference that the NMOS1 switch is replaced by a short-circuit. The two figures should be compared up to 53ns, after which the lack of NMOS1 makes the rest irrelevant. Notice that without NMOS1 the voltage error due to charge injected on ϕ_e is 8mV bigger. This is because R_{ON1} increases impedance in the initial transient for the left-hand-side of NMOS2 and this introduces an offset in the charge injected curve. The 'ON' resistance of NMOS1 is a non-linear function of V_1 and this results in the lower slope for the curve of Figure 5.8.a when V_1-V_2 value is closer to +2V (the curve is bent downward).

The causes of charge injection curve nonlinearities are, on one hand, from the dependence of the channel charge on the nonlinear threshold voltage, and on the other, from the α_1 coefficients dependence on V_1 (by way of R_{ON1} is nonlinear with V_1), and on V_2 that is enclosed when defining the switching parameter B, the horizontal axis of Figure 2.11. While these effects bias the results, the analysis can be used to gain a general understanding of the problem and to study design trade-offs.

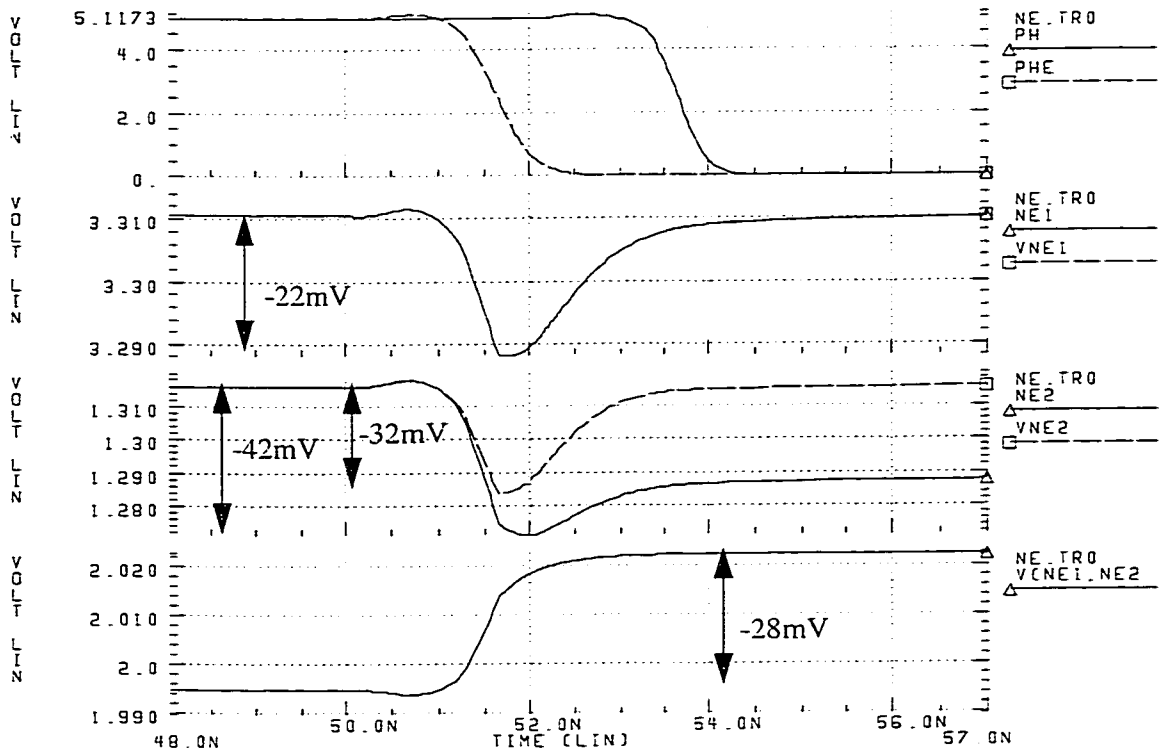


Figure 5.11 HSPICE waveforms when NMOS1 is replaced by a short-circuit.

The simulations shows that the charge injection introduces a gain error of 0.25% and non-linearity of about 1mV level. A 1mV non-linearity causes a serious charge injection problem and the next sections will provide solutions to make this non-linearity as close to "0" as possible. A simple analysis with equal charge injection splitting (50%-50%) is off by a factor of two, and the literature model is closer but also off because of the R_{EQ1} which increases the left-hand-side impedance.

The X-gate Switch

In the transmission gate the charge injected by the NMOS transistor is partially compensated by the charge from the PMOS transistor. This compensation is ineffective because

of the poor matching of the complementary devices. Moreover the charge compensation is signal dependent and sensitive to clock jitter between the two complementary phases.

Figure 5.12 shows the charge injection results with clocks designed so that nonlinearities of signal-dependent turn-off timing effects are minimized.

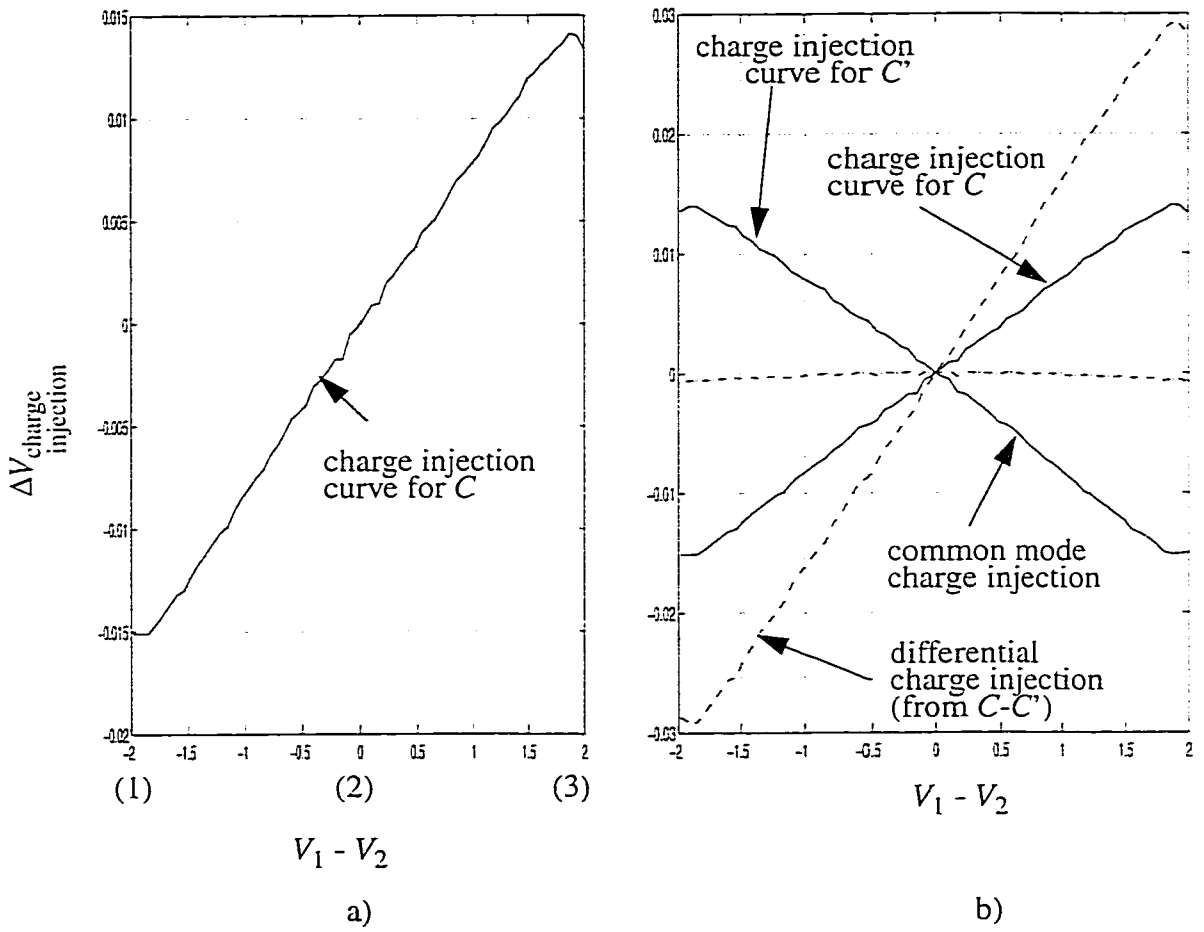


Figure 5.12 The charge injection voltage due to X-gate switches.

To explain the shape of the curve of Figure 5.12.a we can make use of the simulated curve of Figure 5.8.a. Combining that curve, but for scaled 3μm/1.5μm NMOS switches, to the

complementary curve for the 9μm/1.5μm PMOS switches only results in a curve like that of Figure 5.12.a in that it is slightly bent at both ends.

The errors introduced by the X-gate are roughly 0.75% for gain and 0.05% for nonlinearity, three times worse than the NMOS switch. By tuning the slope (section 5.3) and the time delay (section 5.4) one can linearize the mid-portion [-1.5V,1.5V] of the charge injection for a general curve like that of Figure 5.12.

The NMOS Gate with Dummy Switch

The half-sized dummy switch can compensate half of the channel charge of NMOS2 if turned on immediately after NMOS2 turns off. The charge injection is nulled if the channel charge of NMOS2 is equally split on both sides of the switch. This can only be achieved for a very fast clock, or for a slower one but with equal impedances around the switches — neither case being practical.

The simulated switching circuit is the "de" configuration of Figure 5.2. The curve's variation of Figure 5.13 is very small, in a 2mV range, and the nonlinearity is about the 1mV level, the same as the single NMOS switch ('ne' circuit), and with roughly twice the offset but a much smaller gain error. The dominant component in the nonlinearity is quadratic and the third order term is approximately half of that.

To be effective the dummy switch should be turned on simultaneously or after NMOS2 turns off. If the dummy turns on first the charge injection is the same as in the single NMOS switch case because its charge leaks out through NMOS2 to V_2. In the simulated

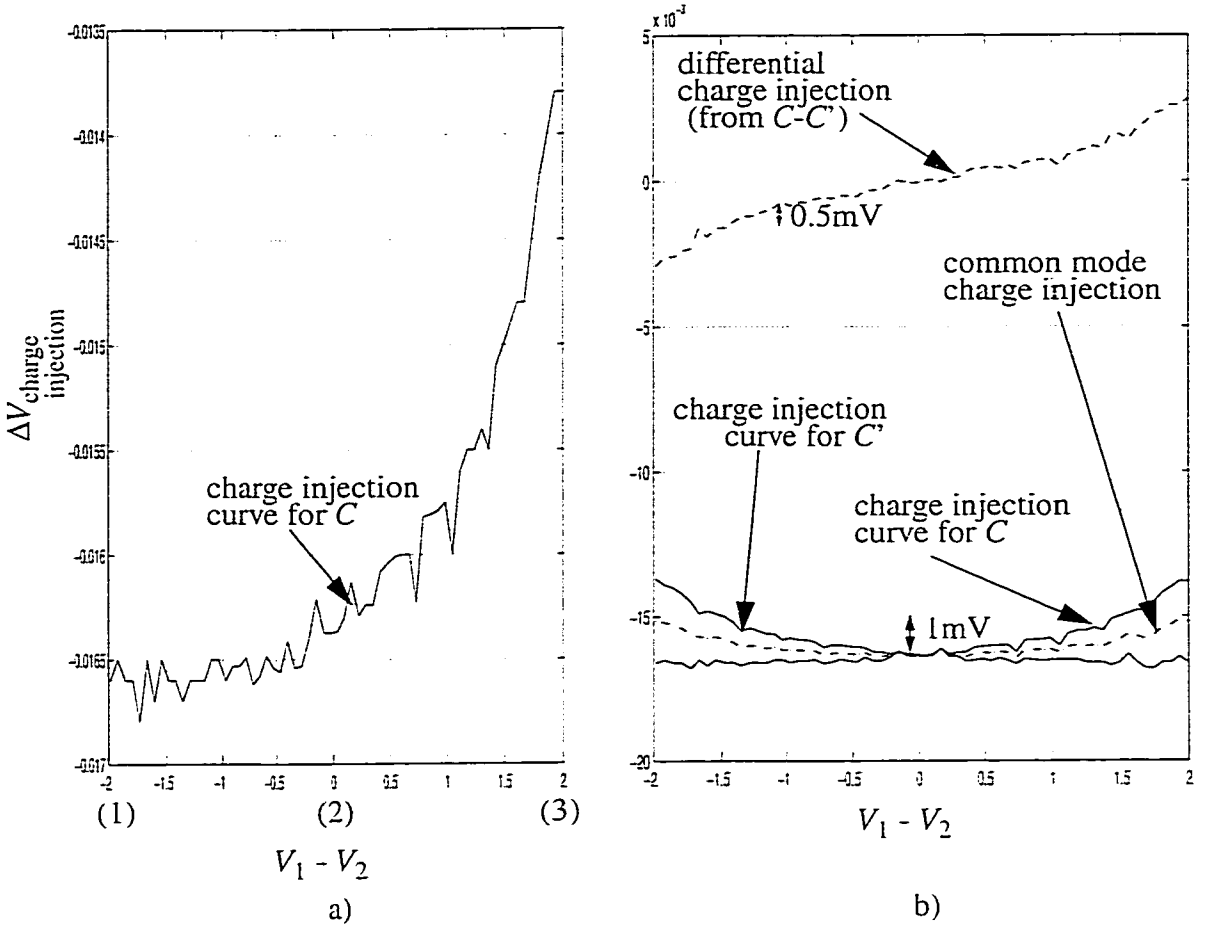


Figure 5.13 The charge injection voltage due to dummy switch compensation.

'de' circuit the dummy transistor turns on after NMOS2 turns off and the total injected charge is increasing with V_2 decreasing. This reinforces the dummy switch behaviour as described in [Eichenberger89] for positive time delay, t_d, comparable to the fall-time of the clock.

Figure 5.14 shows how t_{onoff}, the time between NMOS2 turns off and dummy turns on, increases with V_2 increasing.

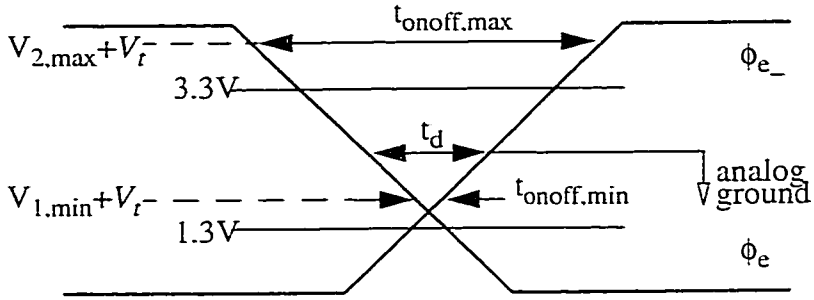


Figure 5.14 The qualitative clock phases for the NMOS switch with dummy. For $t_{onoff.max}$ the dummy compensates most of the NMOS2 charge. For $t_{onoff.min}$ the dummy compensates and adds extra to the charge from NMOS2.

The charge injection (vs V_2) from NMOS2 can be largely counterbalanced by the compensation charge from the dummy, and the result is a reduced dependence of the total charge injection on switched voltage. Linearization of the charge injection can be done by adjusting the time delay t_d between the falling ϕ_e and rising $\phi_{e\_}$ measured at the analog ground level (section 5.4).

The mismatch between the dummy and the main switch is not considered of big concern since it is constant and a very careful layout design can make this mismatch very small.

5.3 The Effect of Turn off Slope

Adjusting the turn off slope of the switching phases affects, in general, the injected charge by a switch into a capacitor depending on the impedances ratio on both sides of the switch [Vittoz85]. Only if these impedances are equal does the injected charge not change with clock slope. For different impedances, the charge injection is smaller in the higher imped-

ance side of the switch. Figure 2.11 in association with EQ 2.14 play an important role in highlighting this, so they are repeated as Figure 5.15 and EQ 5.4.

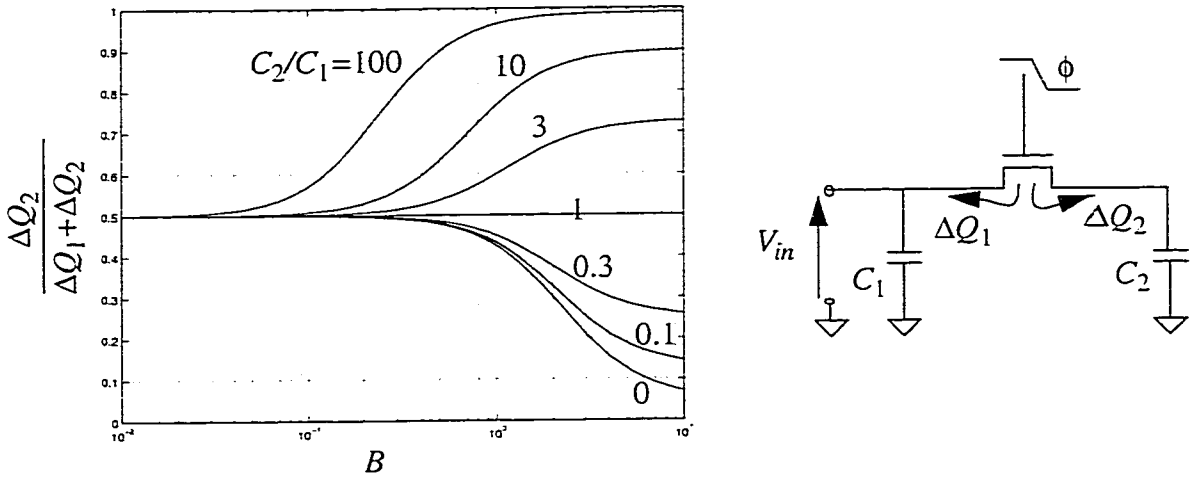


Figure 5.15 Charge injection chart according to [Vittoz85] and the corresponding circuit.

$$B = (V_{DD} - V_{in} - V_t)\sqrt{\frac{\beta}{aC_2}} \qquad where \qquad \beta = \mu C_{ox}\frac{W}{L} \qquad and \qquad a = slope(V/ns) \qquad \text{EQ 5.4}$$

For all the switch types, the clock slope doesn't change much the shape of the charge injection curves as shown in Figure 5.16. Increasing the clock slope decreases the switching parameter, *B*, given by EQ 5.4, therefore the charge split will be closer to the 50%-50% case. We can notice that the curve of Figure 5.16."ne" corresponding to the fast clock approaches the theoretical charge injection curve of Figure 5.8.a. The same effect can be observed for the X-gate and dummy switches in Figure 5.16."xe" and "de". The higher the clock slope the straighter are the charge injection curves. This is because the driving impedances matter less and less in splitting the charge which goes almost equally to each side.

Figure 5.16 "de" shows the sensitivity to slope when dummy switch is used. This is true only for values of the time delay t_d comparable to the fall-time.

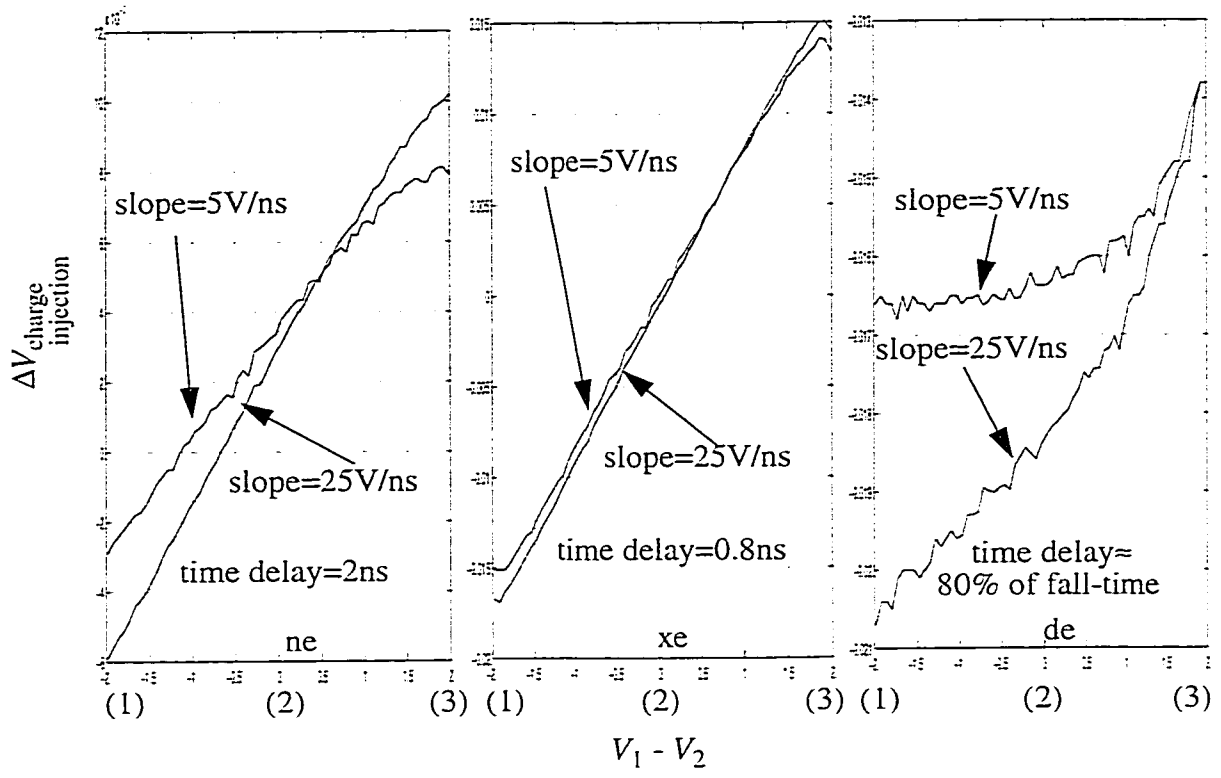


Figure 5.16 Slope effect on charge injection.

Concluding the above, we can increase the clock slope to make the charge injection more linear with the signal. But, as we will see in the next section, this is only part of the solution.

5.4 The Effect of Time Delay

For the curve of Figure 5.17"ne" the time delay is measured between ϕ and ϕ_e. Making the time delay bigger allows the switches to complete their channel charge transfer to the sam-

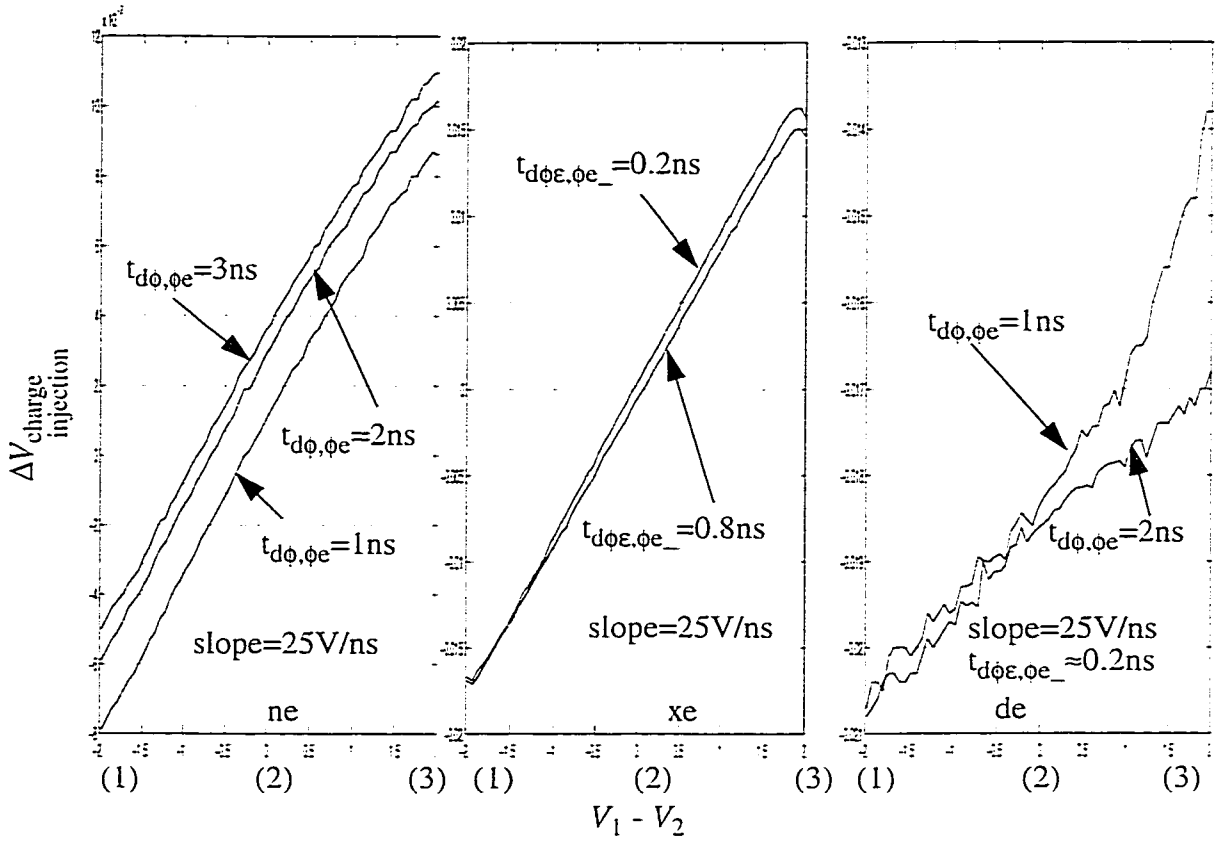


Figure 5.17 Time delay effect on charge injection.

pling capacitor. Therefore the charge injection will be bigger and the charge injection curves have bigger offset.

For the curves of Figure 5.17"xe" the time delay was considered between ϕ_e and $\phi_{e\_}$(varying the delay between ϕ and ϕ_e introduces an offset only as in the "ne" case). Simulations showed that roughly adjusting this time delay in -1ns to 1ns range doesn't bring any significant improvement when using X-gate switches.

Things are different for the dummy switch. For a high clock slope, a time delay between ϕ_e and $\phi_{e\_}$ comparable to the clock fall time and a time delay between ϕ and ϕ_e large

enough (2ns in this case) the charge injection curve can be linearized as seen in Figure 5.17"de". This is due to the fact that, when V_1 is closer to 3.3V where the time constant is the biggest, just after ϕ_e turns off, the dummy switch has more time to fully discharge into the sampling capacitor. The transient simulation that shows this can be observed in Figure 5.18 for the two curves with $t_{d\phi,\phi e}$ of 2ns (top) respectively 1ns (bottom) and for the three cases when V_1-V_2 = -2V, 0V and +2V.

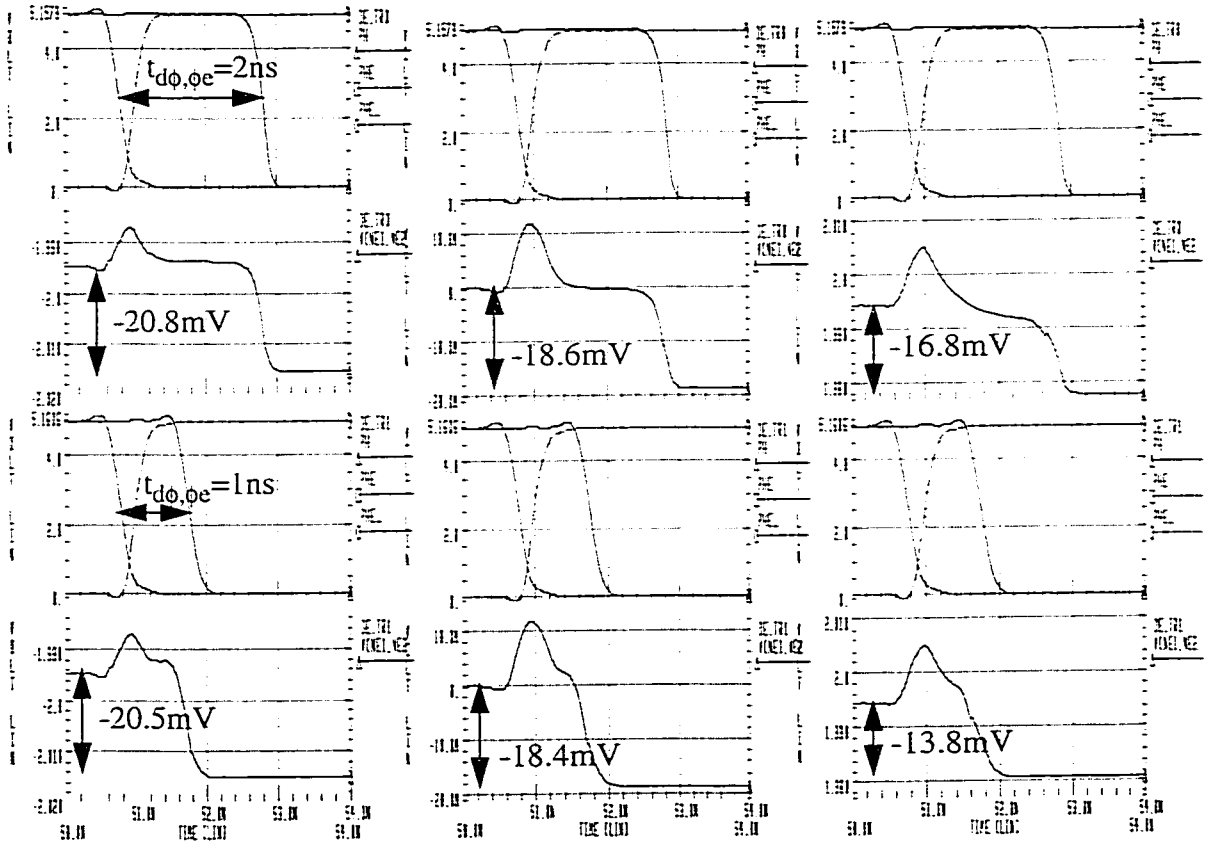


Figure 5.18 Comparison of the 1ns vs 2ns time delay curves in cases (1) (2) (3). The clock has a slope of 25V/ns with a time delay between ϕ_e and $\phi_{e\_}$ of 0.2ns measured at analog ground level ($t_{d\phi e,\phi e_} \approx 0.2$ns).

5.5 Proposed Switch

It's noteworthy to mention how the different types of switches perform when an early version of the clock is not used (all the switches are simultaneously clocked). The voltages due to charge injection effect are shown in Figure 5.19. The switch which has the higher threshold voltage will turn off first hence it dominates the amount of injected charge. Consequently an 'S' shape curves result. For the dummy switch (case "d") the shift from the horizontal axis is due to the asymmetrically placed dummy transistor that compensates charge from only one side.

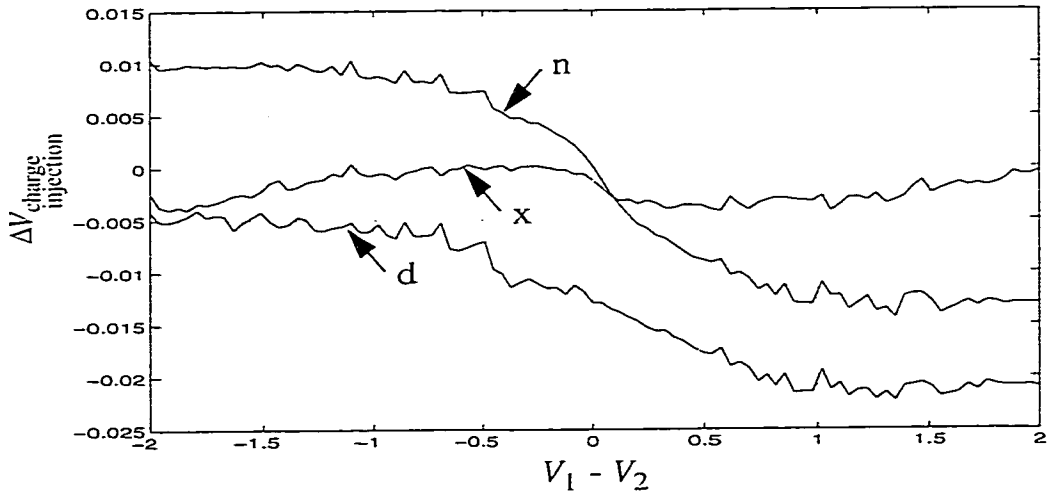


Figure 5.19 Charge injection curves without early clock phases.

The use of the early version of clock phases is effective when combined with the bottom plate sampling technique. But this cannot be applied when both ends of capacitor are voltage controlled. Among the "ne", "xe" and "de" switches the last one can be linearized by tuning the time delay $t_{d\phi,\phi e}$ and using a clock slope that is as high as possible. The "ne"

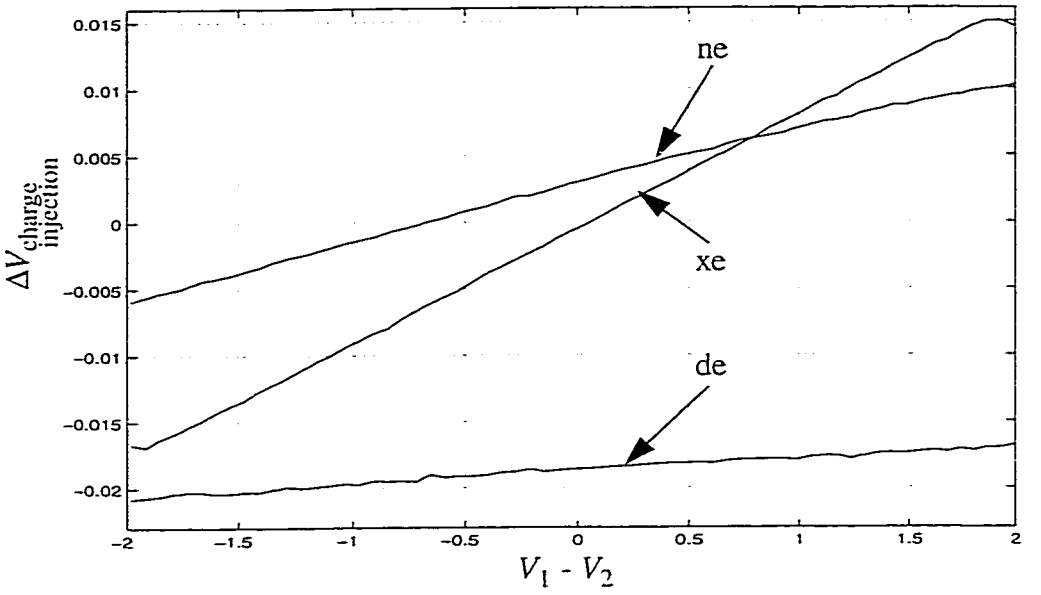


Figure 5.20 The best case among the three switches studied is the dummy switch.

switch cannot be linearized by any of the techniques proposed in this thesis, and the "xe" one can be linearized only for a smaller range of the switched voltage. Figure 5.20 shows the curves that led to choosing the dummy switch for the resonator of the sixth-order bandpass ΣΔ modulator designed.

5.6 The Clock Generator

Clock design is a critical issue for SC circuits. Even on-chip clock generators cannot deliver the exact needed phases. The capacitive loading and the long clock line parasitics degrade the fall and rise characteristics of clock phases, and this can lead to overlapping for a crudely designed clock generator.

The modulator requires a two-phase non-overlapping clock for op-amp SC common-mode feedback and comparators, and four-phase non-overlapping clock for the resonators. The clock for the comparator and its latch reset was designed such that the comparator decision is fully delivered to the feedback capacitors. The SC circuits can work at a maximum clock rate but also at a lower one at the expense of bandwidth. Hence, the clock generator was designed to ensure non-overlapping phases and the right timing for any working frequency of the modulator.

5.6.1 Non-Overlapping Clock

The circuit of Figure 5.21 [Martin80, Domenik81] generates a two-phase non-overlapping clock, ϕ_1 and ϕ_2, with a non-overlapping time of three gates delay. A bigger non-overlapping time can be achieved by adding more inverters and/or resizing the devices. The input clock, "ck" and "ck_", can be obtained from the outputs of a D flip-flop (which usually are overlapping), or "ck_" can be simply obtained from ck using an inverter.

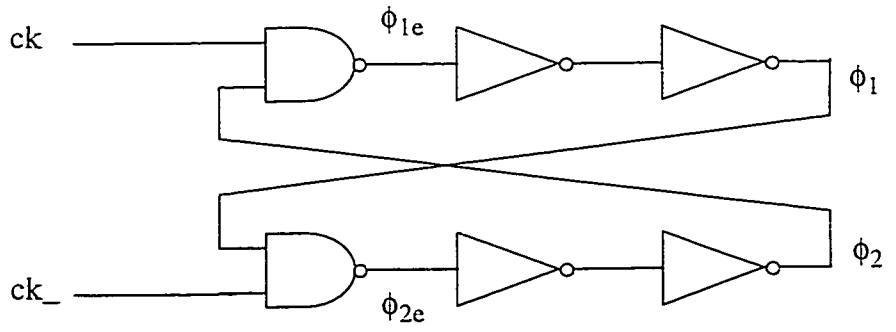


Figure 5.21 Typical two-phase non-overlapping clock generator.

5.6.2 Four-Phase Non-Overlapping

The four-phase non-overlapping clocking scheme of Figure 5.22 is derived from the two-phase non-overlapping clock. The input ($\phi_{1Aov\_}$, $\phi_{2Aov\_}$, $\phi_{1Bov\_}$ and $\phi_{2Bov\_}$) consists of four-phase clocks that can be overlapping. A way to generate these phases is using a four D flip-flop ring, but this requires proper initialization (only one of the flip-flop output should be on "high" at a time; the input phases are the $\overline{Q}$ outputs of each flip-flop) and, if one of the flip-flop state goes wrong, it cannot recover. Other way is using a 2-bit synchronous counter followed by a 'one-hot' decoder. The inverters marked 'N' and 'P' have augmented their NMOS, respectively PMOS device widths in order to ensure a sharp clock edge and an adequate non-overlapping gap.

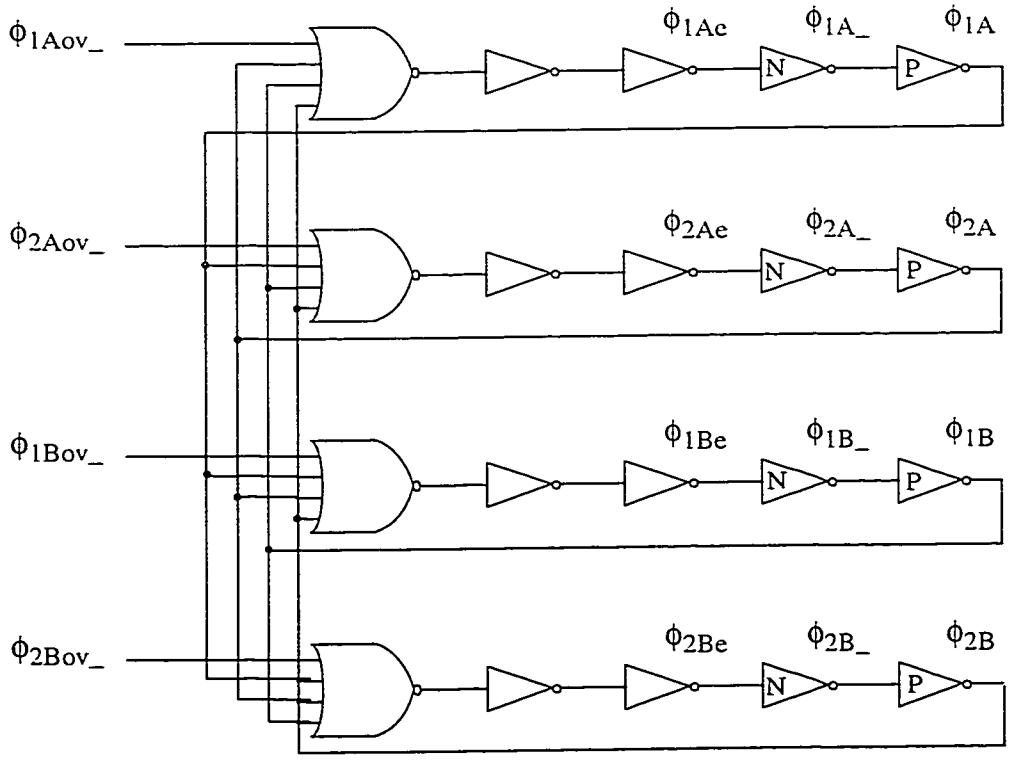


Figure 5.22 Four-phase non-overlapping clock generator.

5.6.3 The Clock Drivers

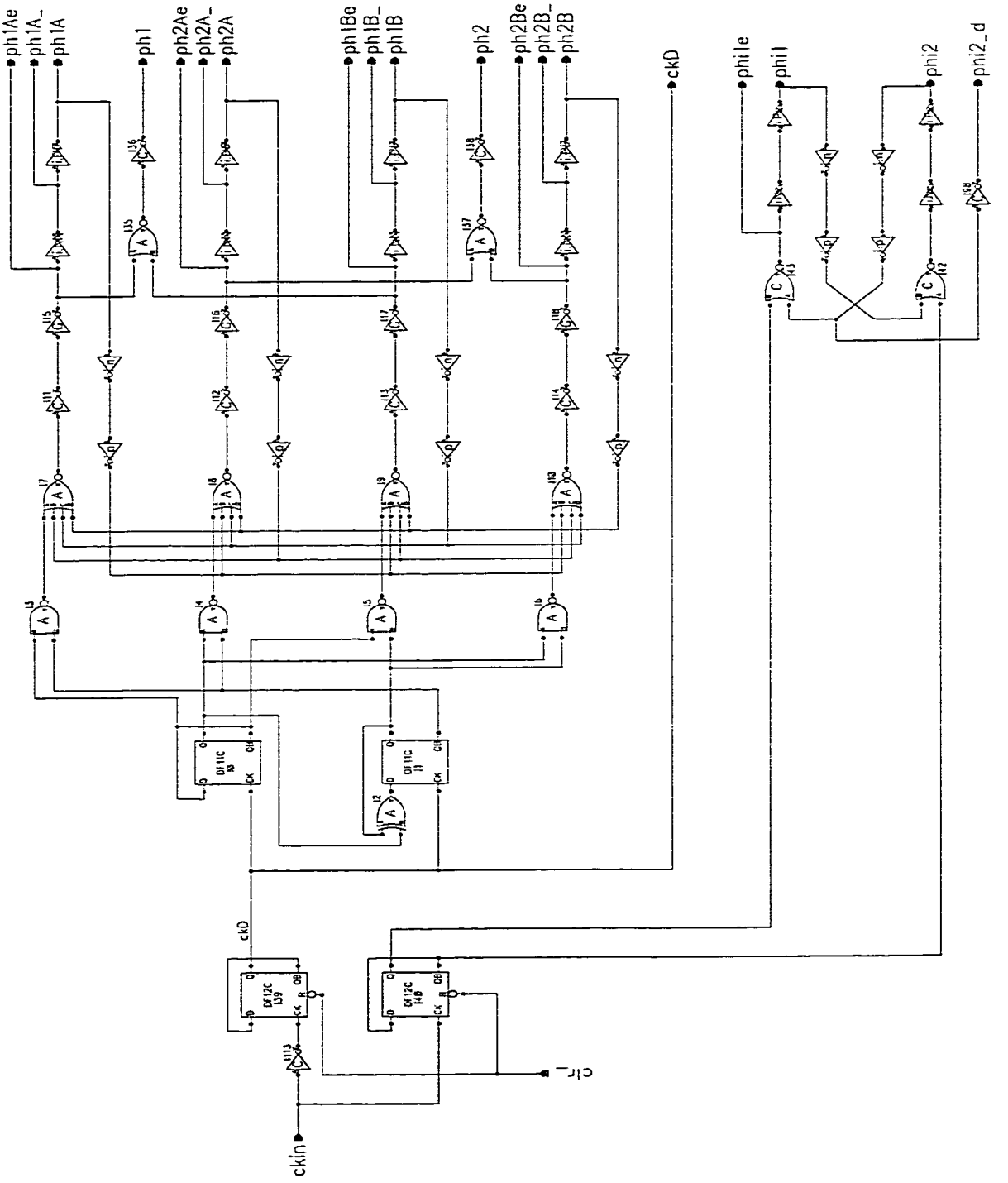


Figure 5.23 The whole clock generator.

All the clock phases needed by the ΣΔ modulator are generated by the circuit of Figure 5.23 (notation: 'phi' for comparators and 'ph' for the rest). The primary clock waveforms are shown in Figure 5.24.

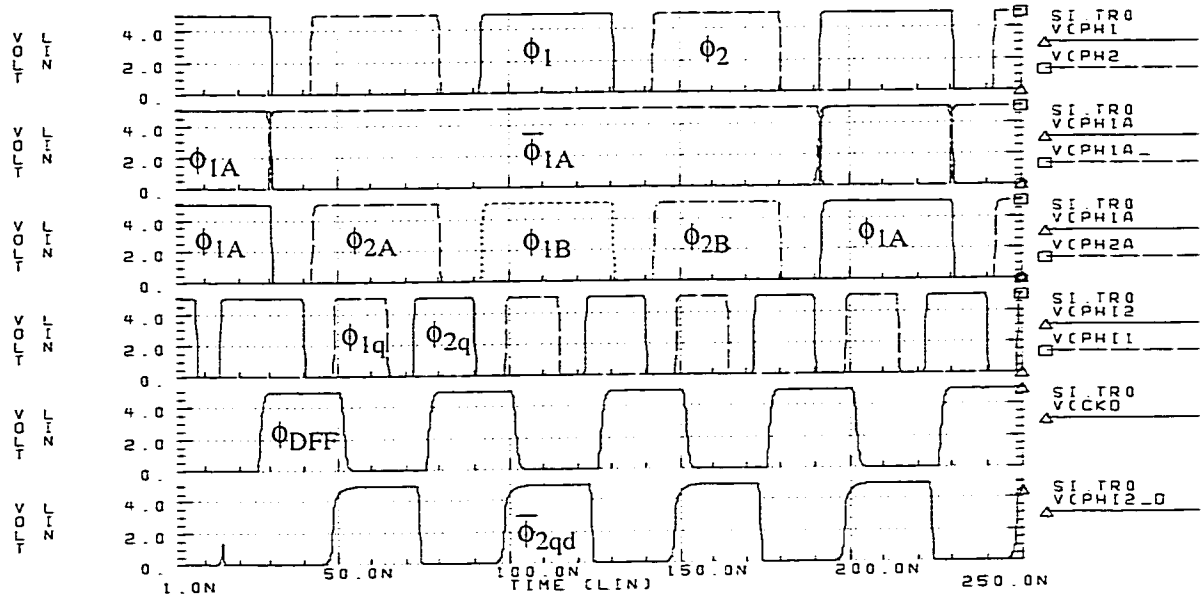


Figure 5.24 Clock waveforms.

5.7 Conclusions

This chapter depicted the charge injection problem for the case when the holding capacitors are voltage driven at both ends and suggested possible design solutions.

The nonlinearity due to charge injection would be eliminated if an ideal infinite speed clock is used. For real SC circuits it is possible only to reduce this nonlinearity by using the maximum clock slope allowed by technology. Beyond this the switches timing and siz-

ing are important in linearizing the charge injection error. Using the dummy switch topology and adjusting the time delay between switching phases seems to be the best solution. However this requires a precisely designed clock generator. Overall the expected nonlinearity from charge injection effect in the circuit is less than 1mV level.

The two-phase and four-phase non-overlapping clock generator is described in the last part of the chapter. The way the clock generator was designed ensured that the clock phases track each other realizing the right timing for the switches. Therefore the jitter is not of concern for our circuit.

Chapter 6 Summary and Conclusions

The recent advances in VLSI technologies have made the ΣΔ analog-to-digital conversion technique very successful. The penalty paid for the high resolution achievable with ΣΔ converters has always been speed: the hardware has to operate at the oversampling rate that is limited by process technology. This thesis pushes the limits of a given process through an innovative architecture and advanced circuit techniques.

6.1 Summary

Chapter 1 introduced the two main high-order ΣΔ topologies capable of producing high SNR for modest OSR values: single-loop and cascade structures. The double sampling technique was presented as a way to double the speed of SC circuits without requiring faster op-amps.

Chapter 2 was a detailed review of previous single-loop modulator architectures. The Z-domain *NTF* and *STF* for bandpass ΣΔ modulators with a bandwidth centered around π/2

were given. It was shown that adding a small-negative local resonator feedback coefficient splits the *NTF* zeros around the band of interest which cause an improvement in SNR of several dBs. If a particular *STF*, that is independent of the *NTF*, is required then the cascade of resonators structure with distributed feedforward and feedback coefficients should be used.

Resonators can be easily built using two delay cells in a negative feedback loop. The half and full delay switched-capacitor cells were analysed taking into account the non-ideal effects of finite op-amp DC gain and non-zero op-amp's input capacitance. Depending on the circuit topology these effects produce a gain error either in magnitude or phase, or both.

Chapter 3 represented the system level design and simulations for a sixth-order BPΣΔ modulator. Similar SNR values are produced by a sixth-order three-level quantizer and by an eighth-order two-level quantizer modulator. The less complex sixth-order version was thus chosen. The *NTF* and *STF* were designed and a novel architecture was proposed. The novelties here consisted in combining the tri-level quantizer and splitting the *NTF* zeros along the tangent to the unit circle technique. All these improved stability and increased SNR several dBs without adding significant complexity to the circuit. The stability of the modulator was analysed by the root locus method. Simulations showed that 1% coefficient mismatches and up to 25% for the local resonator coefficient do not adversely impact the system performance.

Chapter 4 deals with the circuit implementation of the modulator. A new four-path fully differential resonator is presented and analysed. The finite DC gain and non-zero input capacitance of the op-amp introduce a gain and phase error in the resonator's transfer function. Nevertheless they keep the passband centered around $f_s/4$. Simulations showed that an op-amp with 50 dB gain and an input capacitance equal to the holding capacitor don't degrade the SNR significantly. The resonator is designed to be capacitor-mismatch and paths-mismatch insensitive. The use of the four-path technique doubled the speed of the modulator. The folded-cascode op-amp, op-amp biasing, CMFB, the tri-level quantizer and the comparator circuits were further presented.

The most sensitive function/failure source of the modulator designed is considered to be the charge injection. Chapter 5 addressed the critical task of choosing the switch topology that minimizes the error caused by charge injection for the case of a switched capacitor voltage driven at both ends (this is the resonator's case). The X-gate offers a good linearity for a narrow voltage range. The dummy switch can offer the best linearity if a high clock slope and the right timing are used, but this demands an accurate clock generator. A four-phase non-overlapping clock generator was presented. The circuit is "relatively stable" ("robust") because it was designed such that the clock phases track each other and produces the right timing for switches.

A layout including the ΣΔ modulator and two test circuits, a sample-and-hold and a biquad, was designed and submitted for fabrication. Because of a gdsII conversion problem the pads were disconnected and no measurements were possible. Appendix A presents

the main causes of layout errors and the design techniques that were utilized to minimize them. One of these techniques to minimize the element mismatches was to use a locally symmetric floorplan for the fully differential SC resonators.

6.2 Final Conclusions

This thesis provided a possible solution for a ΣΔ A/D converter for applications like GSM or FM radio that require a bandwidth of up to 200 kHz. The modulator's oversampling ratio is 50 and the simulated SNR is approximately 95 dB for an input signal of -20 dB relative to the full scale. The clock frequency (e.g. ϕ_1) is 10MHz and the sampling frequency is 20MHz. The new ΣΔ modulator architecture proposed in this thesis allowed us to achieve this performance in a low-cost 1.5μm CMOS process. The performance can be further improved using a more advanced CMOS technology.

It was proven by means of analysis and simulations that one can design switches for SC circuits with capacitors that are voltage driven at both ends to minimize the errors due to charge injection. The first thing to take into account is to use the maximum clock slope allowed by a given CMOS process. If high signal swing is not required, then the X-gate, which introduces a linear charge injection error only for a narrow signal range, can be used. If high swing is required the dummy switch technique is the optimal solution. The charge injection error in this case is linearized if the time delay between the early clock phase that turns off the NMOS device and the phase that turns on the dummy switch is comparable to the fall-time of the clock and if it is allowed enough time for the dummy

switch to complete its channel charge transfer into the holding capacitor (10 times the clock fall-time might be enough).

Charge injection difficulties limit linearity for our new topology, which is otherwise very efficient. Its real niche may be in low-power circuits where low switching speeds allow the use of very small switches, rather than in the high-speed application we have been studying.

Appendix A Layout Considerations

The final step of an integrated circuit design flow is the layout. Despite substantial progress on modern CAD tools the analog and mixed-signal circuit layouts are mainly designed by hand. This is because today's CAD tools don't offer general and complete design strategies for this type of circuits. Speed and accuracy are the main requirements for analog circuits and they should be carefully considered in the layout design.

A.1 Mixed-Signal Paths

SC circuits require careful layout design due to the digital noise that can easily perturb the sensitive analog paths. The substrate noise can be limited using shielding techniques. The methods of shielding are:

1. guard rings which offer a low impedance path for substrate noise currents,
2. metal Faraday shielding which creates a surface barrier along the noisy paths,
3. separation from noise sources (RC attenuation in substrate).

Sensitive analog lines or devices (like inputs to op-amps, feedback DAC lines, or capacitors) can be shielded by plates (wells or metal layers) or rings carefully biased and connected to a quiet low-impedance node. In this way the substrate noise currents are drained towards these non-critical nodes.

Noise can also be injected into the analog paths from direct capacitive coupling with digital lines. This happens when analog and digital lines are routed in parallel for a long distance or when an analog line crosses a digital bus.

When parallel routing of the analog and digital lines cannot be avoided, decoupling can be done by increasing the distance in between, or even putting a shield connected to ground between the critical paths. Running a sensitive line, e.g. the one connected to the virtual ground of an op-amp connected as an integrator, across a digital bus should be avoided since the noise is directly integrated onto the feedback capacitor. Noise entering the first stage of a $\Sigma\Delta$ modulator is indistinguishable from the analog input signal and propagates to the modulator's output.

It is impossible to shield a circuit completely from the substrate noise. Using differential balancing, the noise is common-mode rejected. It is very important in this case that both sides of the differential circuit are equally disturbed by the substrate noise. This implies "mirror-like" geometric matching of the two areas.

These techniques were used in the $\Sigma\Delta$ modulator layout design of this thesis.

A.2 Power supplies

Because of the finite conductance of the metal power lines (V_{DD} and V_{SS}) and the inductance (3 to 10 nH typical value) of the bond-wire between the pins and the pads, current glitches from the digital circuits are injected into the analog circuits through their power buses. To prevent such coupling, separate power supply connections (separate pins and separate pads) should be used for analog and digital circuits. When not enough pins and pads are available, the digital and the analog nets should merge just before the common pad [Johns97].

The modulator in this thesis uses separate pins and pads for V_{SS}, but only one pin and pad for V_{DD} with digital and analog V_{DD} paths merged at the pad. In order to minimize parasitic inductance, the power supply connections were set in the middle of the frame.

A.3 Element matching

In order to ensure common-mode rejection of noise, differential analog circuits have to be laid out as symmetrically as possible. Different symmetry techniques are used for transistors, resistors and capacitors.

The analog **transistors**, which are typically much larger than the digital ones, are laid out as interleaved multiple-gate fingers. This technique saves area and reduces parasitic capacitance of drain and source. The common-centroid layout [Franca94] was used to match

transistors of a differential circuit, where the fingers of one transistor are interleaved with the fingers of a second transistor. Dummy transistors may be used as the two outside fingers to further improve the accuracy of the matching by reducing edge effects. The gates of the dummies are connected to V_{DD} or V_{SS} such that they are off all the time.

Large **resistors** were laid out with a serpentine arrangement surrounded by a dummy resistor to reduce the mismatch caused by the boundary-dependent undercut effect. An interleaved finger layout can be used when very accurate resistance ratios are required. These fingers are connected by high-conductance metal lines and dummy fingers are used. A shield (well) connected to a clean ground or power supply node was used under the resistors to keep the substrate noise from being injected into the resistor.

In SC circuits **capacitor** ratios should have a high accuracy. Capacitor mismatch is due to two main factors: one is the gradient of the oxide thickness across the chip surface and the other is the boundary-dependent overetching (undercut) effect which reduces the actual capacitor area.

The approach in designing matched capacitors is to use unit capacitors (cells). The mismatch errors due to the gradient of the oxide thickness can be reduced if the unit cells, that form the two big capacitors that have to match, are laid out interleaved in a common centroid fashion. The overetching effect doesn't affect the matching if the capacitors contain an integer number of unit cells. This effect appears only when a capacitor with non-integer

number of unit cells is required (e.g. for $C_1/C_2 = 3.3/4$). In order to maintain the capacitor ratio we need to keep their perimeter/area ratio constant as well [Johns97].

Plates with rounded (or 45°) corners should be used to minimize the boundary-dependent effects. The parasitics related to interconnections of the capacitor plates have a contribution to the mismatch error too. A carefully designed layout should minimize and match these parasitics.

The resonators architecture is capacitor mismatch insensitive, so matching these capacitors was not critical. Wells underneath them were used to minimize the substrate noise.

A.4 Floorplanning

Perfect symmetry is difficult to achieve when building a fully differential complex circuit. Moreover if elements that have to match are quite far from each other, even a perfectly symmetric layout will have poor matching. Thus only a local symmetry that keeps the matching elements close is satisfactory. This is the case shown in Figure A.1 for a differential SC circuit that is symmetrically laid out with the op-amps in the middle followed by capacitors and then the switches at the sides. Such an arrangement creates considerable mismatch paths for the analog signals and as a result tones will be generated at the output. The layout of this thesis used a better solution that is to line up the op-amps on one side of the layout followed alongside by all the capacitors and then by the switches as shown in Figure A.2.

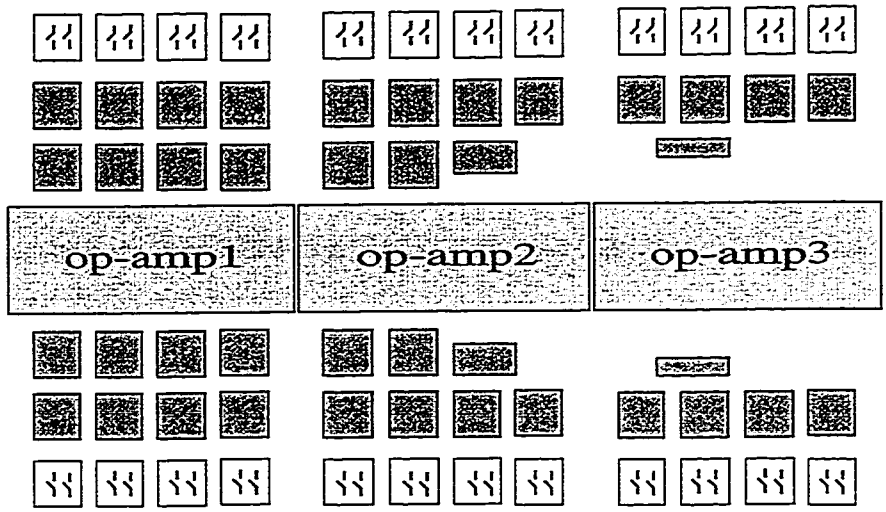


Figure A.1 Symmetric floorplan for a fully differential SC circuit.

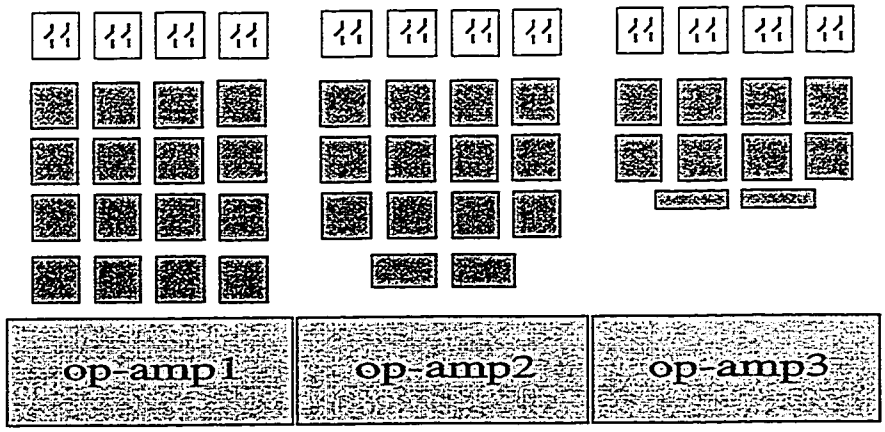


Figure A.2 Local symmetry floorplan for a fully differential SC circuit.

As general rules for the floorplanning the analog sensitive blocks should be as far as possible from the digital circuits and well shielded. Connections to the sensitive nodes should

be made as short as possible and also shielded. The lines to the analog circuits should avoid crossing the digital busses.

A.5 Conclusions

Unlike for digital circuits, the layout for analog and mixed-signal circuits cannot be automatically designed by present CAD tools. Numerous critical effects, like coupled noise or parasitic capacitances, are poorly predicted by simulator tools. Layout techniques which minimize noise were presented.

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