

# **A Single-IF Receiver Architecture Using a Complex Sigma-Delta Modulator**

by

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A thesis submitted to the Faculty of Graduate Studies and Research  
in partial fulfillment of the requirements for the the degree of Masters  
of Engineering

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## *Abstract*

In the growing market for portable communications, it is becoming more important to design high performance transceivers which consume little power. Currently, many architectures are exploited to give the maximum dynamic range while running off a 1 V battery. This makes it challenging to design components such as A/D converters which may be required to have 12-bit resolution.

This thesis proposes a new A/D converter called a Complex Bandpass  $\Sigma\Delta$  Modulator suitable for a Single-IF receiver architecture. This modulator is based on existing bandpass  $\Sigma\Delta$  Modulator structures, and was designed to give roughly double the bandwidth performance of existing Bandpass  $\Sigma\Delta$  Modulators. Two versions of this modulator were designed and fabricated as switched C circuits in a 0.8 $\mu$ m BiCMOS technology, and the results are presented. The maximum SNDR of these modulators was 48dB with a bandwidth of 10kHz and a sampling rate of 4MHz with a power dissipation of 160mW. The maximum operating frequency was found to be approximately 45MHz.

This modulator was also tested with a suitable analog front-end operating at an RF of 1.9GHz and an IF of 60MHz. Results are presented for demodulated GMSK data (similar to GSM) for this receiver. This is meant to show the feasibility of using this type of  $\Sigma\Delta$  Modulator in a radio receiver.

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## *Acknowledgements*

I would like to thank my supervisor Martin Snelgrove for his constant support and guidance throughout my MEng. His intuitive way of viewing things helped me grasp things about analog design that were more than a mystery before. And his connections helped to get my chips fabricated in time (to go to Italy). Thanks Marty.

A big thanks goes to Theo Varelas, Luc Lussier, Christian Cojocar and the rest of the Philsar crowd. Without access to their platform chip, design tools and experience, this whole thesis wouldn't have been possible. Thanks guys.

Jose Macedo deserves the credit for at least half this research, since he provided a fully functional RF front-end for my chip. Thanks for putting in the time to lay out a front-end suitable for my A/D. I owe you one.

Of course, there's a zillion people that are responsible for keeping me sane throughout the past 2 years. Just to name a few : Phil Lauzon, Alana Wirta, Leonard Dauphinee, Walt Bax, and the rest of the radio group at Carleton. Thanks for the information, help and beer that you provided.

For financial support, thanks goes to NSERC and Micronet, without which I wouldn't have nearly as large a CD collection as I have today.

And finally, thanks to my sister and parents for their constant encouragement, questions and occasional pressure to get my thesis done. Hope you still got enough left for my PhD!

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## *Glossary of Terms*

$\Sigma\Delta$	.....	Sigma-Delta Modulator
AGC	.....	Automatic Gain Control
AWGN	.....	Additive White Gaussian Noise
BER	.....	Bit Error Rate
BiCMOS	.....	Bipolar Complementary Metal Oxide over Semiconductor
BP $\Sigma\Delta$	.....	Bandpass Sigma-Delta Modulator
CBP $\Sigma\Delta$	.....	Complex Bandpass Sigma-Delta Modulator
CLB	.....	Carry Look-ahead Buffer
CMFB	.....	Common-Mode Feedback
IF	.....	Intermediate Frequency
INTF	.....	Image Noise Transfer Function
IP3	.....	Third-Order Intercept Point
ISTF	.....	Image Signal Transfer Function
LMS	.....	Least-Mean Squares
LNA	.....	Low Noise Amplifier
LO	.....	Local Oscillator
MSA	.....	Maximum Stable Amplitude
NF	.....	Noise Figure
NTF	.....	Noise Transfer Function
OSR	.....	Over-Sampling Ratio
PCN	.....	Personal Communication Network
PCS	.....	Personal Communications System
RF	.....	Radio Frequency
SC	.....	Switched-Capacitor
SNR	.....	Signal to Noise Ratio
STF	.....	Signal Transfer Function
TF	.....	Transfer Function
UGBW	.....	Unity-Gain Bandwidth

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## CHAPTER 1

# *Introduction*

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*“Everything that can be invented has been invented.”*

- Charles H. Duell, Commissioner, U.S. Office of Patents, 1899.

This thesis is about the design and implementation of a new type of Sigma-Delta Modulator ( $\Sigma\Delta$ M) called a Complex Bandpass  $\Sigma\Delta$ M. To a lesser extent, it is also about the practicalities of incorporating this into a radio receiver. This circuit, which has been implemented for the first time, is demonstrated in a suitable receiver architecture as a proof-of-concept study.

### *1.1 Motivation*

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For designers working on radio receivers, there has always been a push to design for higher performance at lower power. These two constraints are often contradictory however, so receivers trade off between them in order to meet a certain specification.

Traditionally, analog signal processing was used throughout the receiver. But today, more and more people are advocating the use of an Analog-to-Digital (A/D) converter in the receiver. All this does is change the representation of the signal, not the content, but it is

easier to perform precise filtering with Digital Signal Processing (DSP). Also, DSP can be made programmable, giving one more degree of flexibility on the receiver (e.g. to handle multiple standards).

Existing art offers many ways to build this A/D converter. One way is by using a Bandpass Sigma-Delta Modulator (BP $\Sigma\Delta$ M). This was first implemented in [Jan92] and has been developed by others for better performance [Lon93]. The reason this is considered to be an improvement for radio receivers is that this performs A/D conversion on the signal at an Intermediate Frequency (IF) and thus moves the A/D converter one step closer to the antenna.

By doing this, we eliminate the need for some analog signal processing circuits which can have limited performance due to component mismatch. DSP is not limited by that, since digital hardware can achieve perfect matching between components. Now a key question is: How can we design the A/D converter to give us maximum performance, where performance is defined both in terms of resolution and bandwidth (BW).

Recently, a new type of BP $\Sigma\Delta$ M has been proposed called a Complex  $\Sigma\Delta$ M [Jan94a][Azi95]. This is especially suited to an image-reject (IR) receiver because it operates on two orthogonal signals, which are found in IR receivers (see Figure 1).

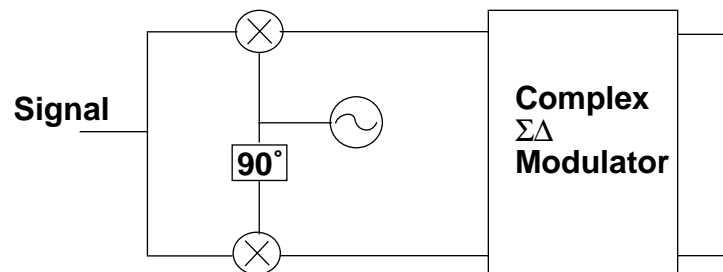


FIGURE 1. A Complex SDM system

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This type of  $\Sigma\Delta$  is expected to give a factor of 2 improvement on bandwidth relative to a traditional BP $\Sigma\Delta$  [Azi95]. To demonstrate the feasibility of this type of  $\Sigma\Delta$ , a platform chip was modified [Phi96]. This allowed for quick design and fabrication of the prototype. The trade off was that the circuit wasn't optimized for this type of modulator architecture. The results outlined within are for the first silicon, to demonstrate the proof-of-concept of this modulator. [Jan97] outlines some results for a fully custom Complex  $\Sigma\Delta$ .

This  $\Sigma\Delta$  is ideal for any type of receiver (from AM to GMSK) but to demonstrate its feasibility, we have chosen to test it for a PCS application.

## 1.2 *Thesis Outline*

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This thesis is roughly split 70/30 between the design and implementation of a Complex  $\Sigma\Delta$  and the implementation and testing of a Single-IF receiver using a Complex  $\Sigma\Delta$ . Chapter 2 deals with the specifics of receiver architectures and where the  $\Sigma\Delta$  fits in. It also discusses some PCS standards and targets GSM as the test standard we will use.

Chapter 3 talks about the theory behind a Complex  $\Sigma\Delta$  Modulator. It also discusses some of the prior art on Bandpass and Complex  $\Sigma\Delta$  structures.

Chapter 4 is the design and architecture of the two Complex  $\Sigma\Delta$  prototypes that we designed. It also discusses some of the innovations behind both these modulators.

Chapter 5 details the testing of both Complex  $\Sigma\Delta$  Modulators. It also draws conclusions about the SNR performance degradation that was found.

Chapter 6 presents results for the Complex  $\Sigma\Delta$  integrated into a Single-IF radio receiver. This is done using an RF of 1.9GHz with GMSK modulation as the test benchmark.

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Chapter 7 draws conclusions about the Complex  $\Sigma\Delta\text{M}$  and its feasibility in a radio receiver. It also discusses future enhancements that can be made to improve speed and performance of the modulator.

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*“This ‘telephone’ has too many shortcomings to be seriously considered as a means of communication. This device is inherently of no value to us.”*

- Western Union internal memo, 1876

To better understand what specifications we should be designing an A/D converter for, it is important to understand where the A/D fits into a radio receiver. This section outlines the basic principles that radio receivers use, as well as a few examples from existing art on receivers. It also discusses the ‘fit’ of the A/D converter into these existing receivers, as well as what type of A/D converter would be required for specific receivers. Finally, this section also provides some background into some PCS standards. In the following chapters, we will show that a Complex  $\Sigma\Delta\text{M}$  is a feasible choice for an A/D converter for a receiver by using a PCS standard as a benchmark.

## ***2.1 Receivers - The Superheterodyne Technique***

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Most current architectures are ‘variations on a theme’; the theme being the superheterodyne radio receiver proposed by Armstrong in the early part of the century [Arm19]. This allowed receivers to be built that used fixed Intermediate Frequency (IF) filters instead of tunable-band ones. The advantage of this was that the fixed filters were

much simpler and had better response than their tunable equivalents. These radio receivers could have any number of IF stages where each IF stage tends to have the same form. This is shown below in Figure 2.

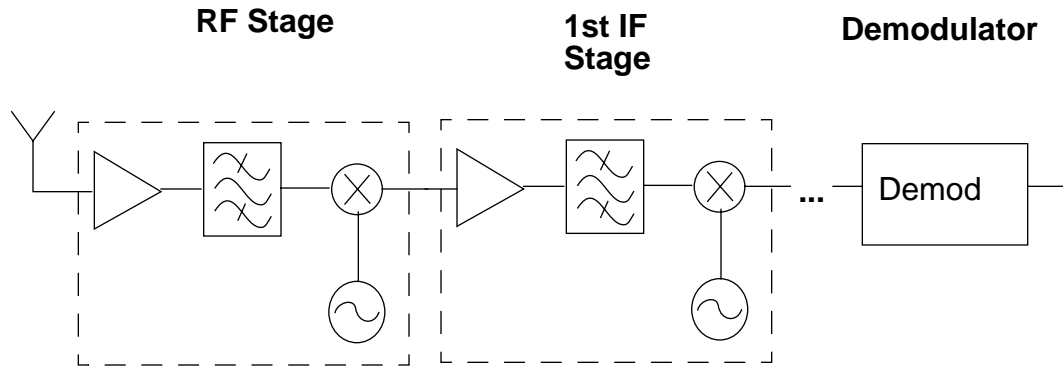


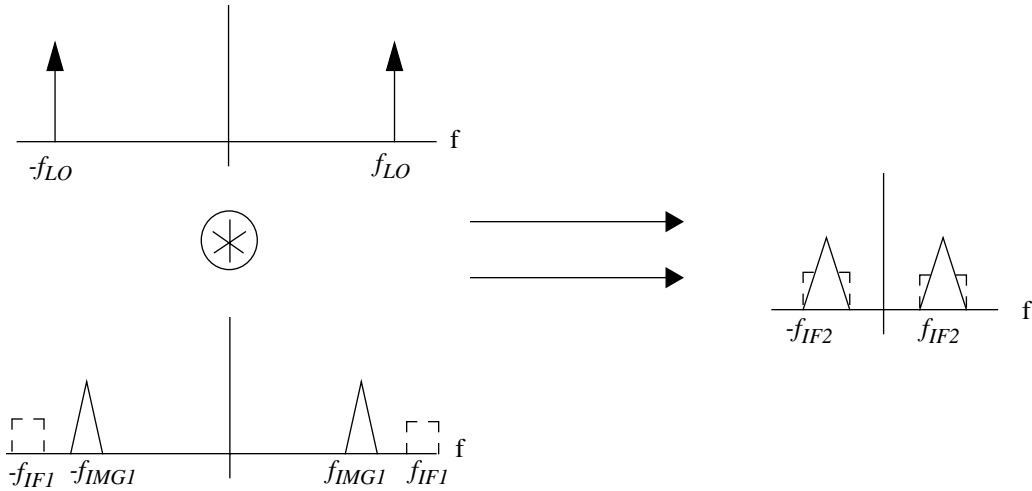
FIGURE 2. Superheterodyne Receiver

This entire receiver could be realized with analog components, but then any sort of mismatch between the circuits in each stage would degrade the performance of the receiver. To prevent this, we could digitize the signal with an A/D converter, because DSP has perfect matching between components. This A/D converter can be placed at any stage in the receiver of Figure 2, from the demodulator to the antenna. The trade-off is that the closer we move the A/D to the antenna, the faster it has to work and the more dynamic range it needs (translation: more expensive A/D) but the less analog components we need for the receiver.

This architecture is used in a lot of radio receivers. Unfortunately, it suffers from a problem with image rejection, which is discussed in the next section.

## 2.2 Image Rejection in Receivers

One major problem with any IF receiver is image rejection. During the mixing stage, some frequency,  $f_{IF1}$ , is mixed with an oscillator signal,  $f_{LO}$ , to produce a signal at  $f_{IF2} = f_{IF1} - f_{LO}$ . However, because mixing convolves both the positive and negative frequency components of a signal to  $f_{IF2}$ , the negative frequency component of the signal at a frequency  $f_{IMG1} (= f_{LO} - f_{IF2})$  also gets mapped to the same IF. This can be seen in , where by convolving the signals at  $f_{IMG1}$  and  $f_{IF1}$  by an oscillator signal  $f_{LO}$ , we end up adding the two signal together.



**FIGURE 3. Mixing Images on top of Signals**

One way to combat this is to filter the image out before the mixing stage [Mac96], but it may be necessary to have 80dB or more attenuation at  $f_{IMG1}$  which is only  $2*f_{IF2}$  away from the desired signal. If  $f_{IF2}$  is small enough, the Image Reject (IR) filter becomes extremely expensive (as it tends to a “brick wall” response). Typically these filter

constraints make  $f_{IF2} \approx f_{IF1}/10 \approx f_{RF}/100$ ; even then it is not possible to filter off the image completely.

Another way to combat this image problem is by using a one-sided oscillator signal to mix the desired signal to the desired IF. This is known in the literature as an Inphase/Quadrature (I/Q) mix or Image Reject mixing. By one-sided oscillator signal, we mean a complex-valued signal  $e^{j\omega t} = \cos \omega t + j \sin \omega t$  that has a one-sided spectrum. But with superheterodyne receivers, image rejection is needed at every stage to insure that no undesirable signals may degrade the quality of reception. This type of receiver has problems with matching between the I and Q channels, as is explained in later sections.

For example, to accomplish true image rejection in both mixers of a dual IF receiver, we would have to get the mixers to do complex mixing (because the second mixer now has both a complex input, and a complex oscillator signal) [Cro95]. This can be seen in Figure 3 where the second IF stage has a complicated arrangement for the mixer. Obviously the shortcoming of this method is that the second stage has four mixers as compared to the two in the first stage. And since the complexity has increased, matching between all the channels becomes even more important since matching errors can accumulate.

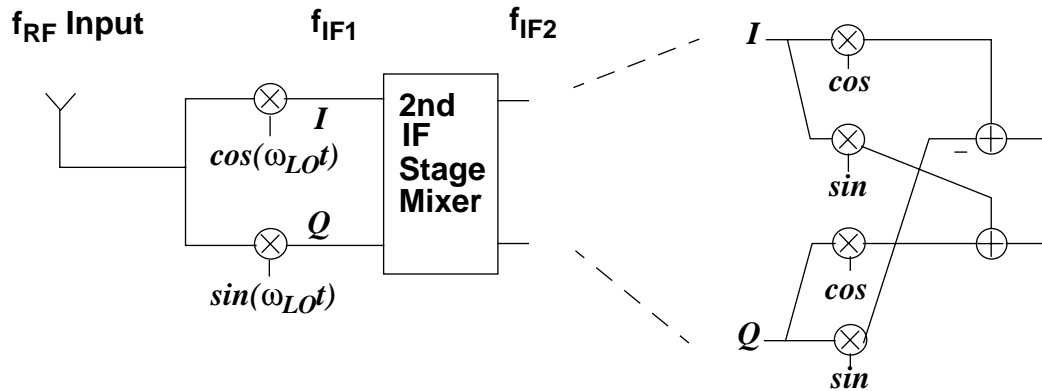


FIGURE 4. Example of IR Technique in Dual IF Receiver

Yet another way to perform image rejection is to recombine the signal after each mixing stage [Bau94] as shown in Figure 4. This appears simpler, because we now need only two mixers, one adder, and one  $90^\circ$  phase-shifter, instead of the previous four mixers and two adders. The only problem with this is that the  $90^\circ$  phase-shifter is not trivial to realize, and in fact, can have a phase error of as much as  $\pm 3^\circ$  [Alt86]. This is highly layout and process dependent though, and with careful design, can be much less.

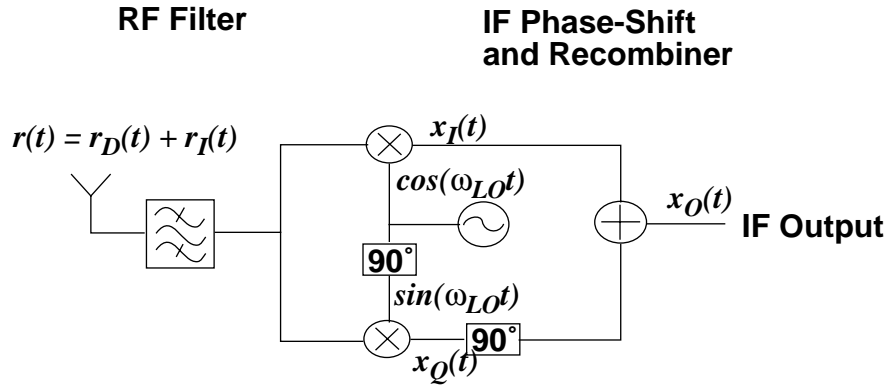


FIGURE 5. Another IR Technique for Multiple IF Receivers

Mathematically, real analysis of this kind of system starts with (EQ.1) and (EQ.2) where  $r_D(t)$  is our desired signal,  $r_I(t)$  is the image signal, and  $r(t)$  is the combination of these two:

$$\begin{aligned}
 x_I(t) &= r(t) \cos \omega_{LO} t \\
 &= r_D(t) \cos \omega_{LO} t + r_I(t) \cos \omega_{LO} t
 \end{aligned}
 \tag{EQ 1}$$

$$\begin{aligned}
 x_Q(t) &= r(t) \sin \omega_{LO} t \\
 &= r_D(t) \sin \omega_{LO} t + r_I(t) \sin \omega_{LO} t
 \end{aligned}
 \tag{EQ 2}$$

This is a mathematically cumbersome way of analyzing an I/Q system. It is far easier to use complex exponentials to represent the signals rather than the preceding functions. We know from elementary complex mathematics that:

$$e^{j\theta} = \cos \theta + j \sin \theta \quad (\text{EQ 3})$$

Now if we treat  $x_I(t)$  and  $x_Q(t)$  as the real and imaginary parts of a function  $x(t)$ , we can rewrite (EQ.1) and (EQ.2) as:

$$\begin{aligned} x(t) &= x_I(t) + jx_Q(t) \\ &= r_D(t)e^{j\omega_{LO}t} + r_I(t)e^{j\omega_{LO}t} \end{aligned} \quad (\text{EQ 4})$$

For the moment, let us assume that we are amplitude modulating carriers at  $f_{RF}$  and the image  $f_{RF} - 2f_{IF}$  (it turns out that the derivation for frequency modulation is similar [Vie95]). This gives the following for  $r_D(t)$  and  $r_I(t)$ :

$$\begin{aligned} r_D(t) &= a(t) \cos \omega_{RF} t \\ r_I(t) &= b(t) \cos (\omega_{RF} - 2\omega_{IF}) t \end{aligned} \quad (\text{EQ 5})$$

Or, in complex notation,

$$r_D(t) = \frac{a(t)}{2} [e^{j\omega_{RF}t} + e^{-j\omega_{RF}t}] \quad (\text{EQ 6})$$

$$r_I(t) = \frac{b(t)}{2} [e^{j(\omega_{RF} - 2\omega_{IF})t} + e^{-j(\omega_{RF} - 2\omega_{IF})t}] \quad (\text{EQ 7})$$

Where  $f_{IF} = f_{RF} - f_{LO}$ . After substituting this into (EQ.1) and (EQ.2) and removing the high frequency terms, we get:

$$x_I(t) = \frac{1}{2}a(t)\cos\omega_{IF}t + \frac{1}{2}b(t)\cos(-\omega_{IF}t) \quad (\text{EQ 8})$$

$$x_Q(t) = \left(-\frac{1}{2}\right)a(t)\sin\omega_{IF}t - \frac{1}{2}b(t)\sin(-\omega_{IF}t) \quad (\text{EQ 9})$$

or,

$$x(t) = \frac{a(t)}{2}e^{-j\omega_{IF}t} + \frac{b(t)}{2}e^{j\omega_{IF}t} \quad (\text{EQ 10})$$

Then, if we delay (phase shift)  $x_Q(t)$  by  $90^\circ$ , we get the following for  $x_O(t)$ :

$$\begin{aligned} x_O(t) &= \frac{1}{2}a(t)\cos\omega_{IF}t + \frac{1}{2}b(t)\cos(-\omega_{IF}t) \\ &\quad + \frac{1}{2}a(t)\cos\omega_{IF}t - \frac{1}{2}b(t)\cos(-\omega_{IF}t) \end{aligned}$$

$$x_O(t) = a(t)\cos\omega_{IF}t \quad (\text{EQ 11})$$

In the complex world, this is equivalent to having positive-pass filter and only looking at the real part of the output. We mentioned before that there could be a possible  $\pm 3^\circ$  phase error from a '90°' phase-shifter. This causes some of the image signal to be present in the IF output. Assuming that the phase error ( $\Delta\theta$ ) is completely in the quadrature (sin) channel of the Local Oscillator (LO), we can rewrite  $x_Q(t)$  as:

$$\begin{aligned} x_Q(t) &= r(t)\sin(\omega_{LO}t + \Delta\theta) \\ &= r_D(t)\sin(\omega_{LO}t + \Delta\theta) + r_I(t)\sin(\omega_{LO}t + \Delta\theta) \end{aligned} \quad (\text{EQ 12})$$

And after substituting the previously defined formulae for  $r_D(t)$  and  $r_I(t)$  in (EQ.5) we get:

$$\begin{aligned}
x_Q(t) &= -\frac{1}{2}a(t)\sin(\omega_{IF}t - \Delta\theta) - \frac{1}{2}b(t)\sin(-\omega_{IF}t - \Delta\theta) \\
&= -\frac{1}{2}a(t)[\sin\omega_{IF}t\cos\Delta\theta - \cos\omega_{IF}t\sin\Delta\theta] - \\
&\quad \frac{1}{2}b(t)[\sin(-\omega_{IF}t)\cos\Delta\theta - \cos(-\omega_{IF}t)\sin\Delta\theta]
\end{aligned} \tag{EQ 13}$$

Assuming that  $\Delta\theta$  is small so that  $\cos\Delta\theta = 1$  and  $\sin\Delta\theta = \Delta\theta$  yields:

$$\begin{aligned}
x_Q(t) &= -\frac{1}{2}a(t)[\sin\omega_{IF}t - \Delta\theta\cos\omega_{IF}t] - \\
&\quad \frac{1}{2}b(t)[\sin(-\omega_{IF}t) - \Delta\theta\cos(-\omega_{IF}t)]
\end{aligned} \tag{EQ 14}$$

And after phase shifting this by  $90^\circ$  and adding to  $x_I(t)$ , we find that  $x_O(t)$  is:

$$x_O(t) = a(t)\cos\omega_{IF}t + \frac{1}{2}\Delta\theta a(t)\sin\omega_{IF}t + \frac{1}{2}\Delta\theta b(t)\sin\omega_{IF}t \tag{EQ 15}$$

We can see that not only do we have a phase-shifted copy of the signal in our output, but the image signal also gets aliased in (albeit attenuated by  $\sin\Delta\theta$ )! Typical values of phase error ( $\pm 3^\circ$ ) would produce approximately -25dB of image alias into the signal. This specification is often called the Image Rejection (IR) of a quadrature system.

IR receivers tend to be rare in practical applications because of this mismatch problem. But the superheterodyne receiver remains one of the most popular types of radio receivers today. It is widely used in the growing market for high-frequency telecommunications and satellite communication [Mar95][McD92].



### 2.3 Existing Art - Dual IF Receiver

The dual IF receiver has been the traditional choice for most applications. [Rap94] discusses some of the characteristics of the components of a typical dual IF receiver built mostly out of discrete components.

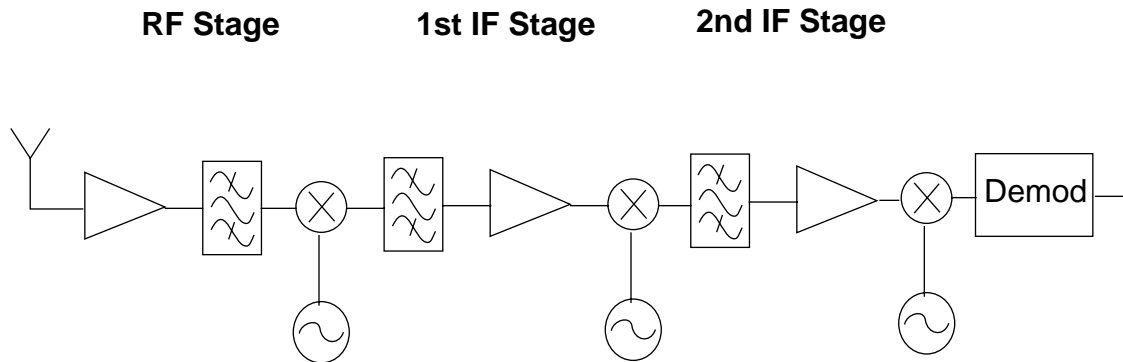


FIGURE 6. Dual IF Receiver

This view of receivers assumes that most of the high frequency components would be discrete, due to coupling and harmonic distortion that would be present in an integrated solution. The drawback of this is that matching is even worse with discrete components than with an integrated circuit. Currently however, RF and high frequency IF circuits are being integrated with good performance [Mac96][Ste95]. This all points towards a more compact view of a receiver, where a two or three chip solution may be all that is required. Also, this receiver has problems with image rejection. The filters in each of the stages have to be able to attenuate image signals that are 65dB more powerful than the desired signal [Zvo96]. The previous image reject schemes that we looked at all increase the complexity of this receiver, and with discrete components, that could mean worse performance due to matching.

Another fact that is addressed is the role of the A/D converter in this receiver. [Rap94] states that if we would like to integrate as much of the receiver as possible, we can use an A/D to convert the band-limited second IF. This may make using a flash A/D converter expensive, since it has to sample at twice the IF with 12 to 13 bit resolution. At any rate, this still doesn't help us with the image rejection problem that this receiver faces.

## 2.4 Existing Art - Direct Conversion

Another architecture that is used is a Homodyne, or Direct Conversion receiver. This is at the other end of the spectrum from dual IF architectures in that there are zero IF stages. And since there are no IF's, the image get mixed to  $2*f_{RF}$ . [Sch90a] outlines an implementation of a receiver suitable for the Digital European Cordless Telephone (DECT) standard. This is shown in Figure 6.

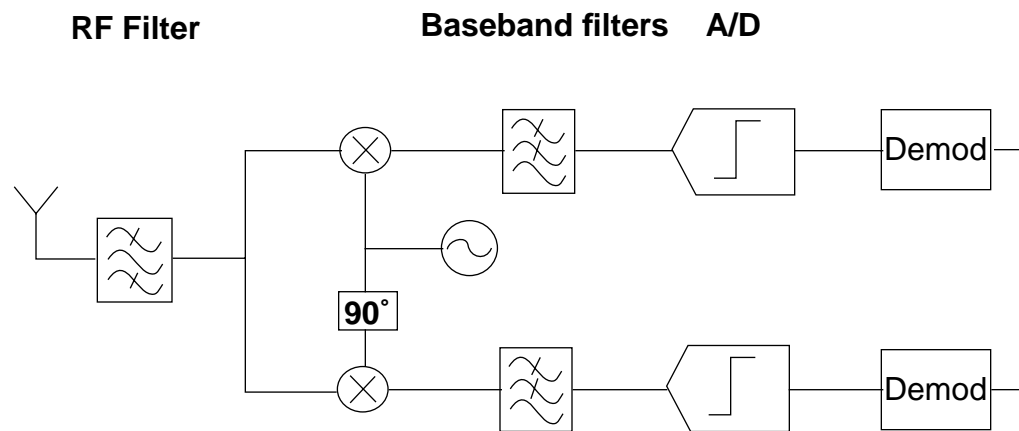


FIGURE 7. Direct Conversion Receiver

This receiver performs the A/D conversion at baseband, and the demodulation after that. It has the advantage that there is a reduced number of analog RF components needed. The disadvantages of this receiver are that it is sensitive to coupling, including oscillator feedthrough to DC offset at the output of the mixer, flicker noise ( $1/f$  noise) and second

harmonic distortion. Direct conversion receivers are still used today due to their simplicity [Sch90a][Has92][McD92].

## 2.5 Existing Art - Single-IF Receivers

Another receiver that is used the Single-IF receiver [Vie95][Swa96a][Ste95]. The idea behind this receiver is that it is a cross between dual IF and direct conversion architectures, and it can avoid the shortcomings of both. It avoids the DC problems of direct conversion by using an IF and the complexity problems of dual or more IF receivers by only needing one IF filter. A single-IF receiver was developed in [Ste95] and is shown in Figure 7.

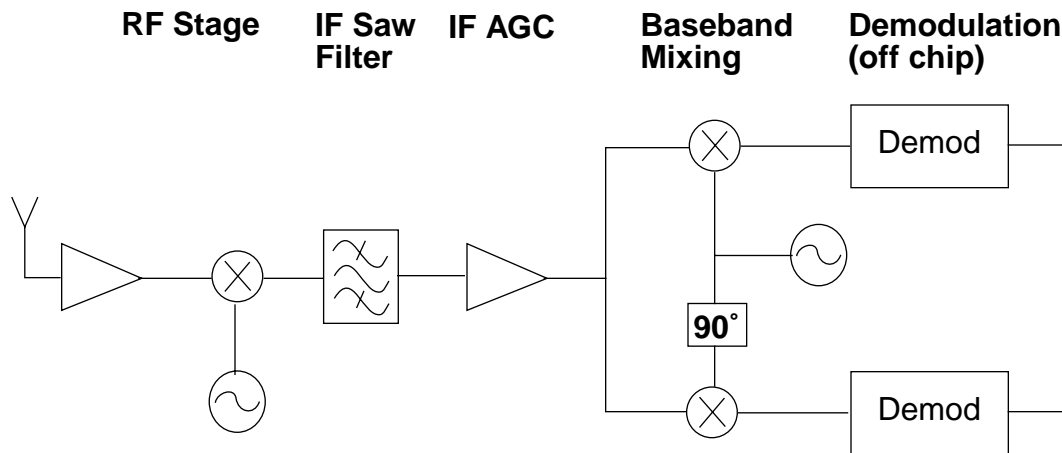


FIGURE 8. Single-IF Receiver

This chip doesn't perform data demodulation itself, but provides the inphase (I) and quadrature (Q) channels so that another chip can do the demodulation. This chip still suffers from the image reject problem, and we need a blocking filter after the antenna to attenuate as much of the image as is required. It also suffers from the problem that there might be mismatch in the analog quadrature mixer that causes some of the image to alias on top of the desired signal. The receiver of [Ste95] claims a phase error of  $1.2^\circ$  which

translates to an IR of 36dB. This still means the front-end RF filter still has to filter out 29dB of the image. On top of that, there are still the same problems at the output as for direct conversion receivers (DC offset, LO feedthrough, etc) since the output stage is still analog. All of this points towards the fact that if we can perform A/D conversion somewhere in this receiver chain, we can help minimize some of these problems.

## 2.6 *Receiver Requirements for A/D Converters*

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As far as the A/D converter for a receiver is concerned, we have many choices. We can use a 2-stage or single-stage Flash A/D converter, but we are limited by the resolution to 10-bits or so.

If our desired signal is narrowband, it makes no sense to perform an A/D conversion of the entire frequency band from DC to the IF. By using an Oversampled A/D Converter [Azi96][Can92][Hau91], one can trade bandwidth for resolution. In fact, from [Azi96] we can see a general relation between resolution and bandwidth of A/D converters (Figure 8). Generally speaking, Oversampled  $\Sigma\Delta$  Modulators (or just  $\Sigma\Delta$  Modulators) rely on what the name implies: oversampling a signal. This accomplishes two things; it reduces the quantization noise that is present and it reduces the effective bandwidth of our signal relative to the sampling rate, so anti-alias filters in front of the A/D converter don't need ideal responses. If we oversample significantly (>8 times the Nyquist rate) we can put this filter and the A/D in a feedback loop and 'shape' the quantization noise out of the bandwidth of interest. The choice of filter for this modulator determines where this noise

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shaping will be. For example, a lowpass filter means that a notch would appear at DC, and a bandpass filter means that the notch would appear at some  $f_{IF}$  frequency.

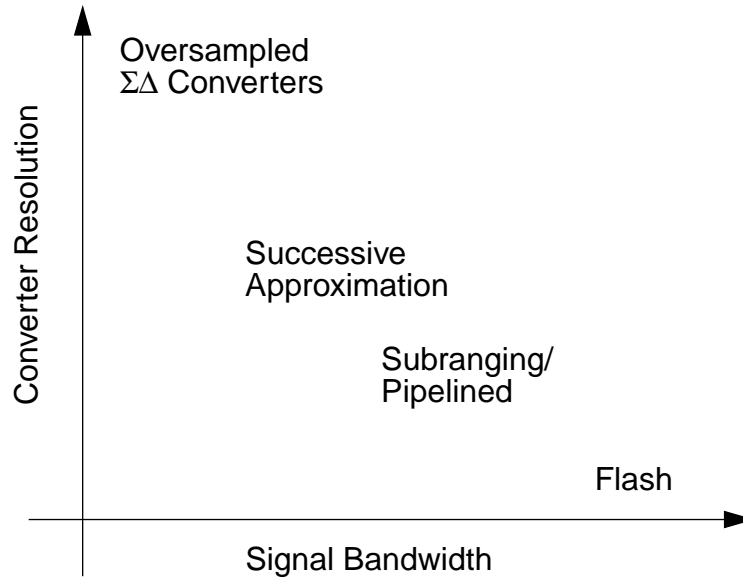


FIGURE 9. Resolution vs. Bandwidth for A/D Converters

By using a bandpass  $\Sigma\Delta$  modulator, we can do narrowband A/D conversion at an IF [Sch89], as opposed to doing it at baseband (like a flash, successive approximation, etc.). If we use a standard bandpass  $\Sigma\Delta$  modulator [Sin94][Lon93][Jan93], we can get reasonable performance, but we end up performing an A/D conversion on both the desired signal (at  $f_{IF}$ ) and the image signal (at  $-f_{IF}$ ) when we don't have to.

An added advantage is that since an A/D converter is a sampled system (the frequency response is periodic with the sampling rate), we can undersample the input signal in order to use a higher  $f_{IF}$  with respect to the sampling rate of the  $\Sigma\Delta$ M.

Recently, a new type of bandpass  $\Sigma\Delta$  modulator has been proposed, called a Complex Bandpass  $\Sigma\Delta$  Modulator [Jan94a][Azi95]. This modulator capitalizes on the fact that we

are dealing with a complex signal (I and Q) as the input, so we can get a better notch for the desired signal at  $f_{IF}$ , and a correspondingly worse notch for the image signal at  $-f_{IF}$ . Figure 9 outlines a possible receiver. The specifics behind the complex  $\Sigma\Delta$  modulator are explored in depth in the next chapter.

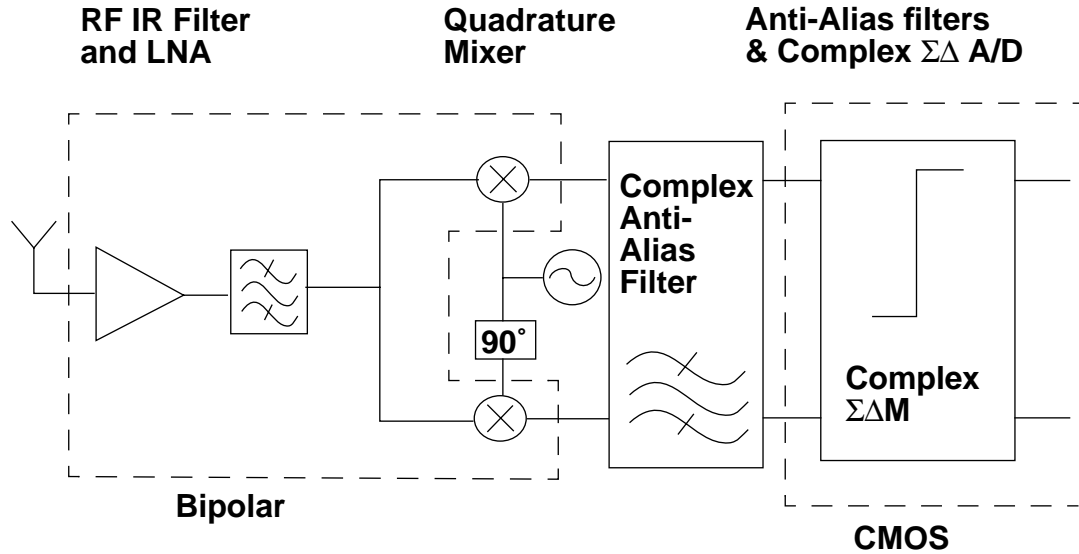


FIGURE 10. Proposed Single-IF Receiver with Complex  $\Sigma\Delta$  Modulator

It is theoretically possible to integrate all these components together on a single chip, but it is not very practical. Switching noise from the A/D converter can very easily be coupled into the sensitive RF front-end components, resulting in a significant increase of Noise Figure (NF) and reduction of Signal to Noise Ratio (SNR). Also, one is limited by the process - the A/D is typically CMOS and the high speed front-end is typically bipolar due to the requirement for high speed/low power circuits operating at 1.9GHz. CMOS front-end circuits have been reported at high frequencies [Kin96][Abo96][Por96], but bipolar processes still offer faster transistors, with higher gains for lower power, and lower NF.

A more realistic partitioning is shown in Figure 9. The 1.9GHz front-end components (Low Noise Amplifier or LNA, Filter & Quadrature Mixer) are shown integrated in a

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Bipolar process. The front-end filter is meant to perform rough band-select (for GSM, the receive bandwidth is 25MHz). The whole front-end has been shown as a fully integrated solution, discussed in [Mac96]. The complex  $\Sigma\Delta$  modulator is shown integrated in a high-speed CMOS process. The complex anti-alias filter provides rough channel select, anti-alias filtering (since the A/D is a sampled-data circuit) and isolation between the ‘noisy’ CMOS switched circuit and the sensitive front-end Bipolar circuits.

## *2.7 Emerging Standards for PCS*

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Personal communication devices (like cellular and cordless phones) are becoming more and more used in today’s society. In fact, there are an estimated 20 million users of cellular and cordless phones in the United States alone [Pad95]. The important distinction between cellular and cordless systems is that cellular systems are meant to service highly mobile clients within a fairly large cell (10 km or less) with a single base station, while cordless systems typically operate with a single base station/client pair with very limited range (100 metres).

In the next generation of cellular phones, more emphasis is placed on increasing the number of cell phone users in the available spectrum. In these networks, multiple clients are handled by one base station (similar to mobile cellular systems) but the transmit power of the handset is greatly reduced from cellular systems (10mW vs. 600mW) and therefore the cell size is greatly reduced (500 metres). The term PCS is often applied to both microcellular networks, and to digital transmission at an RF of 1.9GHz.

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A few of the standards that are being designed for both cellular and cordless are CT2, DECT, DCS-1800 (GSM at a higher RF), IS-95, and PACS. Some specifications on these standards from [Pad95][Cox92] are summarized in Table 1.

**TABLE 1. Specifications of some PCS Standards**

Standard	CT2	DECT	DCS-1800 (GSM)	IS-95	PACS
Freq. Band (MHz)	864-868	1800-1900	1710-1785 1805-1880	869-894 824-849	1850-1910
Multiple Access	TDMA/FDMA	TDMA/FDMA	TDMA/FDMA	CDMA/FDMA	TDMA/FDMA
Channel Spacing (kHz)	100	1728	200	1250	300
Modulation	GFSK (BT = 0.5)	GFSK (BT = 0.5)	GMSK (BT = 0.3)	QPSK	$\pi/4$ QPSK
Bit Rate (kb/s)	72	1152	270.833	1228.8 (chip)	384
Channels/Carrier	1	12	8	40-64	8
Portable Xmit Power (avg., mW)	5	10	125	50	25

As we can see from this, a radio receiver should be versatile enough to handle the wide spread of channel bandwidths, modulations and RF carriers if it is to be used internationally. And it should also use as little power as possible, which may be at odds with the previous requirement. But currently, researchers are looking into designing transceivers to operate at the above frequencies, with a maximum power consumption less than 100mW during transmit and receive [Mar95][Vie95].



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## 2.8 *Receiver Requirements*

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Once a receiver architecture has been settled on, it is important to translate the high-level specifications (like transmit power, channel spacing, etc.) into requirements for each component in the receiver. As we can see from Table 1, three of the five standards that we mentioned have bandwidths in the range of 200kHz. DECT and IS-95 (which uses CDMA) are wider band (more than 1MHz). So, for the rest of this thesis, we will try to prove that a complex  $\Sigma\Delta$  can be integrated in the next generation radio receivers by using a GSM-like standard as the prototype setup (DCS-1800 is like GSM at a higher RF [Cox92]).

[Zvo96] summarizes some of these important parameters for GSM that were derived from the specification. The maximum Noise Figure (NF) that the receiver can have is 8dB. This is so the SNR for the received signal can be greater than 11dB. The receiver typically has a mechanism of automatic gain control (AGC) which amplifies the input so the minimum bit error rate (BER) is met. This AGC range is generally at least 64dB, which covers the range from the minimum reference sensitivity level (-102dBm to -38dBm).

Other specifications can also be stated for the receiver. Compression characteristics of the components in the receiver should be designed so that large interferers (such as +65dB alternate channel interferers) do not affect the reception of the desired signal, particularly for I/Q demodulators.

The GSM specifications also have requirements for the A/D converter as well as for the front-end receiver. The required performance of the converter can be set to 11 bits per channel by the required 64dB spurious free dynamic range. But with an AGC, the performance of the converter can be less. The BW in which we need this resolution is only 200kHz. This makes using a  $\Sigma\Delta$  Modulator ideal, since it can give us high resolution in a

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narrow band. So, our complex  $\Sigma\Delta\text{M}$  design should focus on trying to achieve this resolution in the specified bandwidth.

## 2.9 *Summary*

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Existing receiver architectures were discussed as variations on the Superheterodyne architecture, the two major choices being direct conversion and dual IF. A compromise between these was also discussed: the Single-IF receiver. This receiver is meant to capitalize on the advantages of both direct conversion and dual IF, while avoiding the pitfalls of both. It is also important to recognize the trade-off in placing the A/D converter in the receiver. Placing it nearer to the antenna reduces the number of analog components, but increases the cost of the A/D.

The requirements of a GSM receiver were discussed, specifically NF and dynamic range. From the general GSM specification, the minimum A/D converter resolution and bandwidth was also stated. We shall see in later sections whether it is possible to design the complex  $\Sigma\Delta\text{M}$  to meet these specifications.

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## CHAPTER 3

# *Complex $\Sigma\Delta$ Modulator Theory*

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*“Any sufficiently advanced technology is indistinguishable from magic.”*

*- Arthur C. Clarke*

In the previous section we looked at some existing receivers which suggested that there is a need to develop an A/D converter that would help move some of the signal processing to the digital side. This is partly because matching is perfect in DSP, so circuits with ideal responses can be realized.

This chapter focuses on the theory behind a proposed A/D converter called a complex  $\Sigma\Delta$  modulator. This is based on existing lowpass and bandpass  $\Sigma\Delta$  modulators and is shown to have an improvement on bandwidth over these modulators at a given clock rate.

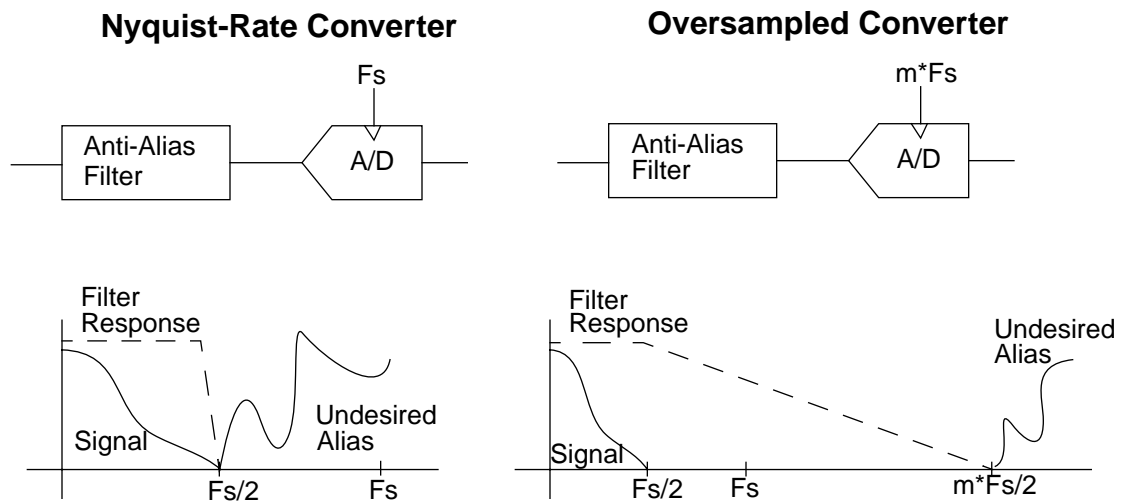
### *3.1 $\Sigma\Delta$ Modulation*

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The operation of Sigma-Delta Modulators ( $\Sigma\Delta$ M) is fairly well understood in the literature [Can92][Can85][Hau91].  $\Sigma\Delta$ M combine two distinct operations: oversampling and noise shaping. It is well known that an A/D converter only has to sample at the Nyquist rate in order to digitize the band of interest (hence the name ‘Nyquist Rate Converters’). This, however, means that the front-end anti-alias filter has to have a brick wall response at half

the sampling rate (see Figure 10). But if we oversample the input signal, our anti-alias filter can be fairly relaxed, as is seen in Figure 10. So, instead of being a high-order Chebyshev or Elliptic filter, this anti-alias filter can be as simple as an RC lowpass (if the oversampling is fairly high compared to the bandwidth of the signal).

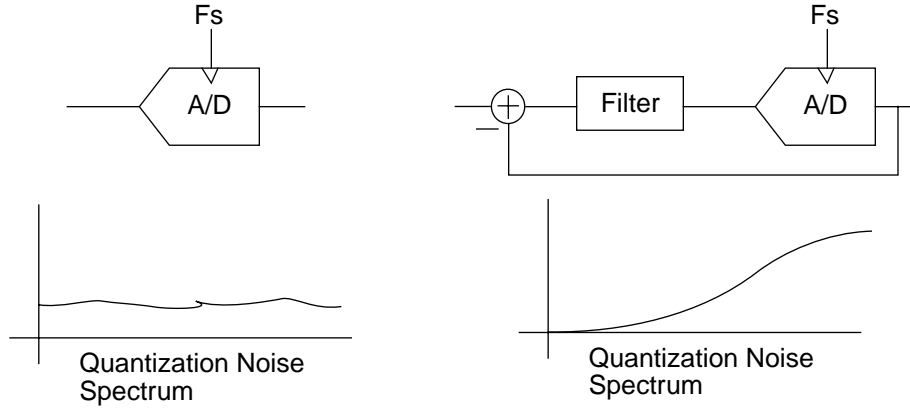
Oversampling also has another effect on A/D quantization noise. For a sufficiently ‘busy’ input signal [Can81], one can assume that the quantization noise of the A/D converter is Additive White Gaussian Noise (AWGN) [Hau91]. The total noise power is dependent on the resolution of the A/D converter, but independent of the bandwidth. So, oversampling an A/D converter will spread this noise over a wider bandwidth, which allows more of it to be filtered off in DSP.



**FIGURE 10. Anti-Alias Filter Requirements for Oversampling**

Noise shaping refers to moving quantization noise from our band of interest to outside this band. Once again, assuming that the noise is AWGN, we can use feedback to remove noise from low frequencies (say 0-4kHz for voice band) at the cost of increasing the noise at

higher frequencies out of our signal band. This is done by imbedding a filter and the A/D converter in a feedback loop as is seen in Figure 11.

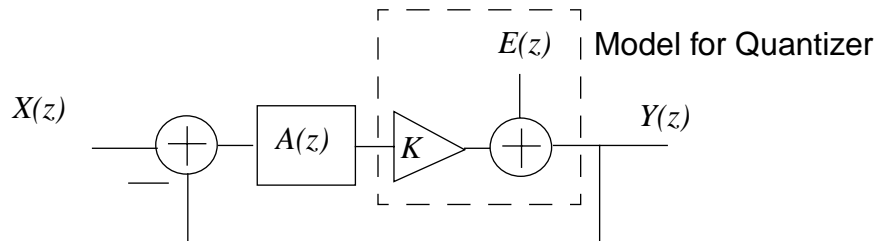


**FIGURE 11. Effect of Feedback on Noise Shaping**

By combining these two concepts, we arrive at the operation of a  $\Sigma\Delta$ M. Now the question remains: How does one design the filter in order to get the right noise shaping.

The first thing we can do is develop a linear model of the system in order to mathematically describe it. If we assume that we can represent the modulator as an additive noise source with an input gain of  $K$ , we can represent the  $\Sigma\Delta$  modulator as the linear model shown in Figure 12, where  $E(z)$  is an AWGN source that represents the noise added by the quantizer (referred to as quantization noise).

### Modulator Architecture



**FIGURE 12. Transfer Function Design of 1st-order  $\Sigma\Delta$  Modulator**

From this, we can define a Signal Transfer Function (STF) and Noise Transfer Function (NTF) as the gain from the inputs  $X(z)$  and  $E(z)$  respectively to the output  $Y(z)$ . The STF only controls the gain that the input signal sees through the A/D converter. The NTF controls the gain that the quantization noise  $E(z)$  sees to the output  $Y(z)$ . Hence, to get noise shaping, we would have to get the NTF to have a gain of zero at some range of frequencies that we are interested in. In other words, we want to place the zeros of the NTF at the narrowband frequencies we would like to quantize.

From the modulator architecture above, we can find the NTF and STF from simple control theory. These are, in terms of the filter  $A(z)$ :

$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1 + KA(z)} \quad (\text{EQ 16})$$

$$STF = \frac{Y(z)}{X(z)} = \frac{KA(z)}{1 + KA(z)} \quad (\text{EQ 17})$$

To simplify the mathematics, the quantizer gain  $K$  is typically assumed to be unity. Here, we can see that the poles of the filter  $A(z)$  end up becoming the zeros of the NTF, and the zeros of  $A(z)$  become the zeros of the STF. In  $\Sigma\Delta$  modulator design, the NTF zeros are the most important parameter to control since the performance of the modulator is directly related to the magnitude of noise that is within the band we are interested in. In order to insure stability, the poles of the STF and NTF must be within the unit circle in the  $Z$  domain. For causality (realizability), we must also make sure the loop is not delay free, hence we usually design  $A(z)$  to have at least 1 delay. For example, if we were to replace  $A(z)$  with a delaying integrator, we would get the following STF and NTF (assuming  $K$  is unity):

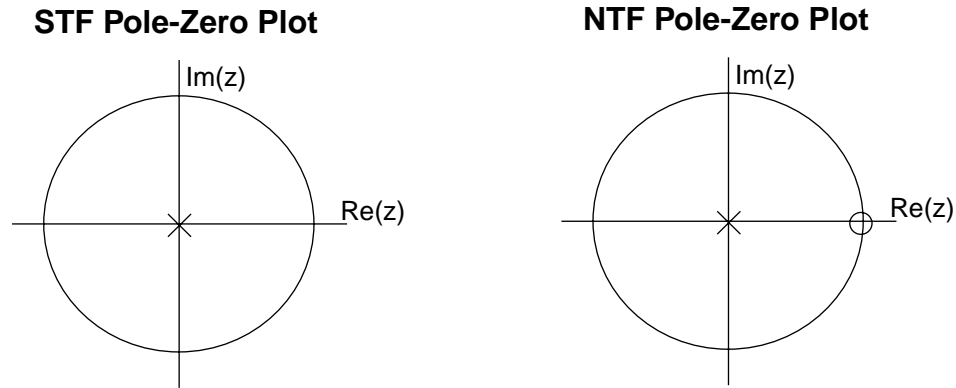
$$A(z) = \frac{1}{z-1}$$

$$NTF = \frac{1}{1+A(z)} = \frac{z-1}{z}$$

$$STF = \frac{A(z)}{1+A(z)} = \frac{1}{z}$$

(EQ 18)

In the Z domain, the STF and NTF look like:



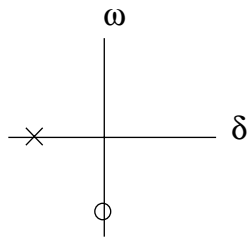
**FIGURE 13. Pole-Zero Plot for STF and NTF for 1st-Order  $\Sigma\Delta$  Modulator**

We have shown a simple first order (with one pole and one zero) NTF and STF but more complicated and higher order NTFs and STF can be realized through filter optimization [Jan94b][Ris94]. We have also seen that we can ‘shape’ the quantization noise away from DC (lowpass  $\Sigma\Delta$ M), but by choosing the appropriate poles and zeros for the filter in the  $\Sigma\Delta$ M feedback loop, we can also shape the noise away from some intermediate frequency. These are normally termed Bandpass  $\Sigma\Delta$ M (BP $\Sigma\Delta$ M) and are well discussed in the current literature [Sch89][Jan92][Sin94][Lon93][Jan93]. The procedure for designing the NTF and STF for BP $\Sigma\Delta$ M is the same as for lowpass  $\Sigma\Delta$ M.

### 3.2 Complex Filter Theory

When designing filters (passive or active), a designer chooses the poles and zeros in order to achieve a desired response, in terms of passband ripple and stopband attenuation. However, in order to realize a real-valued TF, the designer is constrained to having conjugate poles and zeros. If the poles and zeros in the TF are non-conjugate, then the TF ends up having complex coefficients, and therefore a complex-valued filter output [Sne82][All85][Liu86].

#### TF Pole-Zero Plot



#### TF Equations

$$H(s) = \frac{s+j}{s+1} = \frac{s}{s+1} + j\frac{1}{s+1}$$

$$Y(s) = \frac{sX(s)}{s+1} + j\frac{X(s)}{s+1}$$

#### RC Implementation

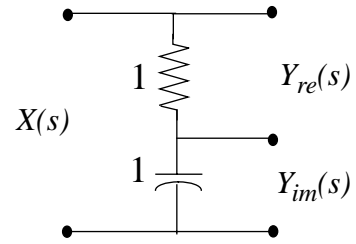
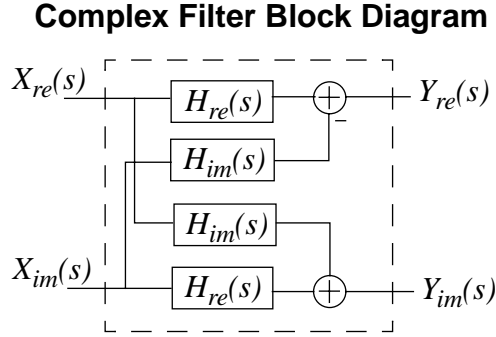


FIGURE 14. Simple Passive Complex Filter

For instance, to realize a given  $H(s) = H_{re}(s) + jH_{im}(s)$ , we can use the system in Figure 14 that has a real input and 2 outputs. The fact that these two outputs correspond to



the real and imaginary part mean they represent a complex signal. One can now extend this to more complicated systems. A general complex filter is shown below in Figure 15.



**FIGURE 15. Generalized Complex Filter (assuming ideal transfer functions)**

In the above filter diagram,  $H_{re}(s)$  and  $H_{im}(s)$  are real-valued transfer functions. This architecture might seem overly complicated (having twice as many filter components as two real-valued filters for each channel) but  $H_{re}(s)$  and  $H_{im}(s)$  usually have the same poles, so much of the hardware can be shared. To show how a complex transfer function is derived from this block diagram, we solve for  $Y_{re}(s)$  and  $Y_{im}(s)$ :

$$\begin{aligned} Y_{re}(s) &= H_{re}(s)X_{re}(s) - H_{im}(s)X_{im}(s) \\ Y_{im}(s) &= H_{re}(s)X_{im}(s) + H_{im}(s)X_{re}(s) \end{aligned} \tag{EQ 19}$$

We can represent  $X_{re}(s)$ ,  $X_{im}(s)$ ,  $H_{re}(s)$  and  $H_{im}(s)$  as complex transfer functions just by multiplying the imaginary part by the complex number  $j$ . This gives us complex  $H(s)$  and  $X(s)$ :

$$\begin{aligned} H(s) &= H_{re}(s) + jH_{im}(s) \\ X(s) &= X_{re}(s) + jX_{im}(s) \end{aligned} \tag{EQ 20}$$

---

We can see (after some algebraic manipulation) that:

$$\begin{aligned} Y_{re}(s) &= \text{Re}[H(s)X(s)] \\ Y_{im}(s) &= \text{Im}[H(s)X(s)] \end{aligned} \tag{EQ 21}$$

So we can also combine  $Y_{re}(s)$  and  $Y_{im}(s)$  into a complex signal.

$$Y(s) = Y_{re}(s) + jY_{im}(s) = H(s)X(s) \tag{EQ 22}$$

In complex numbers, the imaginary part can be thought of as orthogonal to the real part. Similarly in communication systems, two signals which are orthogonal to each other can be thought of as a complex pair. This makes complex filters especially suited for I/Q communication systems. One may now ask why complex filters aren't used more in communication systems. This is primarily because with conventional monolithic components, it is possible to get as much as 3% mismatch between the I and Q channels (which translates to an image rejection of 25dB). With complex filters, the same mismatch can alter the TF much more, since it is asymmetric (as will be shown later).

### 3.3 *Mismatch Effects in Complex Filters*

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It is easiest to study the effects of mismatch in complex filters by studying an example. [All85] provides an in depth discussion of mismatch, which will be summarized here. We

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can take the example complex system of Figure 15, and redraw it if we assume that each transfer function is distinct. This is outlined below in Figure 16.

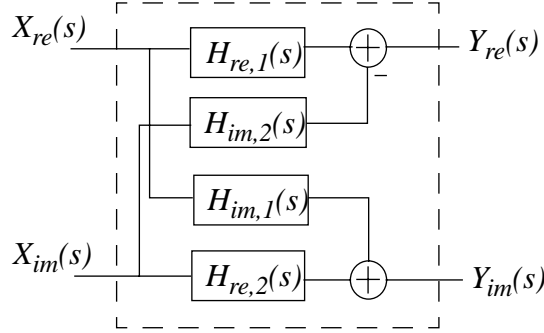


FIGURE 16. Generalized Complex Filter (assuming component mismatch)

Let us assume that the nominal transfer function of the complex filter is  $H_{NOM}(s)$ . Then we can divide the error in the complex filter into a “common mode” TF, and a “differential” TF [All85]. The “common mode” error ( $\Delta H_{CM}(s)$ ) affects both the real and imaginary channels equally, so it can be applied directly to the input to determine its contribution to the output  $Y(s)$ . The “differential” error ( $\Delta H_{DIFF}(s)$ ) causes the signal at the input  $X(s)$  to appear at its complex conjugate at the output. What is more important is that it causes signals at the conjugate of  $X(s)$  to appear directly in the output  $Y(s)$ . In terms of the TF from Figure 16, this gives the following:

$$\Delta H_{CM}(s) = \frac{H_{re,1}(s) + H_{re,2}(s)}{2} + j \frac{H_{im,1}(s) + H_{im,2}(s)}{2} - H_{NOM}(s)$$

$$\Delta H_{DIFF}(s) = \frac{H_{re,1}(s) - H_{re,2}(s)}{2} + j \frac{H_{im,1}(s) - H_{im,2}(s)}{2} \quad (\text{EQ 23})$$

Figure 17 can be shown to be equivalent to Figure 16 with the transfer functions defined by (EQ.23) .

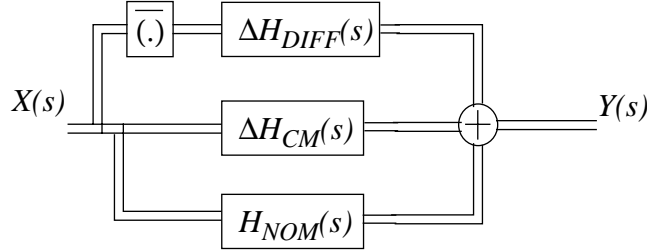


FIGURE 17. Complex Filter with Explicit Error Transfer Functions

For this case, the common mode error is given by  $\Delta H_{CM}(s)$ , the differential error is  $\Delta H_{DIFF}(s)$  and  $\overline{(\cdot)}$  is meant to represent the conjugation operation. We are most concerned about the differential error, since it causes out of band signals to alias inband. For example, take a look at an ideal complex signal  $x(t) = e^{j\omega t}$ . This signal only has power at  $+j\omega$ , but the signal  $y(t) = e^{-j\omega t}$  has power at  $-j\omega$ , the image frequency. If there is any differential error, this image signal propagates to the output along with the original signal. Depending on the structure and layout of the complex filter, mismatch could result in significant performance degradation. One of the problems is that it is hard to quantify this error, without knowing the exact values of each component in the filter. It will be shown in later sections what effects this mismatch has on filters used in a  $\Sigma\Delta\text{M}$ .

### 3.4 Complex $\Sigma\Delta$ Modulation

In a BP $\Sigma\Delta\text{M}$ , we already stated that the filter in the feedback loop (in Figure 12) has a bandpass response. If we were to replace this with a complex bandpass filter, we realize

complex, and therefore asymmetric NTF and STF [Jan94a][Azi95][Swa96b]. This  $\Sigma\Delta\text{M}$  can be analyzed as a complex filter, in that the input is complex (I/Q) and the outputs are single-bit streams, also complex. The obvious advantage to this approach is that a  $\Sigma\Delta\text{M}$  can be designed which has good response in positive frequencies, in exchange for worse response at negative frequencies. The desired signal is modulated to positive frequencies while the image goes to negative frequencies, so this would be advantageous.

The reason this is a good idea can be seen by the ‘Gerzon & Craven Noise Shaping Theorem’ [Ger89] which states that for a given NTF,

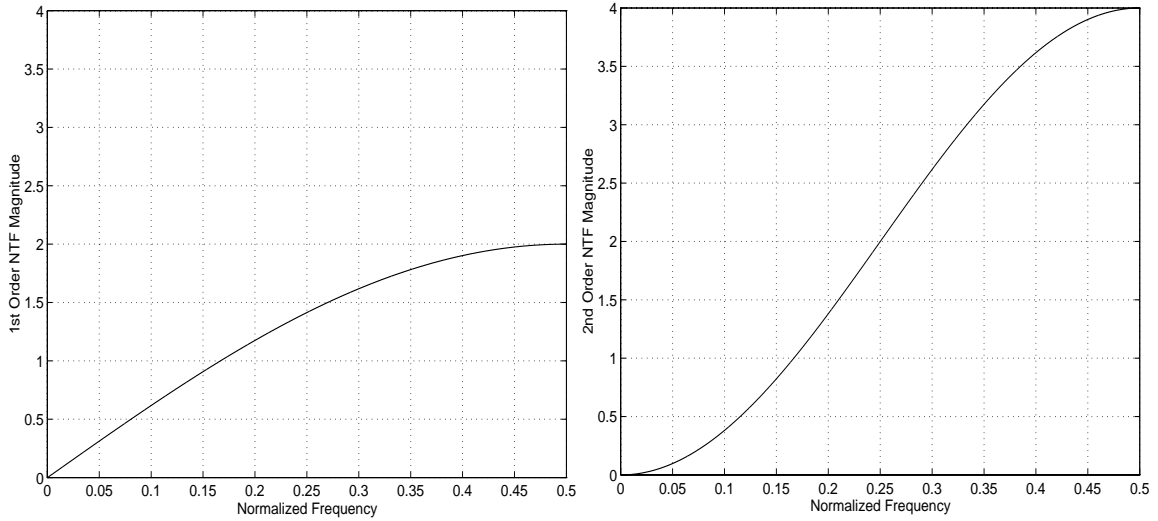
$$\int_0^1 \log |NTF(e^{j\pi f})| df \geq 0 \quad (\text{EQ 24})$$

Where  $f$  is the normalized frequency variable. For minimum phase systems, this integral evaluates to 0. This theorem assumes that the transfer function is real-valued, hence has the same magnitude response in both positive and negative frequencies. But for the complex TF case, we can no longer make that assumption. So, for the general case, the theorem should be written as:

$$\int_{-1}^1 \log |NTF(e^{j\pi f})| df \geq 0 \quad (\text{EQ 25})$$

For minimum phase systems (which is typically what most NTF are designed for), this theorem states that if we would like a wider or deeper notch, we have to pay for it by increasing the out-of-band gain so that the integral evaluates to zero. For example in Figure 18, we can see that a simple 1st order lowpass modulator has 6dB out of band gain.

A 2nd order lowpass has a less noise near DC (deeper notch), but the out of band gain increases to 12dB.



**FIGURE 18. 1st and 2nd Order Lowpass Modulator NTFs**

It is known [Lee87] that for a single-bit quantizer, increasing the out of band gain past a certain point (approximately 1.5) can make the modulator unstable. If we use a complex filter to place more zeros in the passband of the modulator and fewer in the image band, we can see that the out of band gain is still the same, but we have effectively created a deeper notch at the frequency we are interested in. In other words, we have conserved the area below  $\log(NTF)$  by shifting more of it to one band, instead of sharing it between two different bands.

Complex  $\Sigma\Delta$ M are also useful in multi-band systems [Azi95], where one can design each parallel modulator to have NTF notches at different frequencies. As well as that, complex  $\Sigma\Delta$ M also gain a stability vs. bandwidth advantage over real-valued BP $\Sigma\Delta$ M, in that a 4th-order complex modulator can have the same noise-shaping response as an 8th-order real modulator (see Figure 19), yet with a higher order modulator, it is harder to guarantee stability. Similarly for the same order of modulator, the complex modulator is not

restricted to having conjugate NTF zeros, and therefore can have a better notch at the desired frequency.

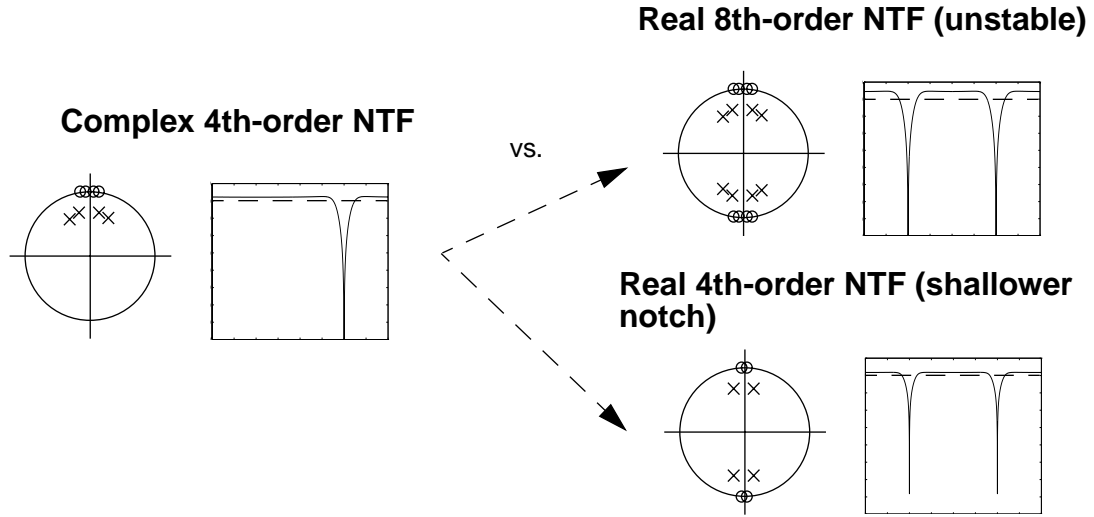


FIGURE 19. Complex vs. Real NTFs

The design of a complex  $\Sigma\Delta\text{M}$  can be done in a couple of different ways. One way is to place the poles and zeros of the NTF and STF (for stability, poles must be inside the unit circle in the Z-domain), as was done in the previous NTF pole-zero plot. Then an optimizer can be run on this pole-zero placement to determine the optimal NTF and STF, given certain constraints on them (discussed in succeeding sections).

Another method is to transform a real-valued TF into a complex-valued TF. This is already done with BP $\Sigma\Delta\text{M}$  by using the following transform [Lon93]:

$$z = -\hat{z}^2 \quad (\text{EQ 26})$$

So, by using this transform,

$$\frac{z-1}{z} \Rightarrow \frac{\hat{z}^2 + 1}{\hat{z}^2} \quad (\text{EQ 27})$$

This transform can work for any function of  $z$ , but is typically used on 1st and 2nd order lowpass  $\Sigma\Delta$  Modulators that meet very specific requirements (NTF zeros at 1 and poles at 0 in the  $Z$ -domain). And this transform places the zeros at  $j$  and  $-j$  in the  $z$ -domain (corresponding to  $f_s/4$  and  $3*f_s/4$  where  $f_s$  is the sampling frequency of the system). A more general bandpass transformation could be:

$$z = \hat{z}^2 - 2Re\left\{e^{j\theta} r_1\right\}\hat{z} - |r_1|^2 + r_1 \quad (\text{EQ 28})$$

where  $r_1$  is a root and  $\theta$  is the angle (in radians) at which the poles and zeros are rotated from their original placement. Even though the NTF is stable (i.e. all the poles are within the unit circle), this does not guarantee that the  $\Sigma\Delta$  Modulator itself is stable [Sch89][Ris94].

The idea of transformation can be readily generalized to complex  $\Sigma\Delta$ M. One way of thinking about it is that we are taking a lowpass  $\Sigma\Delta$  NTF pole-zero plot and rotating it in the  $Z$ -domain. Generally, this can be written as:

$$z = \hat{z}e^{-j\theta} \quad (\text{EQ 29})$$

where  $\theta$  is the angle of rotation in the  $Z$ -domain. For the special case of  $\theta=\pi/2$  ( $f_s/4$ ),

$$z = -j\hat{z} \quad (\text{EQ 30})$$

This is advantageous because it is a simple transformation that can be applied to any lowpass  $\Sigma\Delta$ M. But, once again, this transformation does not guarantee stability. For example in Figure 20, the two NTF are the same, except one is rotated by  $90^\circ$  in the  $Z$ -domain. Simulations show that the complex modulator with the rotated pole-zero constellation is unstable. Unfortunately there is no known way to guarantee stability with



a complex  $\Sigma\Delta$  except by combining NTF design guidelines (which will be outlined in succeeding sections) with extensive simulation.

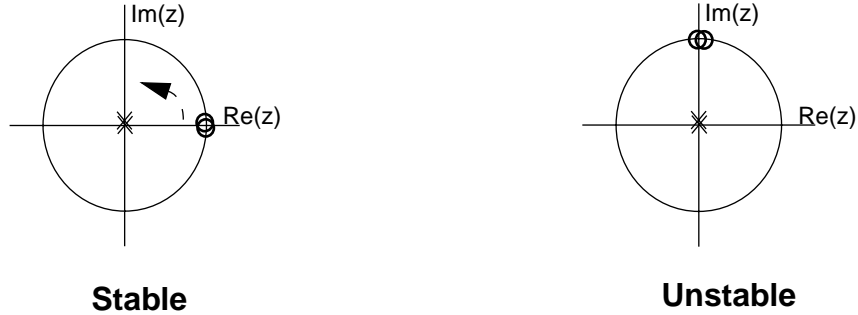


FIGURE 20. Effect of Complex Transform on NTF Stability

In the end, the preferred method is to optimize a lowpass  $\Sigma\Delta$  and use the previous transform (EQ.30) to get the complex equivalent. This method will be discussed in the next section.

### 3.5 Mismatch Issues in Complex $\Sigma\Delta$

One important issue to deal with is mismatch between the I and Q channels of the complex  $\Sigma\Delta$  modulator. In fact, this is an important concern with any I/Q system. We have shown previously (in Chapter 2) that any phase mismatch in the oscillator signal results in an attenuated copy of the image folding onto the desired signal. The same derivation can be done for gain mismatch between the I and Q channels of a quadrature system. And it can be shown that for a 1% gain mismatch between the I and Q channels of a quadrature system (e.g. the quadrature mixer), the image is copied onto the signal with 40dB attenuation [Sne89].

In the complex  $\Sigma\Delta$  that was designed, we may have more than just gain mismatches between the I and Q channels, because we have cross coupling, in order to realize complex poles and zeros. And we already have stated that for a complex system, mismatch causes

the image to be folded into the signal. This can be disastrous for a complex  $\Sigma\Delta\text{M}$ , where any mismatch causes quantization noise at the image frequency (remember we are dealing with a non-symmetric frequency response) to be aliased inband (the deep notch at  $f_s/4$ ). Even if the image quantization noise is attenuated by 40dB before being aliased inband, it can seriously degrade the performance of the modulator. The best example to show this is a modulator that contains all the poles and zeros at  $f_s/4$  (the desired signal frequency) and none at  $-f_s/4$  (the image frequency). For this modulator, we choose the poles and zeros to be:

$$Poles = \pm 0.1 + 0.8j, \pm 0.2 + 0.7j$$

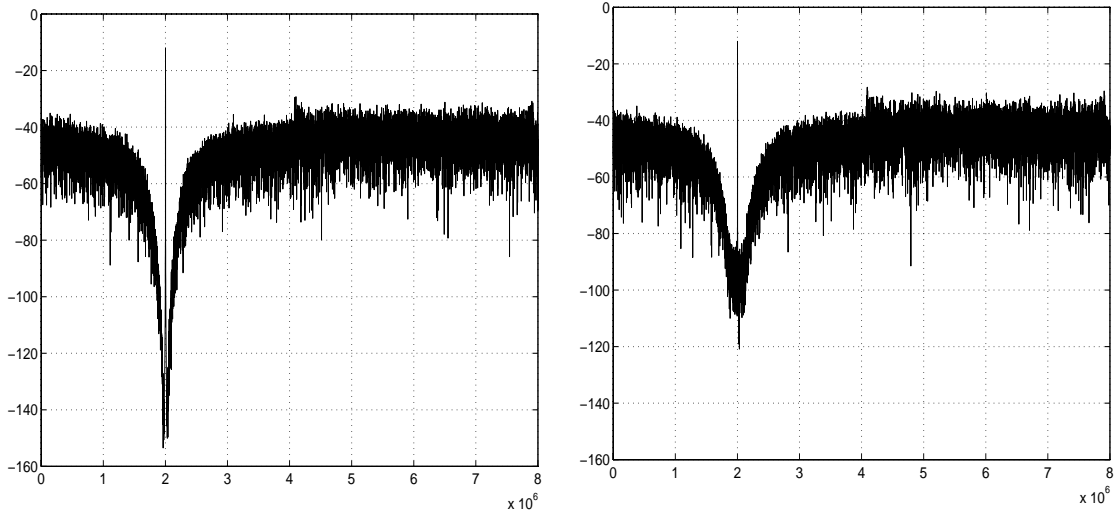
$$NTF_{zeros} = e^{j\frac{\pi}{2}} (quadruple)$$

$$STF_{zeros} = \pm 0.1 + 0.8j$$

$$STF_{gain} = 0.25$$


---

The architecture consists of 4 complex integrators. The frequency responses of these modulators for perfect matching and for 1% random mismatch are shown below in Figure 21.



**FIGURE 21. Response of Example Complex  $\Sigma\Delta$ M for 0% and 1% Coefficient Mismatch**

The SNR of the ideal modulator is 76dB (in a 1 MHz BW) and only 56dB for the mismatched modulator. From this, we conclude that the average SNR degradation is around 20dB which is a loss of approximately 3.5 bits! Obviously we need to design some kind of fix or workaround for this problem, otherwise using a complex  $\Sigma\Delta$  modulator in a communication system would not be practical.

The reason for this SNR loss in complex  $\Sigma\Delta$  modulators was explained in [Jan96a]. The differential error that was discussed before in complex filters can be expressed as an Image Noise Transfer Function (INTF) and an Image Signal Transfer Function (ISTF). They combine to produce an overall modulator output:

$$Y(z) = G(z)X(z) + H(z)E(z) + G_I(z)\overline{X(z)} + H_I(z)\overline{E(z)} \quad (\text{EQ 31})$$

Where  $G(z)$ ,  $H(z)$ ,  $G_I(z)$  and  $H_I(z)$  are the STF, NTF, ISTF, and INTF respectively. These transfer functions represent the gain of the image noise and signal respectively to the inband output of the modulator. The INTF is of most concern, since we could place a complex filter in front of the modulator to attenuate the image signal to the point where the ISTF wouldn't degrade performance. Techniques are discussed in later sections about compensating for the INTF.

### 3.6 *Dealing with Mismatch - Notching Image Noise*

One technique for controlling the INTF was developed and described in [Jan96a]. This involves placing a NTF zero at the image frequency (for the example in the previous section, this means a zero at 6MHz). So, basically, we notch out some of the noise at the image so that less of it gets aliased into the desired signal because of the INTF (Figure 22). In a 4th-order structure, we can realize this image zero at any stage. The question is: which stage is it better to realize this zero in? The first, middle or last?

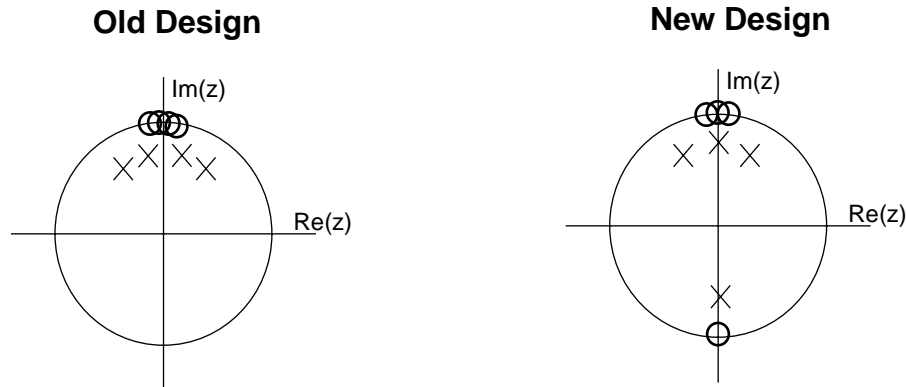


FIGURE 22. Notching Image Noise in NTF

This question was also answered in [Jan96a] where it was determined that creating the image zero in the last stage before the quantizer results in less SNR degradation. The

reason for this was stated by an explanation of input referring the noise. In the modulator, the noise at the input to the quantizer is basically white. Input referring it through each preceding stage (infinite gain at the signal frequency) creates a notch in the noise. Any mismatch in the first stages of the modulator are disastrous because they alias image noise into the signal band. If we notch out this noise first (by placing an image pole in the final stage before the quantizer), we have succeeded in attenuating the image noise, so mismatch in the first stage becomes less of a problem.

### 3.7 *Dealing with Mismatch - Post Compensation*

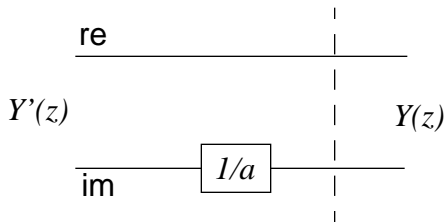
Another way of dealing with mismatch in a complex  $\Sigma\Delta\text{M}$  (or in any complex system for that matter) is to do some gain and phase adjusting after the complex system. For example, let us assume that the ideal output from a complex system is:

$$Y(z) = Y_{re}(z) + jY_{im}(z) \quad (\text{EQ 32})$$

And that our actual output is:

$$Y'(z) = Y_{re}(z) + j(aY_{im}(z)) \quad (\text{EQ 33})$$

We can compensate for this by adding a gain of  $1/a$  to the imaginary channel as is seen in Figure 23.



**FIGURE 23. Gain Compensation for Complex Filter Mismatch**

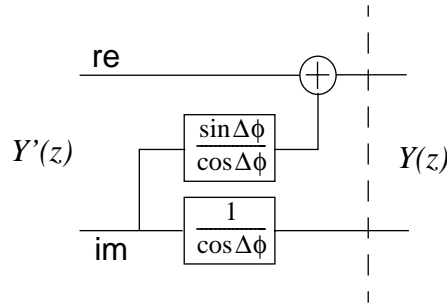
Now let us look at phase mismatches. Say we had a phase mismatch of  $\Delta\phi$  between  $Y_{re}(z)$  and  $Y_{im}(z)$ . Mathematically this would look like:

$$Y'(z) = Y_{re}(z) + je^{j\Delta\phi} Y_{im}(z) \quad (\text{EQ 34})$$

For  $\Delta\phi = 0$ , this reduces to the ideal output shown in (EQ.32). For a non zero  $\Delta\phi$ , we can rewrite  $Y'(z)$  as:

$$\begin{aligned} Y'(z) &= Y_{re}(z) + j(\cos\Delta\phi + j\sin\Delta\phi)Y_{im}(z) \\ &= Y_{re}(z) - \sin\Delta\phi Y_{im}(z) + j\cos\Delta\phi Y_{im}(z) \end{aligned} \quad (\text{EQ 35})$$

Assuming that we know what  $\Delta\phi$  is, we can compensate for this by cancelling the  $Y_{im}(z)$  term in the real part of  $Y'(z)$ , while adjusting the gain of the imaginary part. This compensation system is shown in Figure 24.



**FIGURE 24. Phase Compensation for Complex Filter Mismatches**

We should reiterate that this type of mismatch compensation is based on knowing the magnitude of the mismatch to begin with, which is why it is known as non-adaptive DSP compensation. There are ways of doing adaptive compensation [Li97] which are discussed in succeeding chapters.

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### 3.8 *Complex $\Sigma\Delta$ Transfer Function Design*

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In order to design a good STF and NTF, it is important to adhere to certain guidelines in order to realize TF stability and realizability. Generally, the out of band and in band gain are designed to adhere to certain criteria. The out of band gain is most important for the NTF and is defined as the TF gain which is well outside the bandwidth of the modulator (usually, the magnitude response of the NTF is flat in the out of band region). The in band gain is defined as the TF gain within the specified bandwidth that the modulator is designed for.

It is not intuitively obvious which NTF are stable and which are unstable, but a guideline was proposed by Lee in [Lee87] for 1-bit quantizers which states that the maximum out-of-band gain of the NTF should be:

$$|H(z)| \leq 2 = 6 \text{ dB} \quad (\text{EQ 36})$$

6dB of out of band gain is fairly high as well, which is why  $\Sigma\Delta$  designers usually optimize for less than 5dB. We can show that there are stable modulator NTF (like the lowpass  $\Sigma\Delta$  modulator in Figure 20) which have an out-of-band gain of 12dB. [Ris94] offers another measure by showing that stability of a modulator is dependent on the probability density function (pdf) of the quantizer error. In most cases, this is assumed to have a gaussian distribution. Risbo also showed that for high order modulators (3rd-order lowpass), this pdf assumption is very accurate. This measure of stability was not used for the design of the modulator so it won't be discussed in detail.

Also, to ensure realizability, the feedback loop in the modulator must not be delay free, hence the requirement:

$$H(\infty) = 1 \quad (\text{EQ 37})$$


---

The guidelines for designing the STF are more relaxed since its zeros and gain have no effect on the modulator loop and therefore no effect on stability. The STF has the same poles as the NTF, and one relaxed guideline to follow is to keep the in band gain at unity or:

$$|G(z)| = 1, |\omega| < \omega_0 \quad (\text{EQ 38})$$

This guideline is not necessary, although if the gain is too high, then reduced dynamic range of the modulator can be the result because the STF amplifies interferers as well as the desired signal.

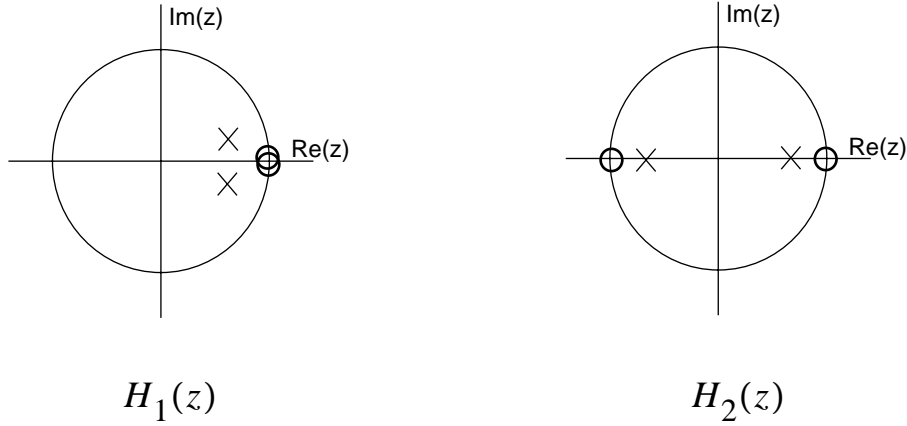
The method that was used to design the STF and NTF for a complex modulator was by optimizing a lowpass  $\Sigma\Delta\text{M}$  by providing initial pole and zero placements and using the preceding constraints. Then we could transform it into a complex BP $\Sigma\Delta\text{M}$  using the previous complex transformation (EQ.30). The filter optimizer that was used to optimize the STF and NTF was filterX, a least-pth optimizer for S-domain and Z-domain filters [Ous90]. The criteria for optimization was to meet a certain in band NTF gain, in band STF gain, and out of band NTF gain. As prototype examples, two designs were attempted; a complex 4th-order and a complex 6th-order. For each of these designs, the complex TF consisted of one complex conjugate pole-zero pair. In order to get filterX to optimize correctly, the STF and NTF were split into two TF: one with the ‘conjugate’ pole & zero (although for the lowpass prototype case, this means a pole/zero at  $0^\circ$  and  $180^\circ$ ) and the other with the rest of the poles and zeros (conjugates for the lowpass case). Mathematically, this looks like:

$$H(z) = H_1(z)H_2(z)$$

$$H_1(z) = \frac{(z-1)^2}{(z^2 + bz + c^2)} \quad H_2(z) = \frac{z^2 - 1}{z^2 - a^2}$$



The poles and zeros of this set of equations look like:



Then the resulting optimized TF were transformed and multiplied together to get the final complex NTF and STF. Using this procedure, the following poles & zeros were obtained for the 6th-order modulator, optimizing for an NTF out of band gain of 5dB, an in band gain of 0 and an STF in band gain of 0dB:

$$Poles = \pm 0.578j, \pm 0.121 + 0.982j, \pm 0.173 + 0.834j$$

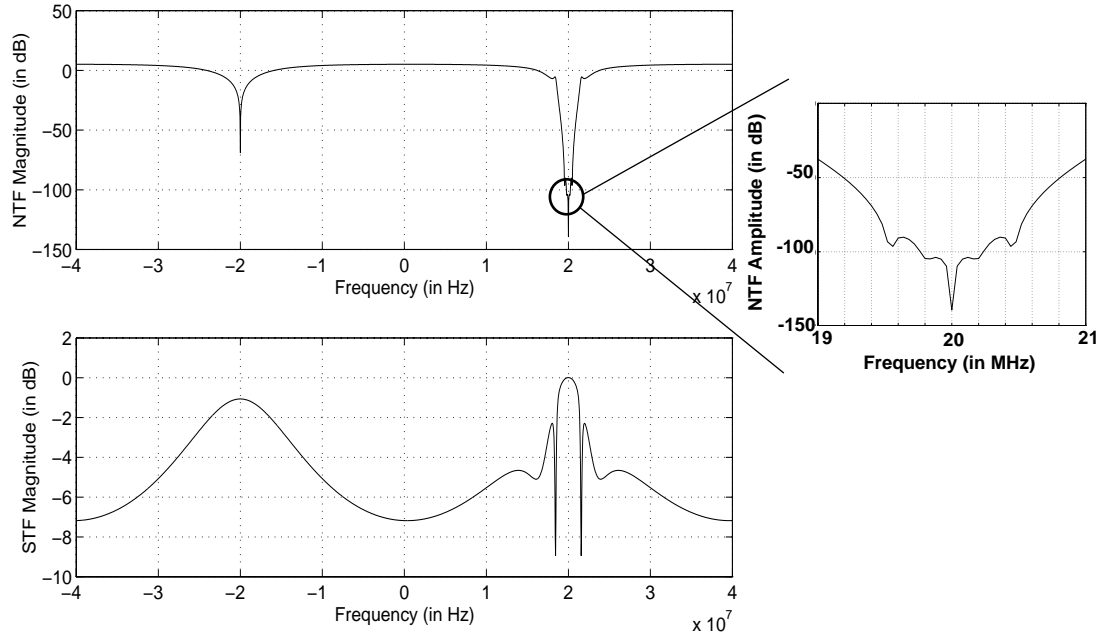
$$NTF_{zeros} = e^{\pm j\frac{\pi}{2}}, e^{j\left(\frac{\pi}{2} \pm 0.036\right)}, e^{j\left(\frac{\pi}{2} \pm 0.015\right)}$$

$$STF_{zeros} = 0, \pm 0.221 + 0.864j, \pm 0.122 + 0.988j$$

$$STF_{gain} = 0.563$$

This gave an STF gain of 0 dB in band (where in band is defined as 400kHz around  $f_s/4$  which is 20MHz), an NTF gain of 5.1dB out of band, and an NTF notch depth of 95dB (relative to NTF out-of-band magnitude) for an OSR of 200. The response of this modulator is shown below in Figure 25 for a sampling rate  $f_s = 80$ MHz. There is a notch at

the image frequency the reason being that with complex filters, mismatch causes signals at the image frequency (-20MHz in this case) to be ‘folded’ onto the desired signal at 20MHz as was already explained previously.



**FIGURE 25. STF and NTF for Optimized 6th-order Complex  $\Sigma\Delta$  Modulator**

The STF was chosen to be bandpass so that it provides some out of band attenuation. But as was mentioned before that this is not as critical as optimizing the notch in the NTF. For

the 4th-order optimized complex modulator, the poles and zeros obtained were (for the same optimization criteria as the 6th order case):

$$Poles = 0.686j, -0.591j, \pm 0.171 + 0.950j$$

$$NTF_{zeros} = e^{\pm j\frac{\pi}{2}}, e^{j\left(\frac{\pi}{2} \pm 0.013\right)}$$

$$STF_{zeros} = 0, \pm 0.224 + 0.971j$$

$$STF_{gain} = 0.283$$

This gave an STF gain of -0.1dB in band, an NTF gain of 5.2dB out of band and an NTF notch depth of 85dB (relative to NTF out of band magnitude). The responses of these TF are shown below (Figure 26).

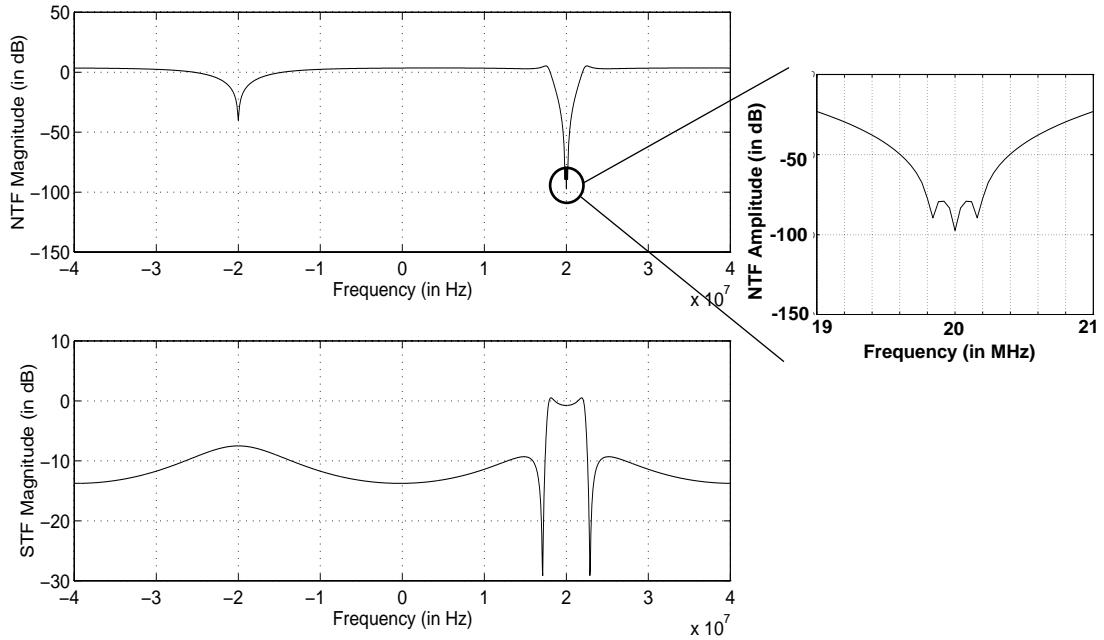


FIGURE 26. STF and NTF for Optimized 4th-order Complex  $\Sigma\Delta$  Modulator

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We can see that the 4th-order NTF has worse response than the 6th-order NTF because we don't have as many NTF zeros to reduce quantization noise in band. And another fact to notice is that the poles and zeros are shown to three decimal places, which will be hard to implement accurately. Whether they need to be accurate to  $1e-4$  or beyond is another question which is discussed in the next chapter.

### 3.9 *Summary*

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Basic principles about  $\Sigma\Delta$  modulators were shown, specifically how oversampling and noise shaping allow us to get increased resolution from an A/D converter. By using complex filters instead of real filters in a  $\Sigma\Delta$ M, we can get better SNR and bandwidths than traditional bandpass  $\Sigma\Delta$ M.

We also looked at the effects of mismatch on a complex filter and complex  $\Sigma\Delta$ M. We saw that for any mismatch, signals at the image frequency get aliased on top of our desired signal. This can be bad for a complex  $\Sigma\Delta$ M, where quantization noise at the image frequency can be aliased in band.

We looked at two ways of dealing with mismatch. One involved attenuating noise at the image frequency so less of it can be aliased inband. The second involved performing gain and phase adjusting in DSP. The next chapter deals with the design and implementation of two complex  $\Sigma\Delta$ M prototypes.

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*“Once you start down the dark path, forever will it dominate your destiny.”*

*- Yoda*

We saw some of the advantages that complex  $\Sigma\Delta$  give over equivalent bandpass  $\Sigma\Delta$  structures in the previous chapter. We also saw some of the problems that we could have with mismatch in this modulator, specifically that image signals get aliased inband. Some solutions to these problems were also discussed.

This chapter concerns the design of two complex  $\Sigma\Delta$  modulators. The second design was intended to be an improvement on the first design in terms of coefficient mismatch sensitivity but requires worse capacitor ratios. Specific innovations that were made to increase the speed of the modulator are also discussed.

## ***4.1 Design Methodology***

---

Initially for this modulator design, we decided to design for a target sampling rate  $f_s=80\text{MHz}$  and a bandwidth (BW) of 200kHz or alternatively, an Oversampling Ratio (OSR) of 200. The reason these values were chosen as was stated before, is that we decided to use PCS as an example to demonstrate these  $\Sigma\Delta$  modulators. For DCS-1800,

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the BW required is 200kHz. And as far as the sampling rate is concerned, the larger the sampling rate, the farther away alias signals are, and the cheaper the anti-alias filter before the A/D converter becomes.

From the previous chapter, we have seen some of the constraints and guidelines we should be designing for. For our modulator, we follow a more conservative guideline than the one proposed by [Lee87] where we limit our out of band NTF gain to less than 5dB.

We have also chosen to design a 4th order complex  $\Sigma\Delta$ M for one important reason. The modulator is a modification of an existing circuit [Phi96] which is a real-valued 4th order bandpass  $\Sigma\Delta$ M. It is much easier to replicate the existing modulator and make some interconnection changes than to design and lay out a higher order modulator from scratch.

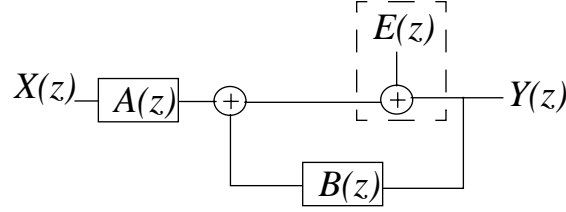
## 4.2 $\Sigma\Delta$ Modulator Architecture

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In any  $\Sigma\Delta$ M, one does not implement the STF and NTF directly, but instead finds feedforward and feedback transfer functions to implement. This was already pointed out in Figure 12, and a slightly different block diagram can be seen in the linear model of Figure 27, where the NTF and STF are expressed in terms of realizable filters in the  $\Sigma\Delta$ M loop. The reason that this block diagram is slightly different is that if we want to implement more complicated transfer functions than the one in Figure 13, we have to have

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a means of setting the zeros of the STF. If this wasn't a concern, then we could set  $A(z) = B(z)$  and get the same effective block diagram as Figure 12.



$$STF = \frac{Y(z)}{X(z)} = G(z) = \frac{A(z)}{1 - B(z)} \quad A(z) = \frac{G(z)}{H(z)}$$

$$NTF = \frac{Y(z)}{E(z)} = H(z) = \frac{1}{1 - B(z)} \quad B(z) = \frac{H(z) - 1}{H(z)}$$

**FIGURE 27. Block Diagram and Implementable TF of a ΣΔM**

We can see now that the zeros of the NTF, or  $H(z)$  become the poles of our new filters,  $A(z)$  and  $B(z)$ . And since we are designing a complex ΣΔM, our  $A(z)$  and  $B(z)$  TF are complex-valued. Since  $A(z)$  and  $B(z)$  share the same poles, we do not implement the ΣΔM as seen in Figure 27, but rather as one filter, implementing the zeros with different feedforward and feedback coefficients.

There are many ways to implement the poles of the TF  $A(z)$  and  $B(z)$ . Two ways are mentioned in [Jan93]; namely a cascade-of-integrators structure which can be thought of as a second canonical form representation with discrete instead of continuous integrators [Sol90]; or a cascade-of-resonators structure (variant of a first canonical form representation with local feedback). And in fact, the structure that was outlined in

[Jan94a] was a direct application of the first canonical form (with complex resonators instead of integrators) as can be seen below:

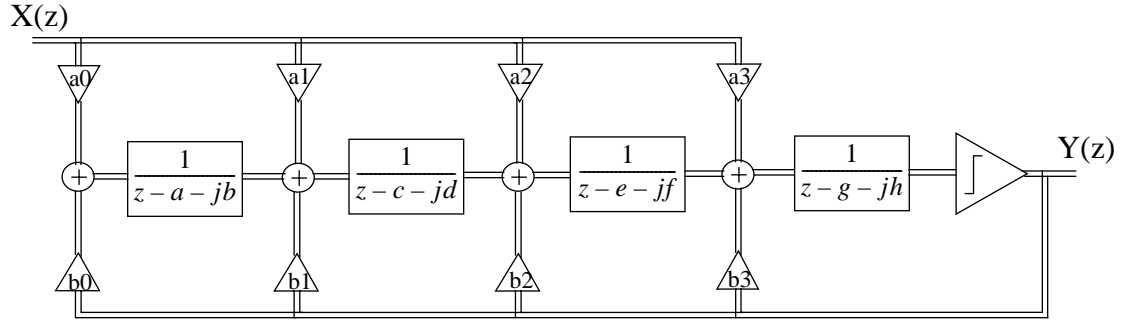


FIGURE 28. Cascade-of-Complex-Integrators Structure for Complex  $\Sigma\Delta$  Modulator

Note that all the feedforward and feedback coefficients are complex-valued. And the double lines represent the fact that the signal traversing the modulator is complex-valued, with a real and imaginary part. It might seem odd to implement a complex-valued resonator, as opposed to the standard discrete integrator. But a complex discrete time resonator was first outlined in [Liu86] and when implemented with real integrators looks like:

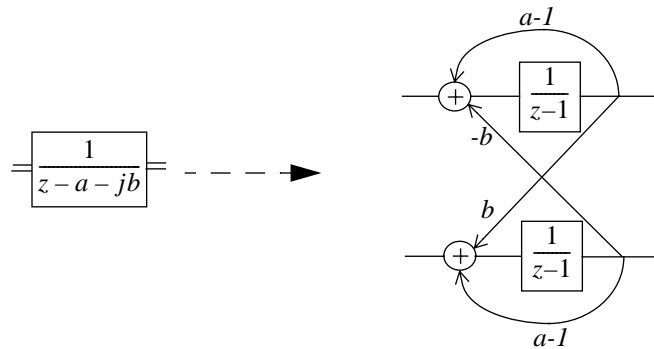
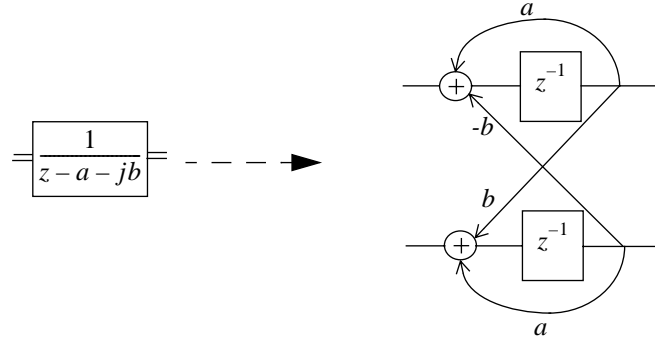


FIGURE 29. Complex Integrator using Discrete-Time Real Integrators



Yet another way to implement the poles of the TF  $A(z)$  and  $B(z)$  is to use a cascade-of-delay-cells architecture [Lon93]. This way, one can implement the same complex resonator by the following:



**FIGURE 30. Complex Integrator using Discrete-Time Delay Blocks**

Both of the preceding architectures are valid, and there are obvious trade-offs between them. The delay-cell architecture is fast and has simple coefficient values, but it turns out that it is more sensitive to low gain in the opamps that are used in the delay cell [Baz96]. The cascade-of-integrators isn't as sensitive to low opamp gain, but has more complex coefficients and is slower than the delay-cell.

The structure that was chosen for the complex  $\Sigma\Delta$  design was the delay-cell architecture, since speed and simplicity were the key parameters governing the design of the  $\Sigma\Delta$ . And we can even simplify the structure given above if we assume that the complex integrator only has to put a pole at  $z=j$ . In that case,  $a=0$ , and  $b=1$ . We will see in the next section that this is, in fact, the modulator we are designing.

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### 4.3 *Complex $\Sigma\Delta$ Modulator A: First Design*

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The method that was used to design the initial NTF and STF was optimizer-based. We start with these optimized transfer functions (we have already shown an optimized 4th order design in the previous chapter) and round the poles and zeros to the nearest tenth. This way, it becomes easier to implement coefficients for the modulator with capacitor ratios. Using this method, with the preceding guidelines for stability for the NTF yielded the following poles and zeros for the NTF and STF of a 4th-order complex modulator (using the previous optimized 4th order modulator as a starting prototype):

$$Poles = \pm 0.8j, \pm 0.2 + 0.7j$$

$$NTF_{zeros} = j(triple), -j$$

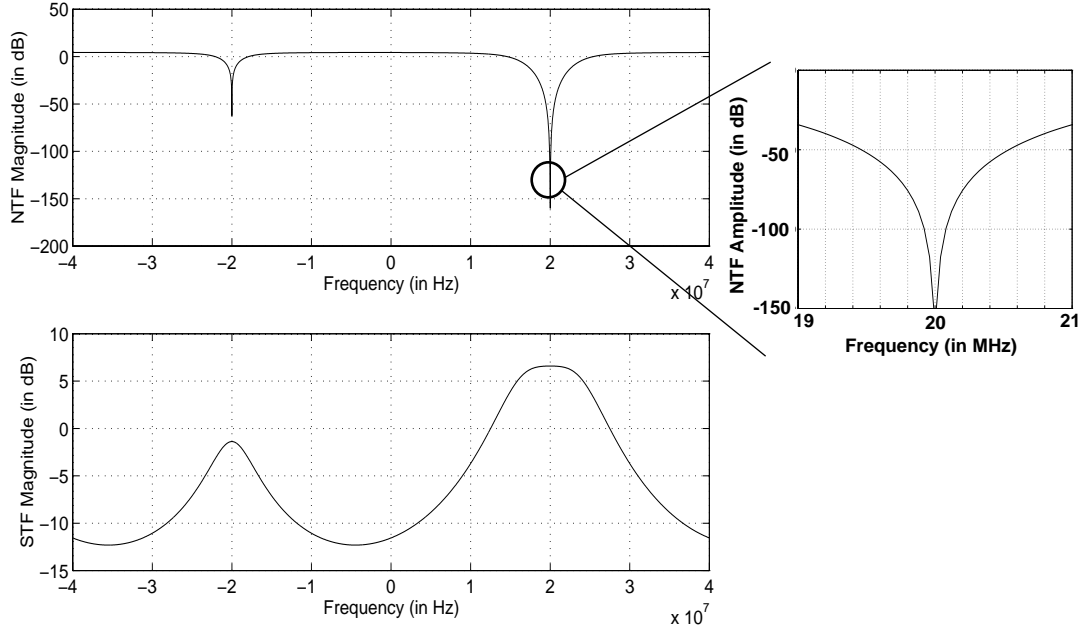
$$STF_{zeros} = 0.8j$$

$$STF_{gain} = 0.5$$

These poles and zeros give us an STF gain of 6.6dB in-band, an NTF gain of 4.4dB out-of-band, and a notch depth of 92dB (relative to NTF out-of-band magnitude) within a

---

bandwidth of 400kHz for an OSR of 200. The associated magnitude responses of these TF are given below in Figure 31:



**FIGURE 31. STF and NTF for 4th-Order Complex Modulator with no Optimization**

For these TF, we have 3 poles of  $A(z)$  and  $B(z)$  at  $z=j$ , and one pole at  $z=-j$ . The  $z=\pm j$  pole pair can be implemented as a straight resonator, from [Lon93], one in the real path and one in the imaginary path, and the other 2 poles at  $z=j$  can be implemented as outlined above.

Now we look at the transfer functions we have to implement,  $A(z)$  and  $B(z)$ , based on the STF and NTF poles and zeros outlined at the beginning of this section. We can implement the resonator for the notches at  $z=\pm j$  in either the first stage or the second stage. For this first implementation, we implemented this resonator in the first stage, and the complex

resonators in the second stage. The Z-domain block diagram for this structure using delay-cells is outlined below in Figure 32:

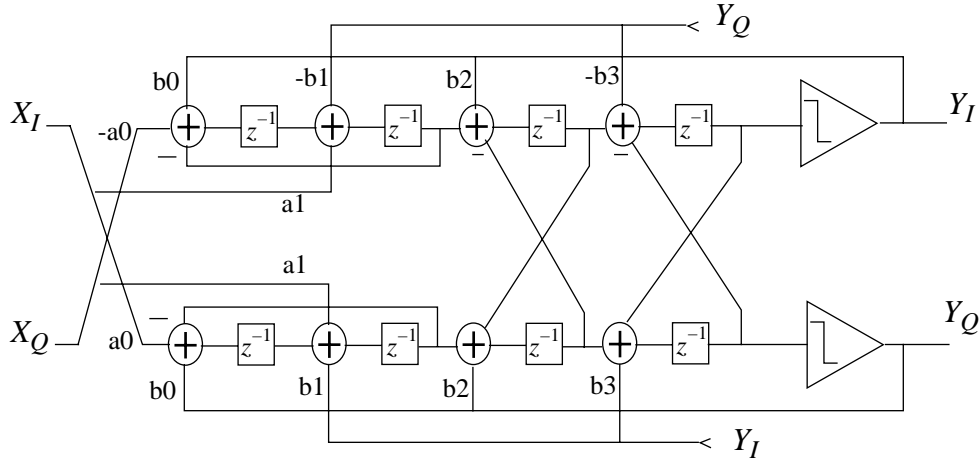


FIGURE 32. Z-domain Block Diagram of Complex  $\Sigma\Delta$  Modulator A

Where coefficients are not shown, the gains are unity. In the two channels, we can note that some of the coefficients ( $a_i$ ,  $b_i$ ) have their sign and inputs reversed between the real and imaginary channels. This is a result of implementing an imaginary-valued coefficient in  $A(z)$  and  $B(z)$ . In Figure 32 for example, we can see that for  $a_0$  which is imaginary, we have a crossover, where  $a_0$  multiplied by an imaginary number gives a real number with a sign change. The coefficients used to implement the  $A(z)$  and  $B(z)$  TF are outlined below (see Appendix A for calculations). Since all the coefficients are either pure real or pure imaginary, we reduce our complexity by a factor of 2 over an optimal design, which has complex coefficients with both a real and imaginary part.

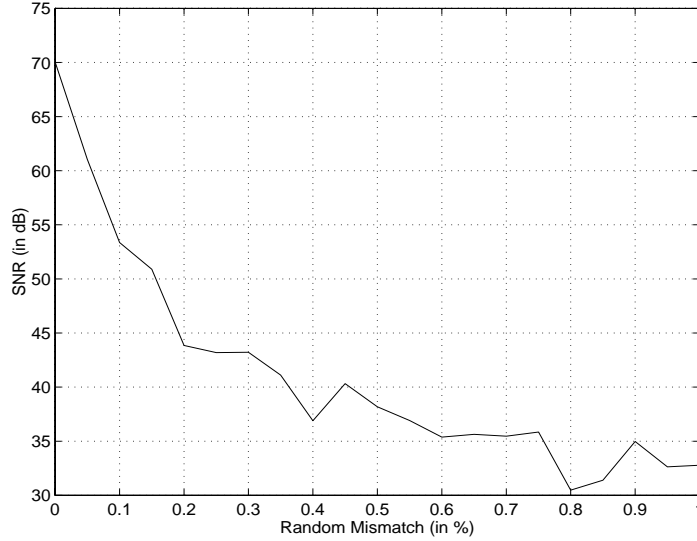
TABLE 2. Coefficients for Complex  $\Sigma\Delta$  Modulator

Coefficient	$a_0$	$a_1$	$b_0$	$b_1$	$b_2$	$b_3$
Value	$-0.4j$	0.5	-0.55	$-0.5j$	0.5	$-0.6j$

Since the designed modulator has a discrete-time structure, it is necessary to implement it with sampled-data circuits. This can be done easily with switched-capacitor (SC) technology, which has been documented extensively in the literature [Sne96][Gre83][Gre86]. All these coefficients are relatively close in value to each other, and have simple rational values which make them easy to implement and match with standard capacitors in this SC design. In this circuit, the maximum ratio between coefficients is 1:2.5 (remember some of our coefficients are unity) which is even better from a space-saving point of view (large ratios could mean the simultaneous use of very large and very small capacitors [Gre88]). This is another reason why this structure was chosen, because if we implement large capacitors (for large coefficient ratios), we would obviously reduce the operating speed of the modulator and if we implement very small capacitors instead, we increase  $kT/C$  noise and get worse performance from the modulator. As it turned out, it was decided that having a 375 fF unit capacitor would come closer to meeting our speed requirements than 500 fF units.

We mentioned before that mismatch in a complex  $\Sigma\Delta\text{M}$  can degrade its SNR performance. We should look at the effect of this on “Modulator A” that we have just designed. Figure 33 shows the effect of mismatch in Modulator A for random coefficient mismatch on all

coefficients up to 1%. The SNR is calculated from a 16384 pt. FFT, averaged over 10 modulators.



**FIGURE 33. Effect of Mismatch on Complex  $\Sigma\Delta$  Modulator A**

This corresponds to Figure 21 where the notch gets degraded with mismatch. This design was initially done without knowing the results in [Jan96a], so we had little idea that the matching performance would be so poor even though we place an NTF notch at the image frequency. The next section describes the second implementation that was done to help correct this sensitivity to mismatch.

#### 4.4 *Complex $\Sigma\Delta$ Modulator B: Improved Design*

To combat this mismatch problem, a new modulator was designed, based on the existing Modulator A. [Jan96a] stated that to minimize the effects of mismatch, one should realize the conjugate NTF zero at  $z=\pm j$  in the last stage of the modulator. Modulator A realized this in the first stage of the modulator as can be seen in Figure 32. This new modulator was

designed to realize exactly the same NTF and STF poles and zeros as Modulator A and hence has the same ideal performance.

To illustrate this design, we have modified the existing structure to create the image NTF zero in the last stage. This is shown in Figure 34 where we have exchanged the order of the two biquads in the modulator.

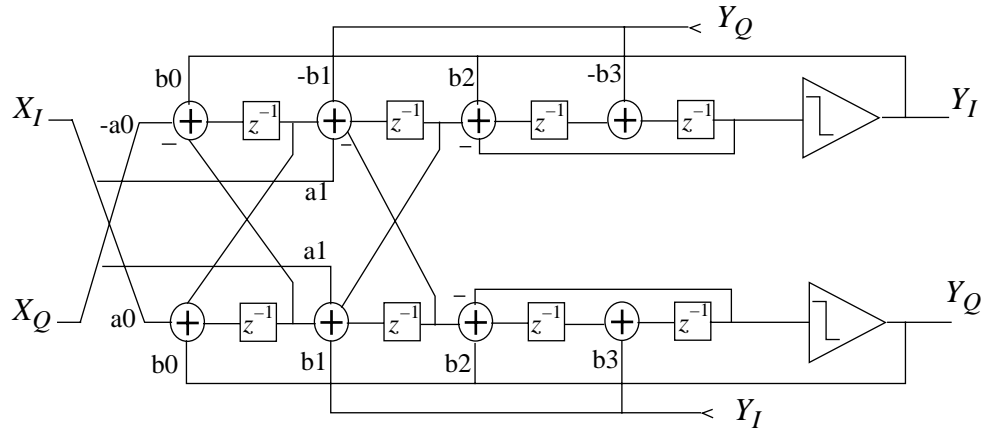


FIGURE 34. Z-Domain Diagram of Complex  $\Sigma\Delta$  Modulator B

One problem with this structure that was mentioned before is that the coefficient ratios become bigger. In the previous architecture, the coefficients were simple ratios (e.g. 0.55), and the maximum ratio between coefficients was 2.5:1. With this architecture, however, the maximum ratio is 25:1. This means we either have ultra small capacitors with high  $kT/C$  noise, or large capacitors which reduce the maximum operating speed. The coefficients for this modulator are outlined below in Table 3 (see Appendix A for calculations). For these coefficients, the only thing different between this architecture and Modulator A is

that the STF gain is 12dB inband and 4dB in the image band instead of the corresponding 6dB and -2dB for the old modulator.

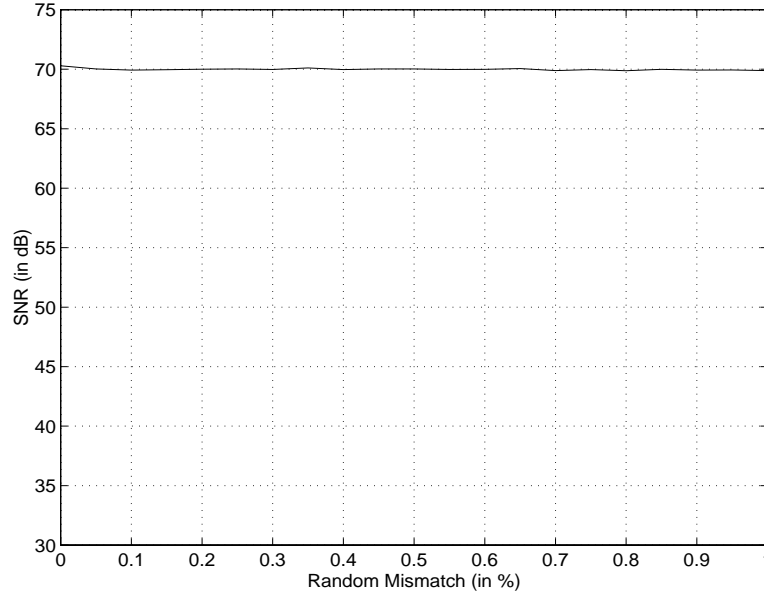
**TABLE 3. Coefficients for Improved Complex  $\Sigma\Delta$  Modulator**

Coefficient	a0	a1	b0	b1	b2	b3
Value	0.2j	1	-0.047	0.48j	1.1	-0.6j

In spite of the capacitor ratios, it is still feasible to design a modulator of this type. We can see the advantage in Figure 35, where 1% random mismatch only degrades the SNR by 1dB instead of 35dB for Modulator A! This is an overly optimistic graph, since ultra-small capacitors will tend to have more mismatch than larger ones [All83] (for this BiCMOS process, capacitor mismatch was measured to be 0.6% for 0.5pF square capacitors) and also for larger mismatches, we can expect that the SNR will degrade by more than 1%. But the ultra-small capacitors in this design are in the feedback from the output quantizer, and affect the poles of the NTF and STF of the modulator. Through analysis, it was found that a coefficient of 0 for b0 (100% reduction in its present value) places a pole at  $z=\exp(j*\pi/2)$  in the Z-domain and leaves the other three poles relatively unaffected. This happens because b0 provides the only damping for the first complex resonator. Without it, the only parts of the architecture which set the poles and zeros are the second complex resonator and the real resonator (an equivalent 3rd order system). Another simulation was also done, where the coefficients were mismatched by random 1% errors except for the a0 and b0 coefficients, which were mismatched by 3% and 5% respectively (a more accurate estimate of error). This turned out to degrade the SNR by 2dB instead of the 1dB stated



previously. So, we can infer that for modest mismatches, the SNR will decrease only slightly.



**FIGURE 35. Effect of Mismatch on Improved Complex  $\Sigma\Delta$  Modulator**

This architecture enhancement of moving the real resonator to the last stage of the modulator helps reduce the image quantization noise aliasing inband. But this has no effect on any input signals at the image frequency. The gain of these signals is controlled by the STF, which will be as sensitive to mismatch as Modulator A. The next section shows a method to deal with this image signal problem.

## 4.5 *Adaptive DSP Compensation for Mismatch*

One of the problems with the above modulator is that even though it is supposed to have a better effect on aliased image noise, it doesn't do anything about any image signals at the input of the modulator. We stated before that 3% differential gain error in an I/Q system (say, an I/Q mixer) results in 25dB IR.

One way to correct this problem might be to have small top metal links with small capacitances that can be connected to the capacitors in the circuit to correct for mismatch. The obvious disadvantage to this is that each chip must be corrected by microsurgery, which is not really viable for production.

Another way was mentioned earlier, which is to increase the size of the capacitors until mismatch is no longer a problem (say,  $< 0.1\%$ ). Of course, as discussed before, this degrades the operation speed of the modulator or consumes more power if we still want to operate at the same speed, which defeats the purpose of a single-IF receiver architecture for portable communications.

A better method is to try and correct for the mismatches in DSP. We can do this one of two ways: on-line (or adaptive) or off-line compensation [Kia93][Cau96][Wei96]. The preferred way is adaptive, so we can correct for errors that may occur over time. One method of doing this is to use a Least-Mean Squares (LMS) Finite Impulse Response (FIR) filter [Wid85]. The LMS algorithm is simple, and can be easily implemented in DSP. It uses an adaptive linear recombination method to calculate an error, and uses this error to update its filter tap coefficients. Mathematically, this looks like:

$$W_{k,n+1} = W_{k,n} + \mu \epsilon_n X_{k,n} \quad (\text{EQ 39})$$

where  $W_{k,n}$  is the  $k$ th tap coefficient at time  $n$ ,  $\mu$  is the gain constant that controls rate of convergence of the filter,  $\epsilon$  is the error signal (input minus output of LMS filter) and  $X_{k,n}$  is the  $k$ th input in the filter at time  $n$ . The effect is to cause the tap coefficients to converge so that the error signal is minimized. This is useful if we would like to minimize an undesirable signal in a filter output.

The method by which this works can be seen in Figure 36. The output of the complex  $\Sigma\Delta\text{M}$  is a pair of bitstreams, representing the complex response of the modulator.

Normally, we mix the signal down to baseband, then perform decimation filtering to remove out of band noise from the  $\Sigma\Delta$  output. We have already stated that any mismatch causes signals and quantization noise at the image frequency band to alias on top of our desired signal band.

Since we know that in the signal band, the degradation is correlated with the image band, we can mix the image down to baseband, and use an FIR filter with LMS updated tap coefficients to estimate the correlation of this image signal to the degradation, and subtract it from the output of the  $\Sigma\Delta$ . This has the advantage that it not only compensates for image signals that might alias inband, but it can also compensate for image noise that aliases inband [Li96]. It is also important to note that since we are dealing with complex signals, the error signal used to update the tap coefficients is complex, and the LMS algorithm of (EQ.39) is used on complex inputs, tap coefficients, and error signal.

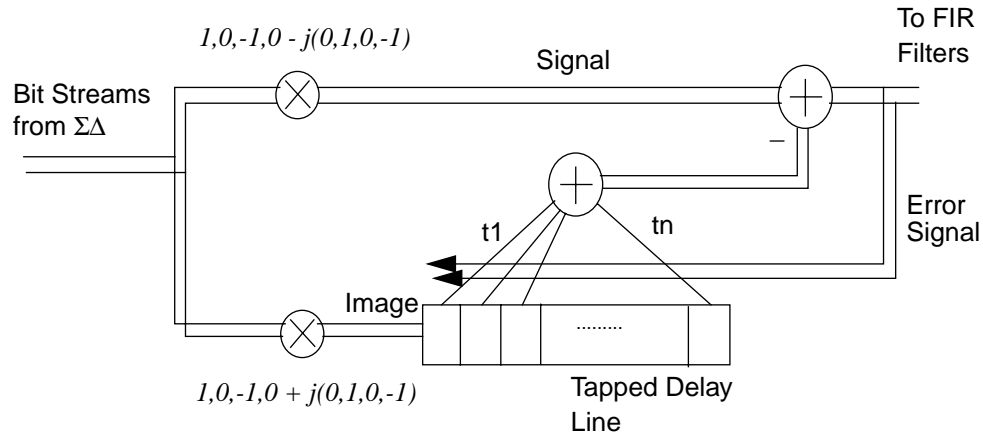


FIGURE 36. DSP Solution to Mismatch Problem

This is just a simulated idea now. More research outside the scope of this thesis needs to be done to answer key questions, for instance, should some decimation and filtering be done on the signal and image before using the LMS algorithm? To give the reader some insight into this question, we can look at Figure 37, which shows what we hope to gain from the DSP system shown in Figure 36. This compensation is being done at the

oversampled rate with no decimation (as we can see, there is still quantization noise in the spectra). One problem might be that the high power out-of-band noise might make the LMS filter fail to converge to the right coefficients. The obvious solution to this would be to decimate, do some filtering on the out-of-band noise, and then use the LMS filter. Now, the filter might not converge as fast since we are operating at the decimated rate, but this is probably not a concern, since when the tap weights converge, they will remain around the same value regardless of the change of image signal.

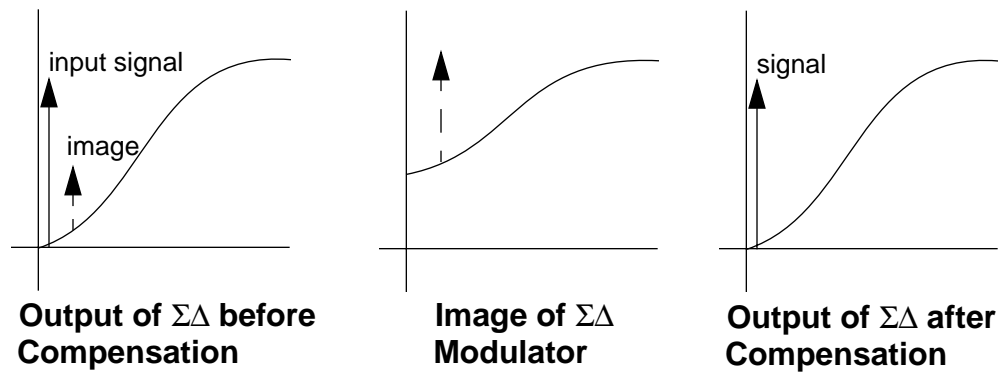


FIGURE 37. Comparison of Spectra in the DSP Solution to Mismatch

Another question is: Usually the LMS algorithm operates so as to make the error signal (in this case, the output of our DSP solution) as close to zero as possible. But our error signal has a large component of our received inband signal, which may have the same effect on the convergence as the large out-of-band noise in the oversampled DSP system.

Needless to say, the importance of adaptive DSP compensation cannot be underestimated since we have shown that modest mismatches in a complex  $\Sigma\Delta$  modulator can result in very serious SNR degradation, but that designing the modulator to control the problem compromises the practicality of the circuit.

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## 4.6 *Summary*

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In this chapter, we have looked at two basic designs that were implemented for a complex  $\Sigma\Delta$ . Both designs were implemented on the same platform chip, using the same general architecture and the target design specification was listed as a sampling rate  $f_s=80\text{MHz}$  with a 200kHz BW.

Both designs were innovative in that each coefficient was either pure real or pure imaginary so that only half the number of coefficients were needed over an optimal design where all the coefficients were complex. The first design (Modulator A) had the advantage that the coefficient ratios to implement were 2.5:1 or less. However it was found to be sensitive to mismatch. The second design (Modulator B) was less sensitive to mismatch, but had larger coefficient ratios to implement (25:1).

These mismatch effects could be corrected with adaptive filtering in DSP. Currently research is being done in this area [Li96] as a viable correction mechanism for complex  $\Sigma\Delta$  modulators.

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## ***CHAPTER 5***      ***Complex $\Sigma\Delta$ Modulator*** ***- Implementation &*** ***Results***

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*“Where’s the kaboom? There was supposed to be an earth-shattering kaboom!”*

*- Marvin the Martian*

So far, we have looked at the theory and advantages behind complex  $\Sigma\Delta$  modulators. We have also looked at the design of two modulators based on the same architecture. Different advantages were presented for each of these designs.

Now, we can look at the results for these modulators. The improvements that were suggested in the previous chapter that lead to Modulator B will be examined in depth here as comparisons between the two modulators are drawn.

### ***5.1 Circuit Structure***

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The modulators were implemented in parallel with an existing production chip [Phi96], so most of the circuits used were already designed for this application. It has already been shown how to implement the complex SC integrators in Figure 28 in [Liu86] and the delay-cell used above in [Lon93]. By combining these two approaches, we can arrive at a complex integrator structure using SC delay-cells.

The SC version of the delay cell used is shown below in a simplified single-ended schematic. This particular feedback was chosen so that the capacitor ratios become simpler. We can see from this that the effect of finite opamp gain on a SC delay cell [Sne96] is doubled, because we are transferring charge twice using the same opamp before feeding it to the next stage, as opposed to normal SC integrators which only transfer the charge once. Clocks  $\phi 1$  and  $\phi 2$  are non-overlapping, as usual for SC design.

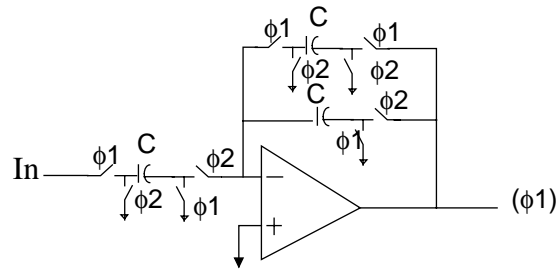
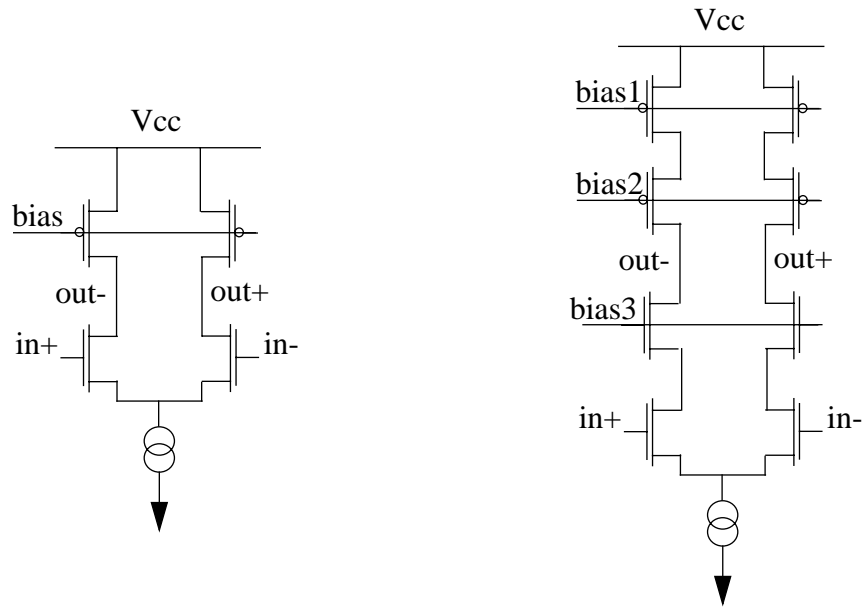


FIGURE 38. Switched-C Delay Cell

Once the architecture was chosen, then the obvious next step was to design the associated circuits for the modulator. These include the switches, opamps, comparator, and clock generator, the opamp being the most important of these. In an opamp, it is desirable to have a high unity-gain bandwidth (UGBW) for high frequency operation, as well as high gain and high output dynamic range. But it is impossible to design for all these considerations, so one must settle on a compromise. For example, to get high output swing, one could design a simple differential pair amplifier with a single-transistor current source load (see Figure 39) but this would not have very high gain. To increase the gain (without sacrificing the speed) we could add cascode stages to increase the output

resistance, since the gain of a transconductance amplifier is proportional to  $g_m * R_O$ . The only problem is that our output swing is reduced (by one  $V_{on}$ ).



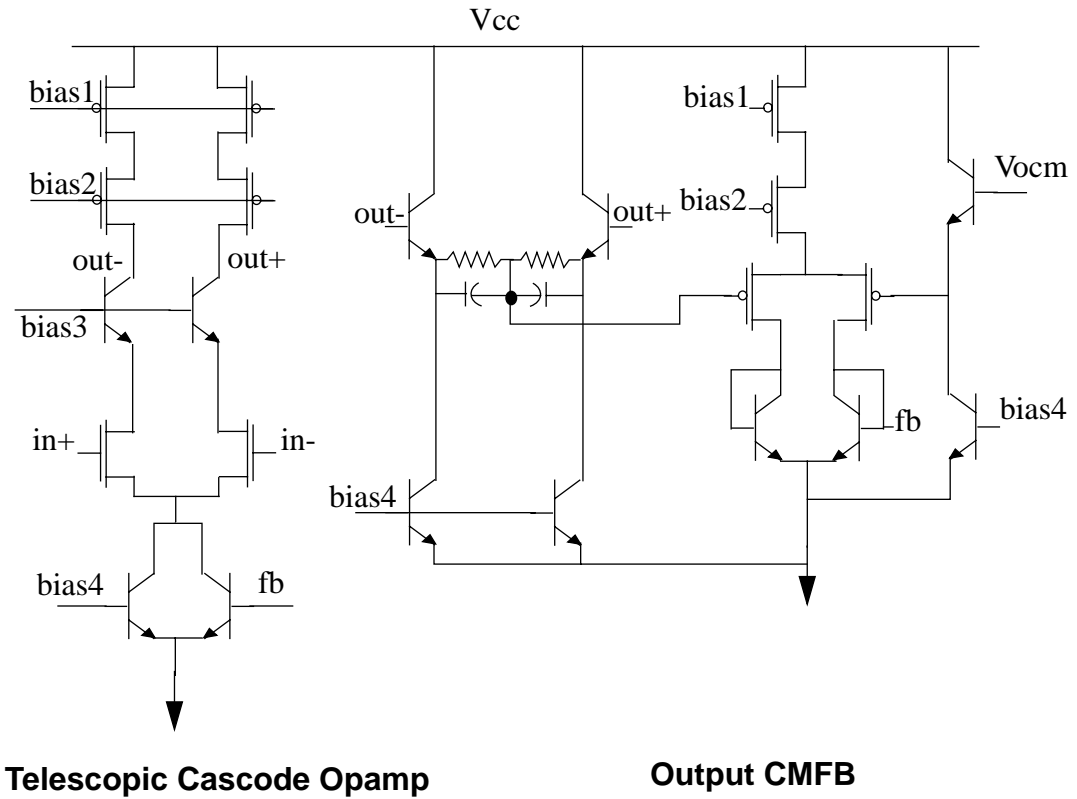
**Single-transistor Output Stage Opamp    Telescopic Cascode Opamp**

**FIGURE 39. Single-transistor vs. Cascode Opamp Circuits**

The opamp used in the platform chip is a BiCMOS telescopic cascode [Sen94], which gives us high gain. It also has Common-Mode Feedback (CMFB) [Sin94][Ban88] which



keeps the output common-mode voltage from drifting. The schematic of the opamp, including common-mode feedback, is shown below in Figure 40:



**FIGURE 40. Telescopic Cascode Opamp used in Complex SD Modulator**

Having bipolar transistors in a mainly CMOS opamp is useful, both for current sources and as a cascode stage on the input of the opamp. The simulation results and experimental results of this opamp will be discussed in the next section.

The next circuit that was needed was a clocked comparator that yielded TTL levels. Once again, this was available on the platform chip that this modulator was designed upon

[Phi96]. The comparator was a simple differential pair with a sense-amp stage to give TTL output levels. The schematic for this is as follows:

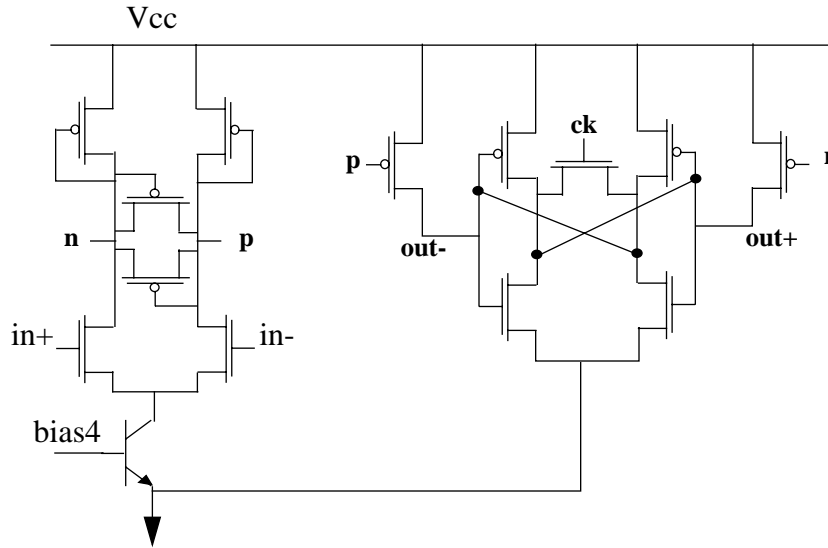


FIGURE 41. Comparator used for Modulator

The final two circuits needed were a low-resistance switch and a high output drive clock generator. The switch is a simple transmission gate, widely used in SC networks, with a W/L ratio of 40/0.8, in order to have a low enough on resistance to meet settling time constraints. The clock generator was a simple RS flip flop with inverters; for different delays on the clock and extra output drive. The schematic for the clock generator is shown below in Figure 42:

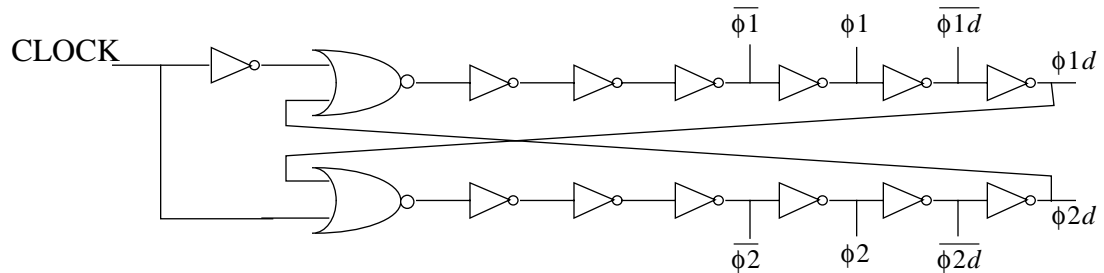


FIGURE 42. Clock Generator Schematic

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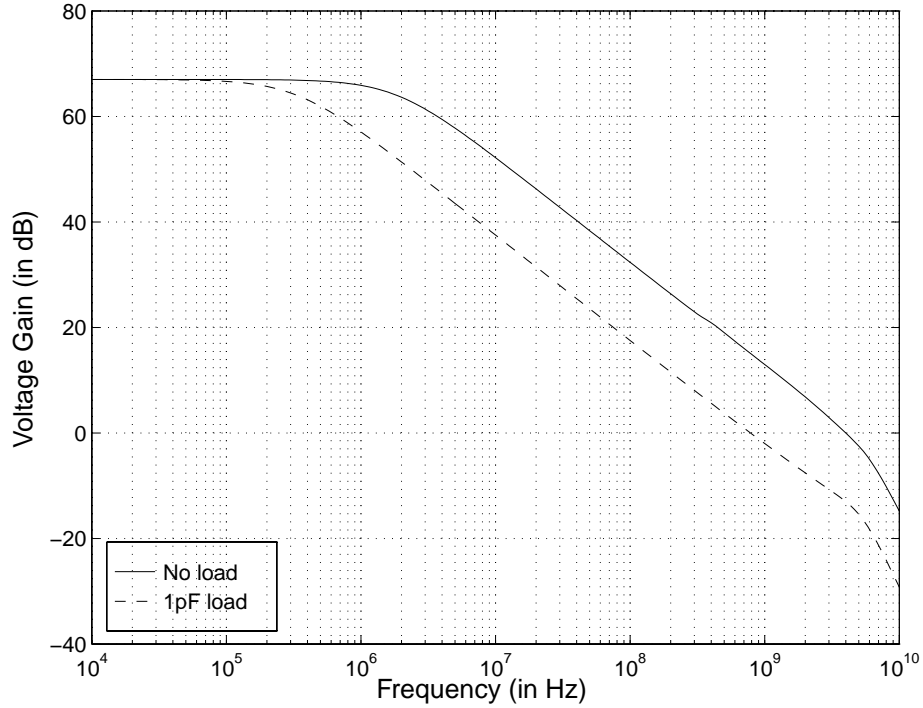
## 5.2 *Performance of Circuit Blocks*

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Ideally, the first circuits simulated and tested would be the individual circuit elements that are used in the modulator, since these are the building blocks that are used in the design. This doesn't usually happen because the turnaround time of several months for test circuits is the same as the turnaround time for the entire modulator. In the previous chapter, four circuits were outlined: the opamp, clock generator, comparator and switch. In each case, it is important that the circuits meet certain minimum specifications.

The first block that we will talk about is the opamp. The opamp has to have high gain at high frequencies, since we would like to clock the  $\Sigma\Delta$  Modulator at 80MHz. For the platform chip which this  $\Sigma\Delta$  Modulator was based on, the opamp was designed to have a DC gain of 60dB [Baz96], because as was pointed out in the previous chapter low opamp gain is more detrimental to delay-cells than SC integrators. It had a UGBW of at least 5 times the sampling frequency, or 400MHz (which has been shown to reduce performance degradation in [Sin94][Mar81]) for loads of 1pF.

Shown below is the magnitude response of the opamp (simulated) with and without a 1pF load. We can see here that for the 1pF load, the UGBW is 794MHz and the DC gain is 66dB. These are well within our specifications above.



**FIGURE 43. Opamp Response (Simulated)**

It should be noted that the above figure is an overly optimistic estimate of the speed we can operate the SC circuit at. In [Baz96], the effective unity gain frequency is derived for a SC integrator, with an input capacitance from the amplifier. It is shown that for opamp input capacitances comparable to the integrator and input capacitors, the total load capacitance on the output of the opamp can be increased by 50%.

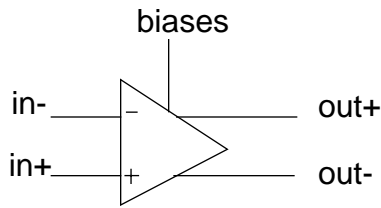
The simulated results of the remaining circuit blocks (comparator, switch, clock generator) are summarized in Table 4.

**TABLE 4. Simulated Performance of Circuit elements of Modulator**

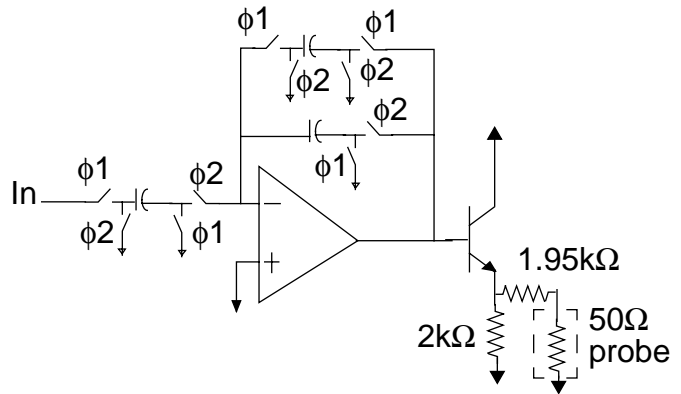
Block	Parameter	Value
Comparator	Resolution (due to metastability)	2mV Sensitivity (7-bit)
Switch	On-Resistance	300 $\Omega$
Clock Generator	Rise Time (max)	0.16 ns
	Fall Time (max)	0.19 ns
	Non-Overlapping time	0.568 ns
	Delay time (between clock and delayed clock)	0.17 ns

Circuits were built for both Modulator A and Modulator B and contain two test structures; one for testing the DC gain of the opamp, and the other for testing the settling time of a differential SC delay-cell with a 1pF load. The test circuits are shown below in Figure 44:

#### Opamp Test Structure



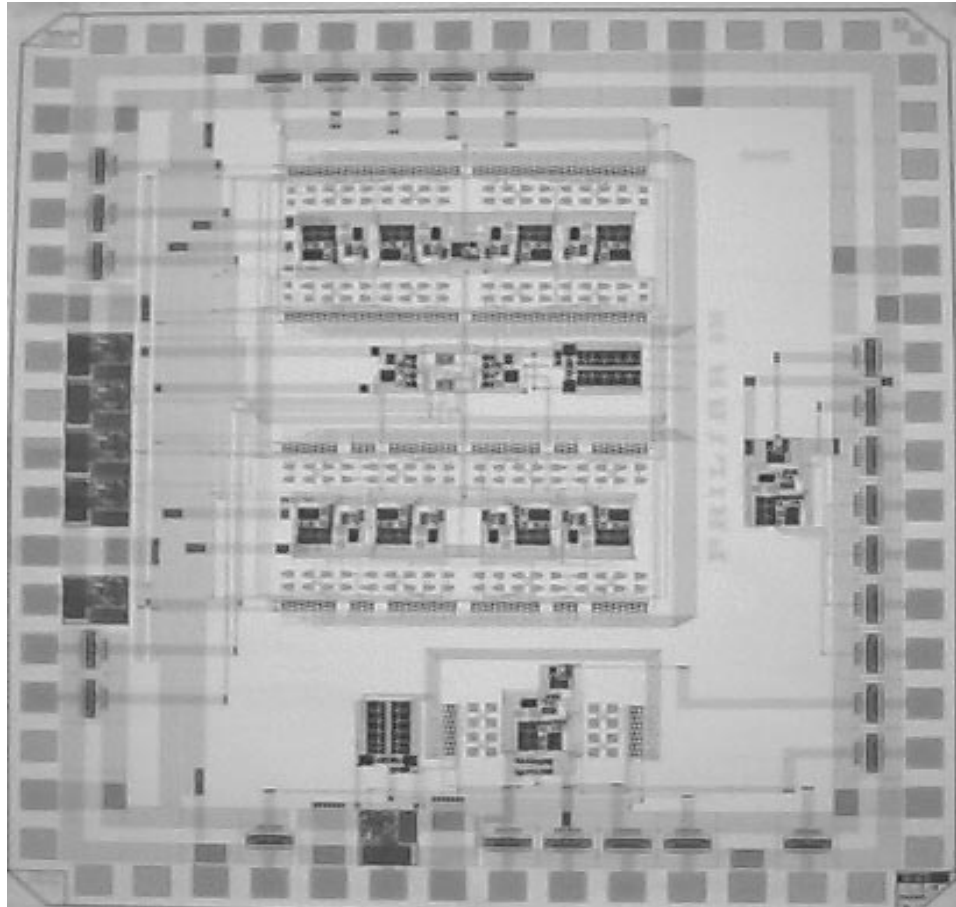
#### Settling Time Test Structure (single ended)



**FIGURE 44. Test Circuits**

From this experimental setup, the measured gain of the opamp was 58dB which is well within the desired range for our modulators [Baz96]. When the settling time was measured, it was found that the clock input (TTL levels) caused excessive ringing on the output, which made accurate settling time measurements impossible. This is due mostly to coupling in the bond wires between the external clock and the output where TTL levels are enough to set up ringing in the circuit. This has the same effect as noise on the circuit and degrades the SNR of the modulator.

The layout of the complete chip including the test structures is shown below in Figure 45 (the layout for Modulator B is almost identical).



**FIGURE 45. Layout of Modulator A**

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### 5.3 *Simulated Performance of the $\Sigma\Delta$ Modulator*

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Now that the performance levels of the circuit elements have been stated, we can now look at the performance of the implemented modulators. Both modulators are designed with the same NTF, so their nominal performance is the same. All the following simulation results can be applied to both Modulator A and Modulator B. Ideal simulations in Simulink [Hic92] show that the maximum SNR is 96dB for a 200kHz BW, for a sampling rate of 80MHz and 0% coefficient mismatch. This is equivalent to an Over-Sampling Ratio (OSR) of 200. The OSR becomes important, because we can predict the increase in SNR per octave. Since the modulator is supposed to have the same performance inband as a 6th-order bandpass  $\Sigma\Delta$ M, or equivalently, a third-order lowpass, we can predict the SNR vs. OSR for a 6th-order bandpass  $\Sigma\Delta$  from [Jan92] to be:

$$SNR_{increase} = (3N + 3)dB/Octave \quad (EQ\ 40)$$

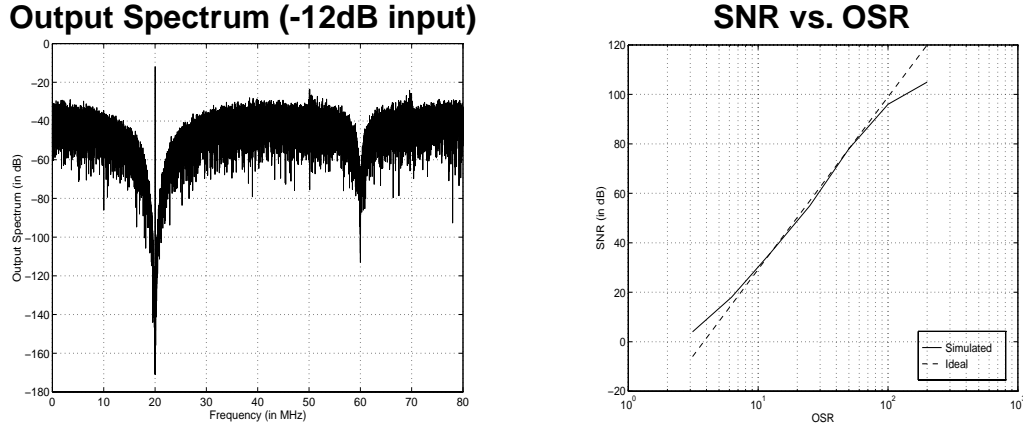
And for N=6,

$$SNR_{increase} = 21dB/Octave \quad (EQ\ 41)$$

The results of this discussion are outlined below in Figure 46. As we can see, the simulated SNR does indeed behave like a sixth-order bandpass  $\Sigma\Delta$  modulator (21 dB/

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Octave of oversampling), and that we can apparently get 16 bits of resolution from this converter.

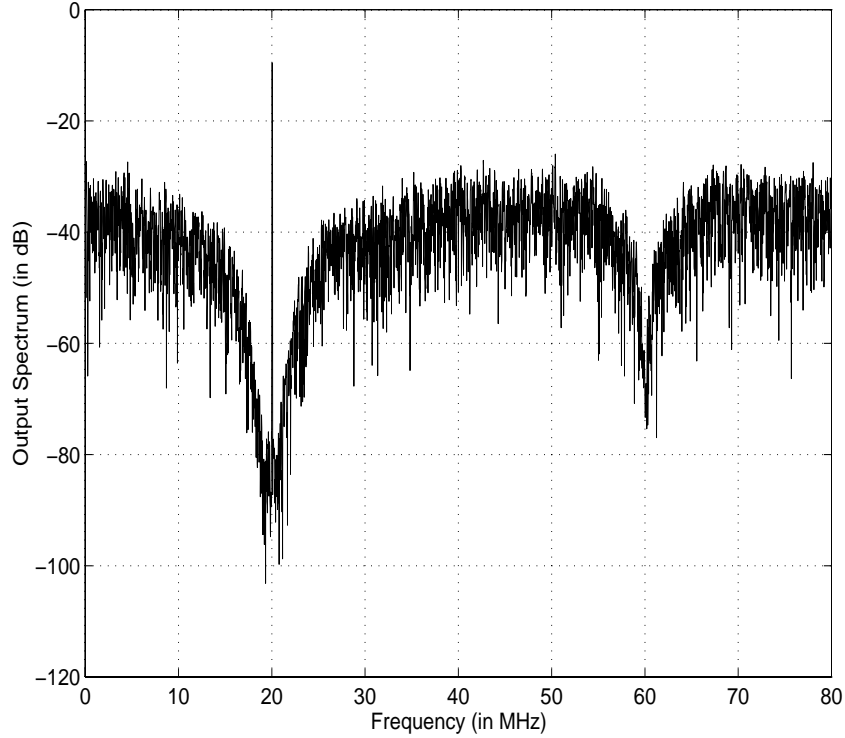


**FIGURE 46. Performance Graphs of 4th-order Complex  $\Sigma\Delta$  Modulator**

In non-ideal simulations in Spectre [Spe96], we get vastly different results. For a 4096 pt. FFT, we find that the maximum SNR for both Modulator A and B, at a sampling rate of 80MHz the SNR is 54dB. We can see this in Figure 47, where the  $\Sigma\Delta$  Modulator output spectrum is plotted for a -9dB input at  $f_s/4$  for  $f_s = 80\text{MHz}$ . It should be noted that the accuracy of these simulations can be called into question due to the accuracy of the simulator and the limited number of points with which to do the FFT. For a sampling rate of 80MHz, and 4096 pts, the frequency width of a bin is 19kHz, which is only about 1/10



of our signal bandwidth! Detailed circuit simulation is very slow and longer runs are of limited value.



**FIGURE 47. Simulated Response (non ideal) of Complex  $\Sigma\Delta$  Modulator**

It is important to note that noise and mismatch were not simulated for the circuits. It was expected that the increased frequency would cause a loss in SNR. The reason for this is primarily opamp settling time. The opamp was designed to only drive a 1pF load. Our architecture, however, had a maximum load of three times the unit capacitors (375 fF) which is 1.125 pF plus the parasitic capacitances of the metal (in some cases, this was on the order of 1000 $\mu$ m long, which could add another 0.2pF). This should be enough to cause a significant loss of SNR. Plus, as was explained above, the high input capacitance of the opamp can cause the capacitive load to be increased. Because of these considerations, it was found to be necessary to operate the modulator at a lower sampling rate ( $f_s = 48\text{MHz}$ ), so that the settling time was no longer a problem.

Another point worth mentioning is that with the small capacitors chosen (between 150fF and 375 fF), kT/C noise can become a concern. For both modulators, the maximum capacitor size used was 375fF for the integrating capacitance. For this size capacitor, the kT/C noise across it is:

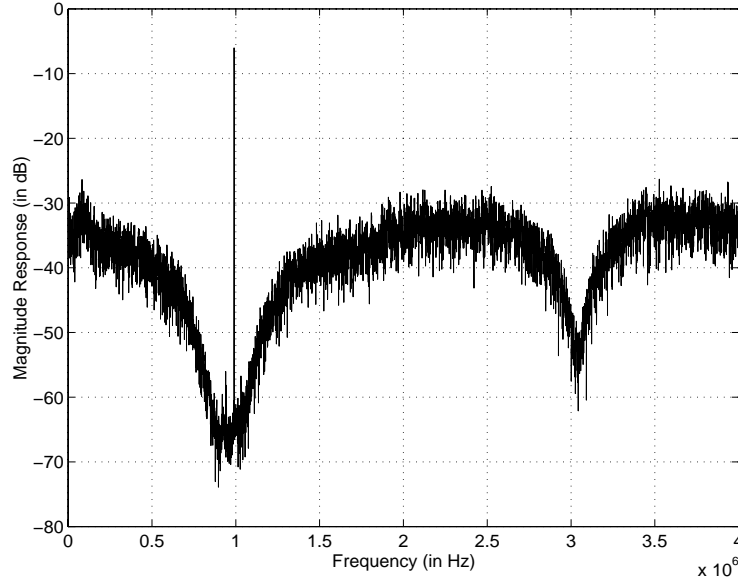
$$\sqrt{\frac{kT}{C}} = \sqrt{\frac{(1.38 \times 10^{-23} \text{ J/K})(300 \text{ K})}{375 \text{ fF}}} = 105 \mu\text{V}_{rms}$$

Referenced to the feedback voltage of 300mV, this is -70dB across the sampling band and for an OSR of 200, -93dB inband, which could in fact be the limiting factor in the performance of this  $\Sigma\Delta$  modulator because there are many capacitors contributing kT/C noise. kT/C noise was also not simulated in the simulations. The solution for this is to increase the capacitor sizes, and decrease the sampling rate. But we still will be able to make use of undersampling, so the reduced clock rate might not be a problem for GSM bandwidths.

#### 5.4 *Experimental Performance of Modulator A*

Modulator A's performance was significantly less than the simulations predicted. Below is the output spectrum (for a 32768 pt. FFT) of the modulator, with a sampling rate of 4 MHz. As we can see, the spectrum in Figure 48 shows a seriously degraded notch with an SNR of only 48dB (for an OSR of 200), as compared with our previous ideal Simulink simulations. At this low sampling rate, settling time concerns become nonexistent.

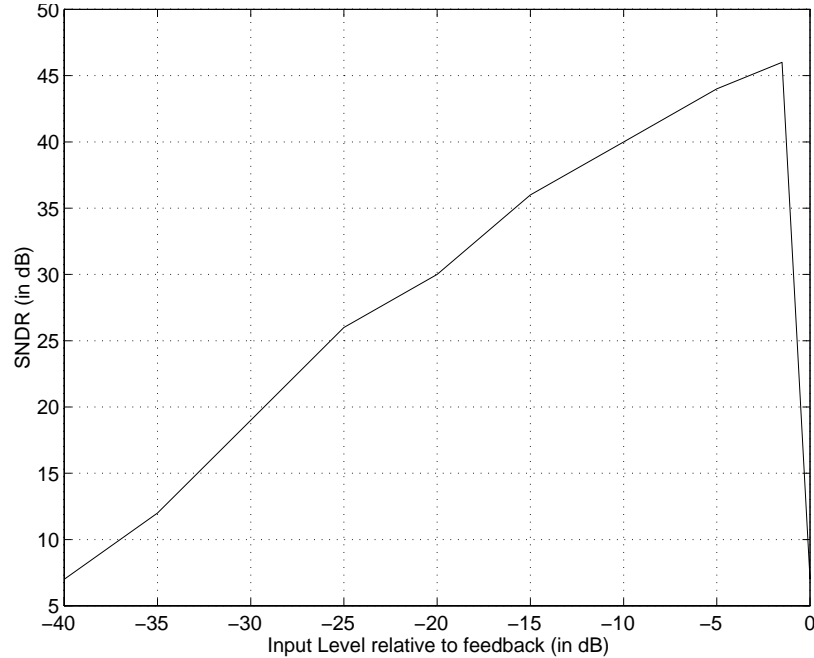
Another factor that could be responsible now is random coefficient mismatches in the modulator. This was already explored in some depth in the previous chapter.



**FIGURE 48. Output Spectrum for Complex Modulator ( $f_s=4$  MHz)**

When we increase the sampling rate to 80MHz, we see decreased performance (as we should expect) due to the settling time of the SC integrators. The maximum SNR is 32dB at  $f_s=80$ MHz vs. an SNR of 48dB at  $f_s=4$ MHz (a discrepancy of 16dB). We can compare this to our simulation results which have an SNR of 49dB at  $f_s=80$ MHz and an SNR of 70dB at  $f_s=10$ MHz (a discrepancy of 21dB). The reason that the experimental discrepancy is better than the simulations is that slightly higher bias currents were used in order to

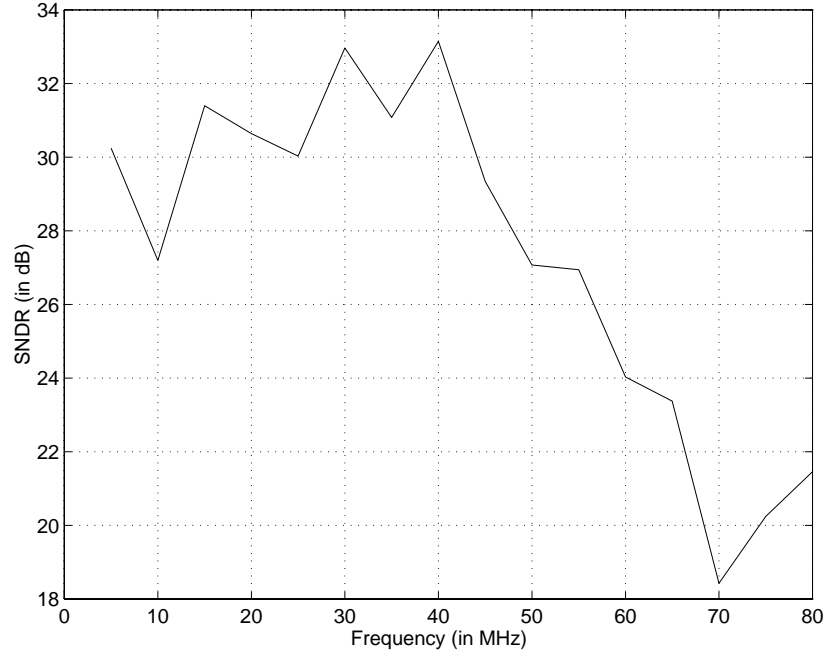
increase opamp output drive, and hence decrease settling time. Below is shown an SNDR vs. Input level graph for the modulator for a sampling rate  $f_s=4\text{MHz}$ .



**FIGURE 49. SNDR vs. Input Level for Complex Modulator ( $f_s = 4\text{MHz}$ )**

We can also plot the effect of sampling frequency on the SNR (for the same OSR). We should see a sharp decrease in SNR as the clock increases above the rate that allows adequate settling. This can be seen in Figure 50, where we have the SNDR vs. sampling rate. The SNDR is lower than we would expect because only an I-channel input was generated for the modulator (which has 3dB less power than equal amplitude I and Q input signals) and because the input used was not full scale. We can see a definite decrease in SNR between low and high frequency operation. The measurements are quite variable, however. One possible reason for this is that due to the clock generator in the circuit, the biases were oscillating (coupling to the clock), which constantly changed the response of

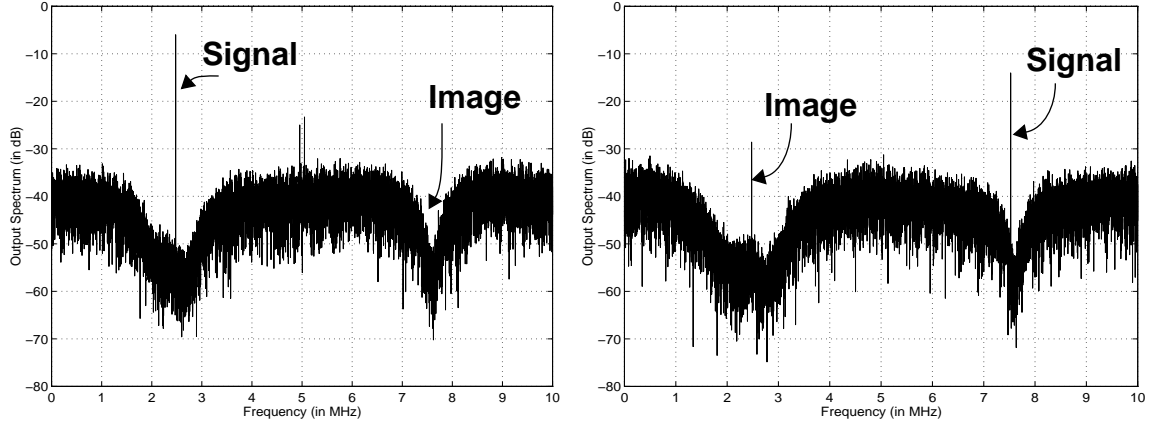
the modulator (notch depth, etc.). This curve suggested the decision to operate the modulator at 48MHz within the complete receiver



**FIGURE 50. SNDR vs. Sampling Frequency for Complex  $\Sigma\Delta$  Modulator (OSR = 200)**

Another important performance metric to look at is the image rejection of the modulator. It was mentioned in Chapter 2 that in any I/Q system, mismatch between the two channels tends to degrade the IR performance of the system (ideally, IR should be infinite). We can measure this by generating a signal at the image frequency, and seeing how much power we have at the signal frequency. Shown below are two measured IR graphs: one with a tone at the desired frequency ( $f_s/4$ ) and the second with a tone at the image frequency ( $3f_s/4$ ). As we can see, the IR is vastly different for both graphs. For the first case (complex tone at  $f_s/4$ ), the measured IR is 41dB, where the IR is the difference between the input tone, and the image tone (also complex at  $3f_s/4$ ). For the input at  $3f_s/4$ , the IR is 14dB! For practical systems, the second IR measurement is what we would consider since we are

more concerned about image power aliasing into our signal rather than signal power aliasing into our image.



**FIGURE 51. Image Rejection (experimental) of the Modulator**

Now the question becomes: why is there such a huge discrepancy (27dB) between both IR measurements? This is due in part to the asymmetric STF. From the previous chapter, we saw that the STF has 6dB gain inband, and -2dB gain for the image. This accounts for some (16dB), but not all the discrepancy that we can see.

To quantify the rest of the error, we can look at [Jan96a] which details precisely the effect of mismatch in complex  $\Sigma\Delta$  modulators. This reference defines a function called the Image Signal Transfer Function (ISTF) which corresponds to the differential error in the STF. This transfer function represents the gain from the input frequency to its corresponding image frequency. A corresponding Image Noise Transfer Function (INTF) also exists for the NTF mismatch error. The STF has an 8dB attenuation between the signal band and the image band, but the ISTF does not necessarily have to have a corresponding 8dB gain between the image band and the signal band. Simulink simulations [Hic92] in Figure 52 show that we get an image rejection of 48dB for an input in the signal band aliasing into the image band and an image rejection of 12dB for an input in the image band aliasing into the signal band, for a difference of 36dB. This simulation

was done for a random sampling of 1% coefficient errors throughout the modulator. This shows that mismatch in the modulator can be responsible for the tremendous difference in image rejection that we have seen. It also reiterates the need for some sort of DSP compensation to improve the IR performance of the modulator [Li96].

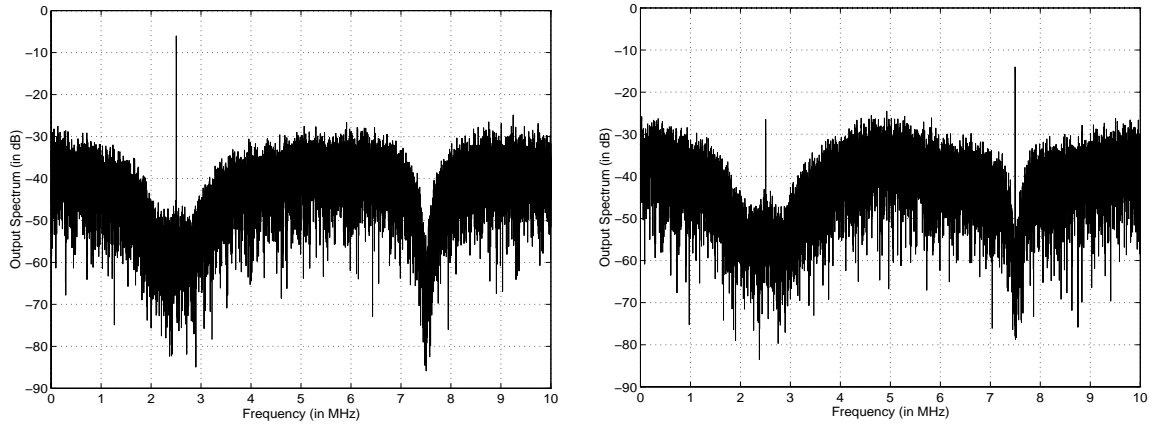


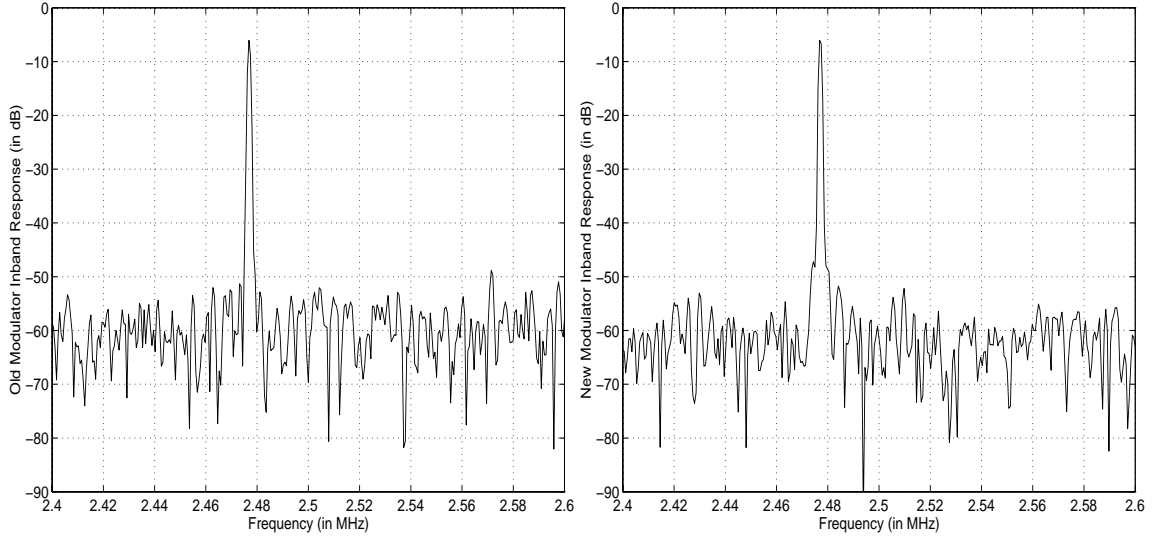
FIGURE 52. Image Rejection (simulated) of the Ideal Modulator for random 1% mismatches

## 5.5 *Experimental Performance of Modulator B*

We saw in the previous section that the performance of Modulator A was quite a bit poorer than what simulations predicted. In Chapter 4, we showed that coefficient mismatch could be the cause of this SNR degradation. Because of this, the improved modulator outlined in the previous chapter was built and tested to see if this was the case.

The experimental results for this new modulator are shown below (Figure 53) in comparison to the old modulator. For an accurate comparison, the inputs were scaled to compensate for the STF gain difference, both modulators were run on the same test board

with the same bias currents and voltages, and the sampling rate for both modulators was  $f_s=10\text{MHz}$  (for a 16384 pt. FFT).



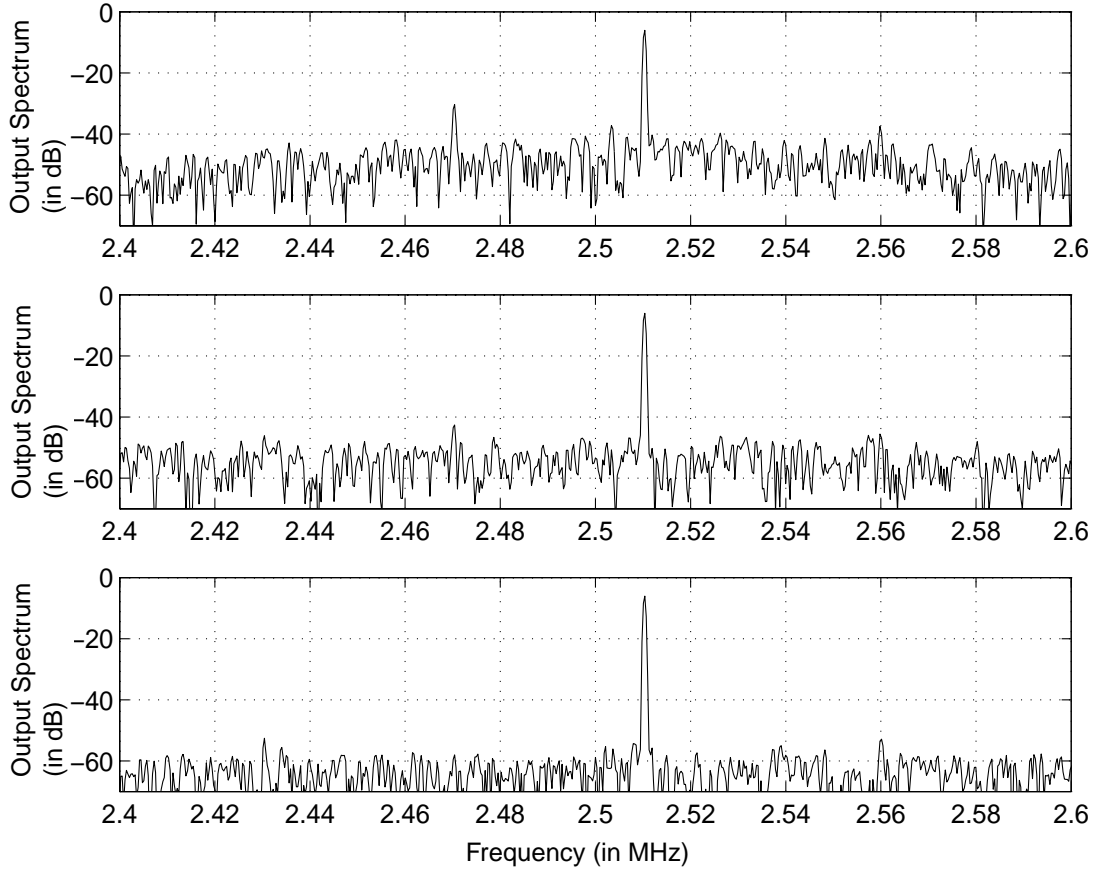
**FIGURE 53. Spectrum Comparison of Old Modulator vs. New Modulator**

Comparing the SNR between the old and new modulators gives us 29dB and 31dB respectively. This is nowhere near to the 35dB improvement that was predicted. This is most likely due to circuit noise. We already found out that the  $kT/C$  noise for the largest capacitor in this modulator is -93dB over the signal band. It is possible that the input referred noise from all the capacitors in the circuit is responsible for part of the performance loss, but it could also be due to many other sources of noise (eg. ringing in the circuit from the clock, etc.).

We can do a test to see if this is in fact the reason for the poor performance of the new modulator. We know that circuit noise ( $kT/C$  or otherwise) is constant, regardless of the reference voltages used in the circuit whereas quantization noise should scale with the references. So, if we were to reduce our  $\Sigma\Delta$  Modulator input and reference voltages by the same amount (same input relative to full scale) and the noise is constant, we should notice a rise in the noise floor of the modulator. Shown below in Figure 54 is a comparison of the



inband spectra for the new modulator for an input of -6dB full scale, an  $f_s$  of 10MHz and feedback reference voltages of 50mV, 100mV and 300mV respectively (for a 16384 pt. FFT and  $f_s=10\text{MHz}$ ).



**FIGURE 54. Comparison of Inband Spectra (Modulator B) after Scaling Reference Voltages**

Increasing the reference voltage by 6dB and 10dB respectively (from upper to lower decreases the noise floor by a corresponding 6dB and 10dB. This helps to confirm the suspicion that circuit noise is responsible for performance degradation in the improved modulator. We should also perform this test on the old version of the modulator to see which is more dominant: mismatch or noise. The results for this are shown below for the same inputs and same test board as the previous figure. Basically we get the same results

for both the old and new versions of the modulator. Therefore, we can say that the main reason for the performance degradation in each case is circuit noise.

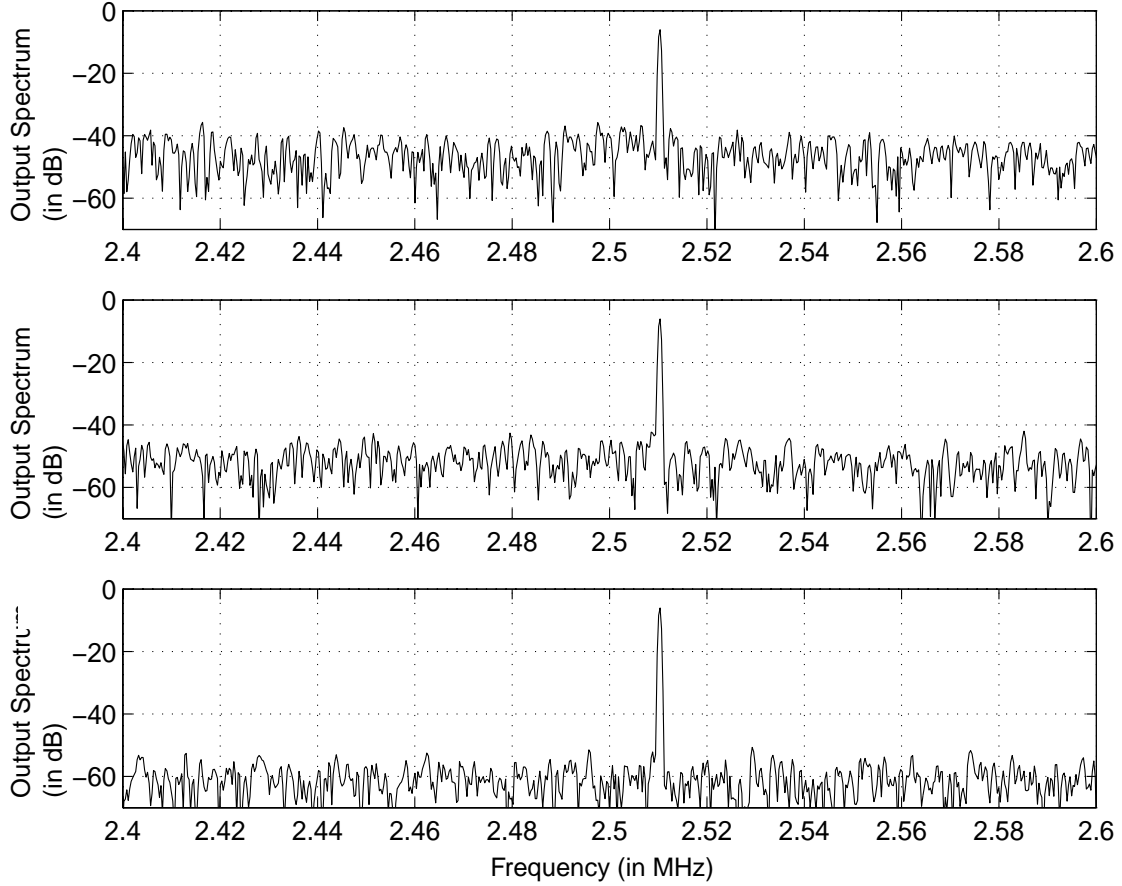


FIGURE 55. Comparison of Spectra (Modulator B) after Scaling Reference Voltages

## 5.6 Summary

In this section, we have presented experimental results for two fourth-order complex  $\Sigma\Delta$  modulators, which were realized in a  $0.8\mu\text{m}$  BiCMOS process. The SNR for an OSR of 200 for both modulators is 48dB (8 bits) at a sampling rate of 4MHz and begins to fall off beyond a 45MHz sampling rate.

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The loss of around 22dB of SNR between experimental and simulated performance was also explained. This was found to be due to circuit noise rather than mismatch within the modulator. The reason for this was partly that extremely small capacitors were used in order to increase the operating speed of the modulator. Also, bias voltages were ringing due to coupling with the clock. But mismatch can still dominate if large capacitors are chosen.

The bottom line is that we have proven that a complex  $\Sigma\Delta$  modulator can be built, but there are issues that need to be resolved in order to increase the resolution and make this a viable alternative to typical bandpass architectures.

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## CHAPTER 6

# *The Complex IF Receiver*

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*“Human beings, who are almost unique in having the ability to learn from the experience of others, are also remarkable for their apparent disinclination to do so.”*

*- Douglas Adams*

Now that the complex  $\Sigma\Delta$ M has been developed, it is important to test it within a radio receiver. After all, it does not make much sense to develop a new A/D converter if it has no practical application. Here we present results for a sample front end suitable for a complex  $\Sigma\Delta$ M, as well as results for GMSK transmitted through the receiver setup.

### *6.1 The Single-IF Architecture Revisited*

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We proposed a Single-IF Receiver architecture front end back in Figure 10 which contains a minimum component count needed to give us the required performance. Basically speaking, the receiver can be divided into three parts: the analog front-end, the complex  $\Sigma\Delta$  modulator, and the decimation filter. This is seen in Figure 56, where we have also specified the processes that each part of a prototype was fabricated in. This doesn't show

the demodulator, data detector, clock recovery, etc. This is all assumed to be after the decimation in DSP.

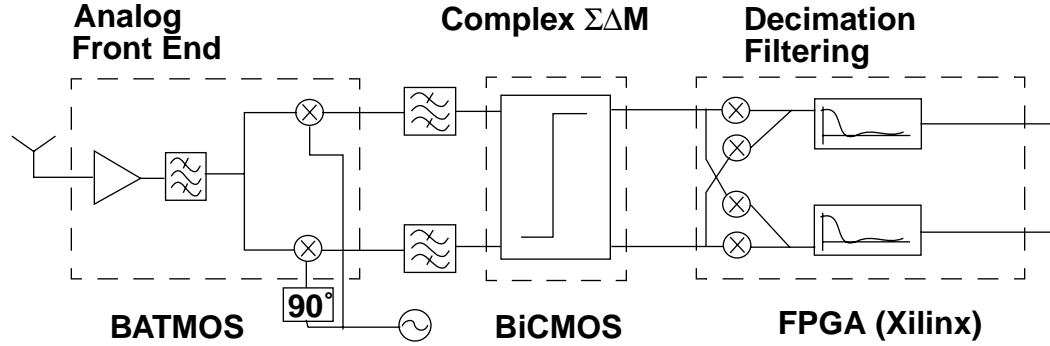


FIGURE 56. Single-IF Receiver Architecture Revisited

In this receiver, we have shown the analog front end and the complex  $\Sigma\Delta$  as two separate monolithic implementations and the filters coupling them as discrete bandpass anti-alias IF filters.

It is important to discuss the ‘fit’ of the complex  $\Sigma\Delta$  into the receiver. The filter in the front end is the image reject filter, so it should be able to significantly attenuate images which are  $2*f_{IF}$  away from  $f_{RF}$ . The value for  $f_{IF}$  is controlled by the  $\Sigma\Delta$ ; we designed it to have a passband at  $f_s/4$ , where  $f_s$  is the sampling rate of the modulator, which makes  $f_{IF}=f_s/4$ .

The trade-off is that the smaller we make  $f_s$ , the easier it is for the  $\Sigma\Delta$  modulator to work, but the smaller  $f_{IF}$  becomes, the more selective the image reject filter and the discrete anti-alias filters become. We can cheat this tradeoff to a degree by undersampling the signal so that  $f_s < f_{IF}$ . This helps the image reject filter, but the requirements on the anti-alias filters are still the same. If, for example, we want an  $f_{IF}$  of 60MHz and do not undersample,  $f_s=4*f_{IF}=240$ MHz for our modulator. We could also make  $f_s=48$ MHz for which the first

passband alias is at  $f_{IF} = 5 \cdot f_s / 4 = 60\text{MHz}$ ). This helps us resolve our need for a high IF with the limit in speed of the  $\Sigma\Delta$  modulator.

## 6.2 *Analog Front-End*

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The analog front end consists of a monolithic LNA [Lon95], Notch Filter [Mac96], and Quadrature Mixer. These were all implemented by Macedo [Mac97] in a  $0.8\mu\text{m}$  BiCMOS process with on-chip inductors. Each of these components are discussed below.

The LNA is a tuned amplifier with an on-chip resonant LC tank. [Lon95] presents a schematic for an LNA using a transformer. The LNA that was implemented for this receiver, however, uses two separate inductors for the LC tank and the degeneration. Simulated results were similar to the LNA in [Lon95]. These results for the LNA from [Lon95] are presented in Table 5

**TABLE 5. LNA Performance Specs (simulated)**

LNA Parameter	Value
Vcc (in V)	3
RF (in GHz)	1.9
Pd (in mW)	6
Gain (in dB)	10
NF (in dB)	2.7

The notch filter has already been described in [Mac96]. It consists of a series LC resonator, cascoded with an on-chip LC tank. The LC tank is tuned to the passband frequency (in this case,  $1.9\text{GHz}$ ), and the series LC resonator is tuned to the image frequency to create the notch. At this frequency (nominally  $2.5\text{GHz}$ ), the input stage sees zero impedance to ground, which results in zero gain at the output. The important specifications for this filter are outlined below. It is important to note now that the notch of

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this filter is designed at 2.5GHz (an IF of 300MHz for an RF of 1.9GHz). This is far too high for our present setup, where we've been assuming an IF of 60MHz because the anti alias filters are only rated for a 60MHz IF. With better filter technology (ie. a SAW filter), we could get bandpass anti alias filters at 300MHz which would be more ideal. This tells us that future work needs to be done to increase the speed of the modulator so it works at a higher IF, undersample the IF signal, or increase the performance of the filter so that the notch appears at a much lower frequency.

**TABLE 6. Notch Filter Performance Specs (experimental)**

Filter Parameter	Value
Gain (1.8GHz)	12dB
NF (1.8GHz)	11.4dB
Input IP3	-7.8dBm
Notch Tuning (@ 2.52GHz)	$\pm 120\text{MHz}$
Pd (in mW)	9.6
Vcc (in V)	3

The quadrature mixer was simply a pair of Gilbert Cells [Gre84], one for each channel. In order to increase the input dynamic range, degeneration resistors were added to the lower transistors (the RF input). There are other ways to build a mixer, for instance, one could use a transformer balun instead of the RF emitter-degenerated differential pair [Lon95]. The balun has the effect of doing a single-ended to differential conversion on the RF, which is then fed to the LO switching transistors. This is currently under investigation as a possible means of decreasing NF in a monolithic Analog Front-End [Mac97]. The performance specs on the mixer are outlined below.

**TABLE 7. Mixer Performance Specs (experimental)**

Mixer Parameter	Value
Vcc (in V)	3
RF (in GHz)	1.9
LO (in GHz)	2.2

**TABLE 7. Mixer Performance Specs (experimental)**

Conversion Gain (in dB)	8.5
NF (in dB)	16

Once these circuits are placed in a complete receiver, we can measure the total performance (i.e. NF, input IP3, etc.) for the entire system. This performance is different from what we would expect from the previous tables because a fully integrated solution does not have  $50\Omega$  terminations for each component's input and output. This is summarized below in Table 8 for a 1.9GHz RF, and 2.2GHz LO.

**TABLE 8. Complete Receiver Specs (single mixer, experimental)**

Receiver Parameter	Value
Vcc (in V)	3
Pd (in mW)	48
NF (in dB)	9.4
Input IP3 (in dBm)	-20
Image Rejection (in dB)	50
Image Rejection tuning (in MHz)	200 (from 2.4GHz - 2.6GHz)

### 6.3 Complex $\Sigma\Delta$ Modulator

The Complex  $\Sigma\Delta$  Modulator was already presented in Chapters 3 and 4. The important parameters that we need to know for designing this radio receiver are summarized below.

**TABLE 9. Complex  $\Sigma\Delta$  Modulator Specs for Receiver Design**

$\Sigma\Delta$ Parameter	Value
Vdd	5V
Pd (in mW, $f_s=4\text{MHz}$ )	150
SNR ( $f_s=4\text{MHz}$ )	48dB
$\Sigma\Delta$ Gain	6dB



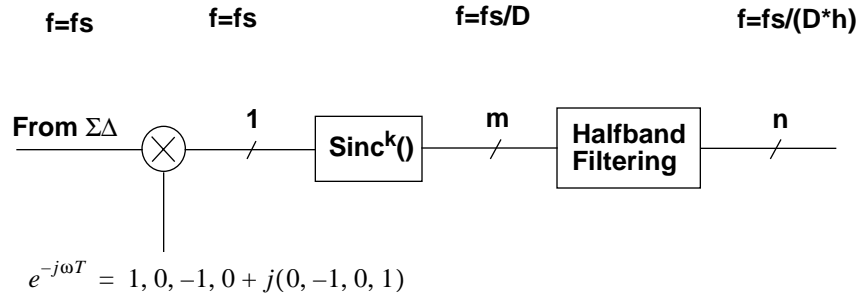
TABLE 9. Complex  $\Sigma\Delta$  Modulator Specs for Receiver Design

Max. Input	300mV p-p
$\Sigma\Delta$ Dynamic Range	52 dB

For this modulator, it was already stated that the opamp gain was found experimentally to be 58dB.

## 6.4 Decimation Filtering

To make a  $\Sigma\Delta$  modulator look like a normal n-bit A/D converter, a decimation filter is needed to convert the oversampled output of the A/D (which is 1-bit, in our case) into n-bit words at the Nyquist rate (two times the BW). Decimation filtering for  $\Sigma\Delta$  Modulators has already been explored in current literature for lowpass modulators [Can92] [Chu84] [Fri89], and bandpass modulators [Sch90b]. The accepted approach for decimating normal bandpass modulators is to do a complex mix on the  $\Sigma\Delta$  bitstream, then do lowpass filtering ( $\text{sinc}^k$  or halfband) to extract the signal. This is shown below, where we have shown all the stages of decimation, along with the corresponding decrease in sampling rate.

FIGURE 57. Decimation for Bandpass  $\Sigma\Delta$  Modulators

For the real-valued BP $\Sigma\Delta$ M, the one-sided complex mix produces two bitstreams for processing from the  $\Sigma\Delta$  output (I and Q). In our case, we have a complex  $\Sigma\Delta$  modulator,

which has a complex bitstream to begin with. This just makes the complex mix a little more complicated, since we are now multiplying two complex numbers together. We can do a comparison of the effect complex mixing has on a real-valued and a complex  $\Sigma\Delta$  modulator (see Figure 58). We can see that for the complex  $\Sigma\Delta$  modulator, each channel contains twice as much information as the I/Q outputs of the real  $\Sigma\Delta$  modulator. This makes sense, because our complex modulator is comparable to having two real modulators digitizing the I and Q channels separately.

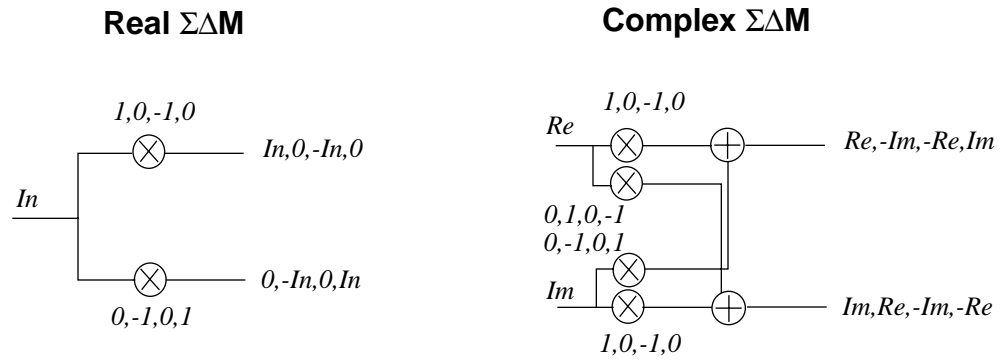


FIGURE 58. Digital I/Q Mixer for Real & Complex  $\Sigma\Delta$  Modulators

When decimating a  $\Sigma\Delta$  bitstream, typically one uses two or more stages. First, a  $\text{sinc}^k()$  is used to decimate the bitstream to a more manageable rate, then more complicated filtering can be performed at this slower rate (such as halfband filtering, etc.) for increased resolution. The order of the sinc filter ( $k$ ) controls the rolloff of the filter, but more importantly than that, it controls the amount of noise power that is aliased inband, due to the sinc sidelobes. Obviously, the higher the order of  $\Sigma\Delta$  Modulator, the deeper the inband noise notch, so the less noise we want aliased inband.

We are only concerned here with two-rate sinc decimators. Multi-rate solutions are presented in [Chu84], however, which demonstrate increased performance over the conventional decimators. A general guideline to follow in decimator filter design is that the order of the filter should be at least one greater than the number of zeros in the NTF

passband in order to avoid degrading the notch. For a 4th order bandpass  $\Sigma\Delta$  modulator, there are two NTF zeros in the passband, which means the sinc decimator should be third order. In our case, we have three zeros in the passband, which means our sinc decimator should be fourth order. An analysis of this class of filters is presented in [Hog81] which shows the aliased noise power with respect to the order of the filter and the relative bandwidth with respect to the low sampling (decimated) rate. The relative bandwidth is related to the OSR in the following:

$$OSR \approx \frac{D}{RBW} \quad (\text{EQ 42})$$

Where D is the decimation ratio and RBW is the relative bandwidth. Table 10 shows the aliased noise power with respect to RBW and the order of the decimation filter.

**TABLE 10. Aliasing Attenuation vs. Filter Order & Signal Bandwidth (from [Hog81])**

Relative BW	Image Aliasing vs. N & Signal Bandwidth (in dB)					
	1	2	3	4	5	6
1/128	42.1	84.2	126.2	168.3	210.4	252.5
1/64	36.0	72.0	108.0	144.0	180.0	215.9
1/32	29.8	59.7	89.5	119.4	149.2	179.0
1/16	23.6	47.2	70.7	94.3	117.9	141.5
1/8	17.1	34.3	51.4	68.5	85.6	102.8
1/4	10.5	20.9	31.4	41.8	52.3	62.7

For our modulator, we already stated that the maximum SNR was 48dB. This means that for this modulator, we should usually use at least a fourth-order decimator with a relative bandwidth of 1/8 to prevent noise aliasing from degrading the performance of the modulator. For a relative BW of 1/8 and an OSR of 200, our decimated rate can be calculated to be approximately  $f_s/32$ . However, in order to implement this decimator on an FPGA with limited space, we choose to use a 3rd order filter with a decimated rate of  $f_s/$

64. This doesn't give us maximum performance, but it is good enough for us to demonstrate the functionality of this receiver.

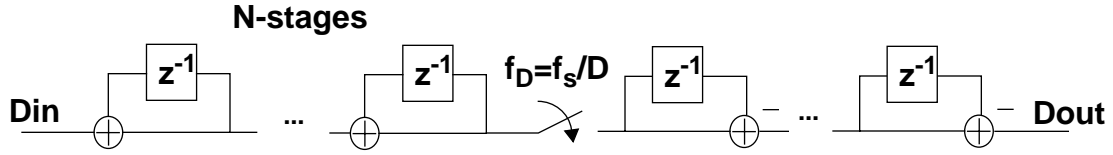


FIGURE 59. CIC Decimator for  $\Sigma\Delta$  Modulators

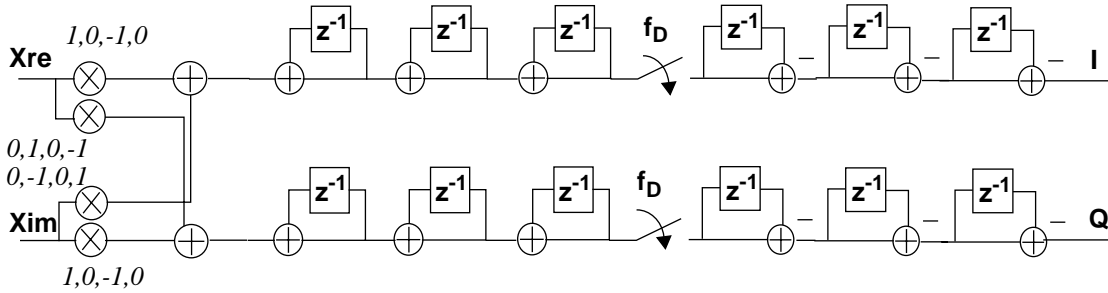
This decimator can be implemented very simply as a sequence of accumulators and decimators (see Figure 59), otherwise known as a Cascaded Integrator-Comb (CIC) structure. Here,  $f_D$  is the slow (decimated) rate that was mentioned above,  $D_{in}$  is the output from our modulator,  $D_{out}$  is our  $n$ -bit word and  $f_s$  is the sampling frequency of the  $\Sigma\Delta$  Modulator. Care has to be taken in the design of these stages to ensure that there are enough bits of resolution so that carry overflow (using two's-complement arithmetic) from the accumulators does not matter. This is discussed in Hogenauer's paper [Hog81] where he states that the required resolution in the CIC filter is:

$$B_{max} = \lceil N \log_2 R \rceil + Bin - 1$$

where  $Bin$  is the length of the input word (1 for the case of a 2-level  $\Sigma\Delta$  Modulator),  $N$  is the number of stages of the CIC filter, and  $R$  is the decimation ratio. So, if we were to design a filter with the previous requirements ( $R=64$ ,  $N=3$ ,  $Bin=1$ ), the maximum resolution of the CIC filter becomes 18 bits.

This third-order CIC decimator was first implemented with C code (see Appendix B), then implemented on a Xilinx FPGA for the Complex  $\Sigma\Delta$  Modulator (see below). For this

setup, the decimation rate was 64, so the maximum resolution needed for the filter was 18 bits.



**FIGURE 60. Complex Decimation Filter Implemented on Xilinx FPGA**

This filter was implemented directly by building an 18-bit accumulator and differentiator. This, unfortunately, is an inherently low-speed implementation (<5 MHz) when put on a gate array, which typically has blocks that contain two registers and enough logic to implement an adder. So, it makes more sense, from a speed point of view to implement the accumulator and differentiator as a cascade of 2-bit structures for speed. A CIC filter with 4-bit accumulators and differentiators is outlined in [Hog81]. On the Xilinx 3000 series FPGA, speeds of 20MHz have been reported with this type of structure. However, because the sampling rate of the modulator was  $f_s=48\text{MHz}$ , real-time decimation with the Xilinx decimator was not used.

## 6.5 Receiver Performance

Initially, functional tests were performed on the front-end (including the discrete anti-alias filters of Figure 56) to determine total power dissipation, and most importantly, phase error between the I and Q channels. The front-end consumed 100mW from a 3V supply, and also had a best-case phase error between IF I and Q channels of  $9^\circ$  (including discrete

anti alias filters after the front-end). The RF for this prototype was 1.9 GHz with a 60 MHz IF.

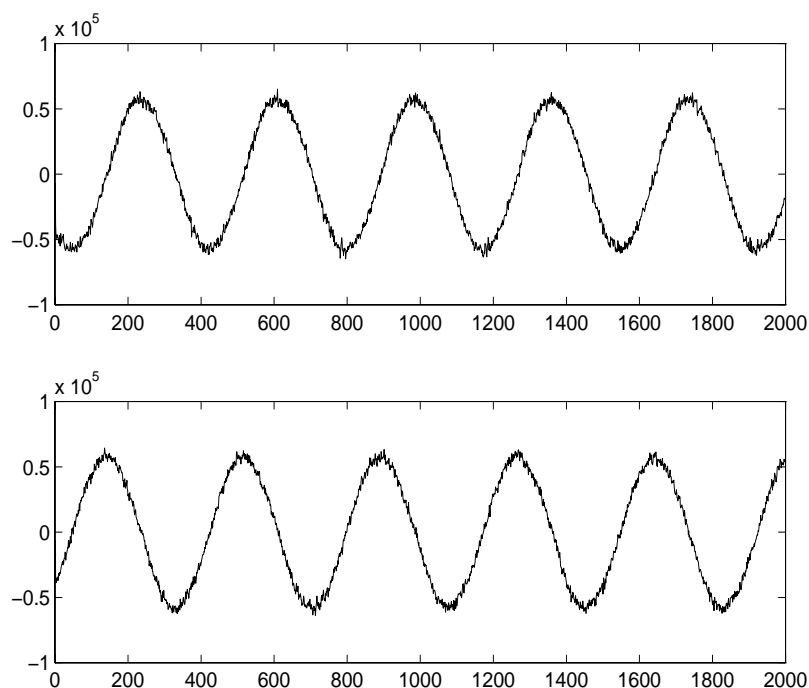
Upon later examination, it was found that there was 211 $\mu$ m of excess metal between the LO I and Q inputs. At 1.9 GHz, this was calculated to give approximately 2° of phase lag between them. Just due to component mismatch, we can get a phase error of up to 3° [Cro95]. Finally, there is also an error introduced by the wirebonds between the LO I and Q inputs. One input has 1nH more inductance than the other due to a longer wirebond. From a 50 $\Omega$  source, this is sufficient to give a phase error of 9° at 1.9GHz! The anti alias filters also have an error of 5° at an IF of 60MHz. So, the phase error we could get would be 19°. For such a large phase error, most of the mismatch tests that we could perform would be due to this error, and not mismatch within the modulator. These errors are all stable though, and in principle could be corrected in DSP.

For the complete receiver, the following parameters were used. This was meant to effectively simulate GSM communication at a slightly higher RF. The reason a 100 kbit/s data rate was used instead of the GSM standard 270.833 kbit/s was that the modulator's clock rate was lower than the desired 80MHz (the decimated rate is only 750kHz).

**TABLE 11. Receiver Parameters**

Parameter	Value
RF	1.9 GHz
RF power	-23 dBm
LO	1.96 GHz
LO power	+5 dBm
$f_s$	48 MHz
Modulation Scheme	GMSK
Data rate	100 kbit/s
Decimated rate	750 kHz
BT	0.3

Initially, a tone was placed at a 2kHz positive offset from the 1.9 GHz carrier to verify the functionality of the receiver. This isn't very interesting from a communications point of view, but it does help verify that the receiver is actually working. The output for this is shown below in Figure 61. As expected, the Q channel leads the I channel by  $90^\circ$ . This is because the complex input, when mixed down to baseband, appears at a frequency of -2kHz ( $\cos\{2\text{kHz}\}$  and  $-\sin\{2\text{kHz}\}$ ).

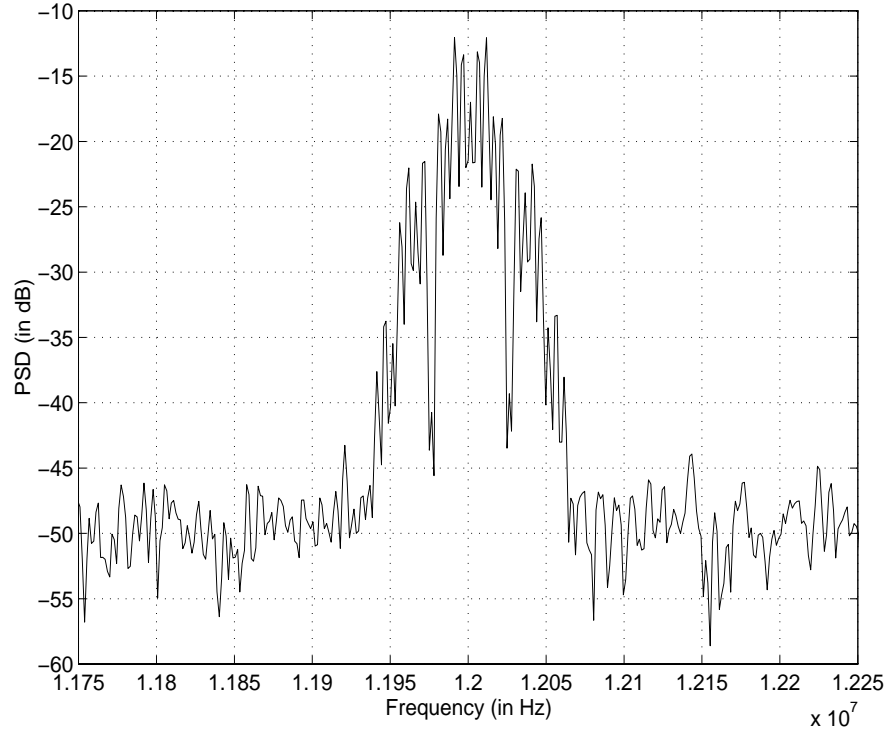


**FIGURE 61. Performance of receiver, -30 dBm input tone**

It also interesting to note that there is no phase or amplitude error in the demodulated output. This is to be expected, since phase and amplitude errors in a signal transfer power to the image frequency. The image frequency is filtered off by DSP and all we are left with is the desired signal with no phase or amplitude error. Without any interferers at the image frequency, this response is precisely what we would expect.

For GMSK, we can do a comparison of the simulated eye diagrams and the experimental eye diagrams for pseudo random data. Figure 62 shows the output spectrum of the

modulator inband. We can see that this has the general shape of transmitted GMSK for a data rate of 100kHz.

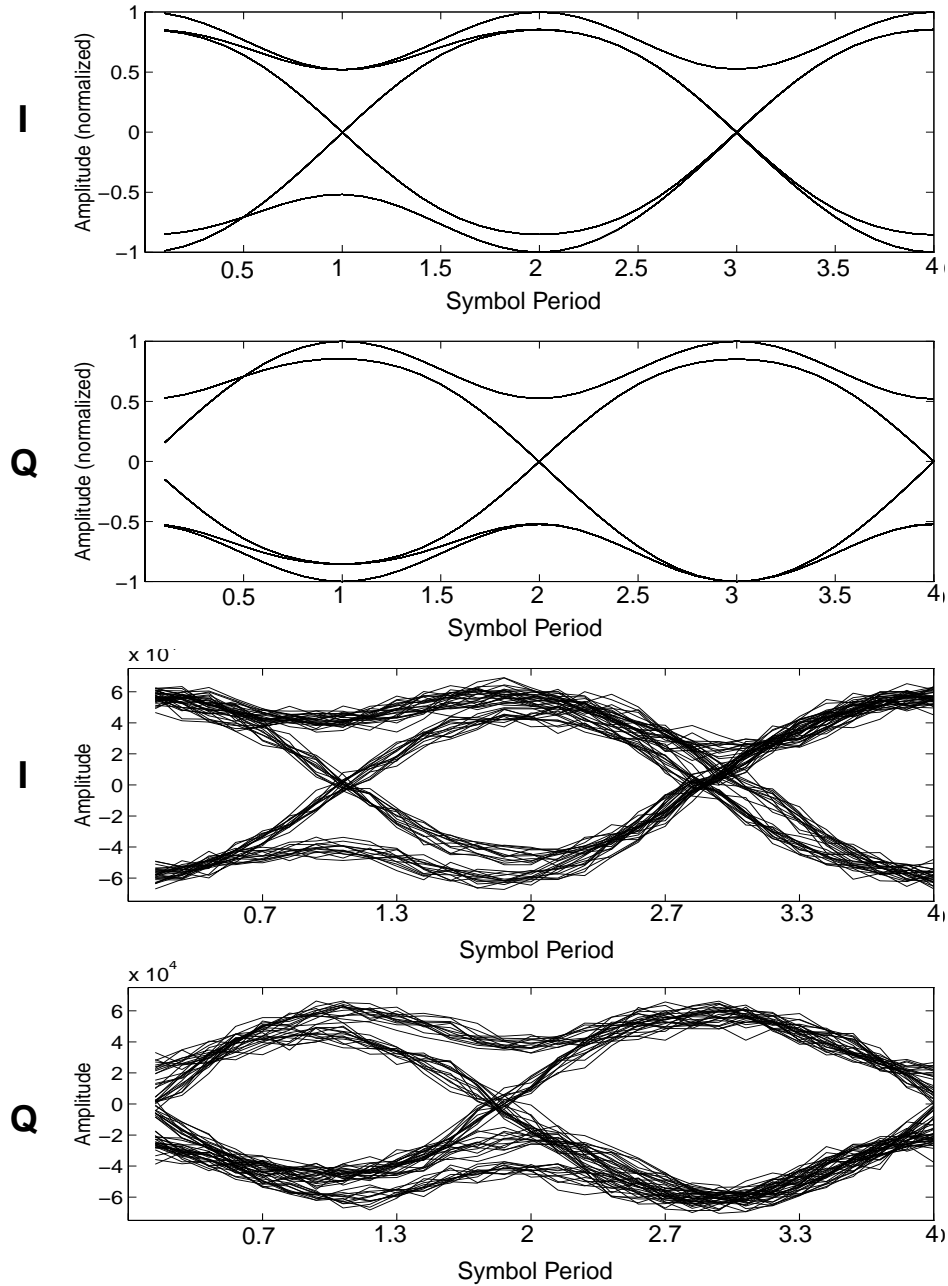


**FIGURE 62. Spectra of Ideal GMSK and  $\Sigma\Delta$  Modulator output**

Figure 63 shows a comparison between the simulated and experimental eye diagrams for the same pseudo-random data. The bit sequence was only 20 bits, due to equipment limitations. We can see that the experimental and simulated results agree with each other. The eye diagrams for the experimental results appear to have some high frequency noise



on top of the signal. This is residual quantization noise and can be partly filtered out (as was mentioned before) by a half-band filter in DSP.



**FIGURE 63. Eye Diagrams for receiver - Simulated and Experimental**

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For our chosen  $BT=0.3$ , the eye opening is fairly well defined for a -12dB input. Appendix C shows the responses for other selected GMSK inputs. In these, we can also see that the eye opening is what simulations predicted.

## 6.6 *Summary*

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We have presented a two-chip solution for a radio receiver using a complex  $\Sigma\Delta$  modulator. Both these chips were fabricated on 0.8 $\mu$ m BiCMOS processes albeit from different foundries.

We have shown that while the performance of each prototype chip has problems (circuit noise in the complex  $\Sigma\Delta$  modulator, phase error with the analog front-end), we can still demodulate a GMSK input at an RF of 1.9 GHz. So, this receiver is feasible for GSM and DCS-1800, if the performance levels of the individual components are improved.

Currently, a new version of the analog front-end is in fabrication which corrects this phase error problem. As well as this, a new complex SD modulator has been reported [Jan97] which claims an SNR of 66dB. This is a demonstration that the 11-bit requirement we needed from an A/D converter back in chapter 2 is practical.

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*“Imagination is more important than knowledge.”*

- Albert Einstein

This chapter contains a summary of the work that was presented in this thesis, plus some conclusions that we can draw about it. After this, directions for future work are suggested.

### **7.1     *Summary***

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The main objective of this thesis was to present the experimental results of the first monolithic Complex Bandpass  $\Sigma\Delta$  Modulator. To a lesser extent, the secondary objective was to show a prototype of a two-chip radio receiver using this complex  $\Sigma\Delta$  modulator to digitize the input.

In Chapter 2, we did a comparison of some different receiver architectures that are currently being used for PCS, each of which has its own shortcomings. The single-IF receiver was discussed, and its advantages were highlighted as compared to dual IF and direct conversion receivers. Some typical specifications for GSM receivers were presented, and it was decided that these would be good guidelines to design for (e.g. 200kHz bandwidth, GMSK modulation).

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Chapter 3 dealt with the theory and prior art of a complex  $\Sigma\Delta$  modulator. The NTF and STF were derived for two sample modulators, and it was found that we get roughly double the improvement in bandwidth over the same order bandpass  $\Sigma\Delta$  modulator. In reality, it turns out that mismatch in the modulator can degrade the performance significantly. It was predicted based on previous literature that with careful design of the  $\Sigma\Delta$  architecture, this performance degradation could be minimized. Alternatively, by knowing the exact value of this mismatch error, it could be compensated for in DSP.

In Chapter 4, we dealt with the design of two modulators. Each was based on a delay-cell architecture for speed. The innovative nature of the first modulator attempted was that the coefficient ratios were simple and a maximum of 2.5:1, making it ideal for a high-speed architecture. The coefficients were also purely real or imaginary, reducing the complexity by a factor of 2. The second modulator was an attempt to control the mismatch sensitivity that was found to be present in the first modulator.

In Chapter 5, we presented experimental results for both modulators. It turned out that the maximum SNR achieved for an OSR of 200 was 48dB (equivalent to 8 bits) for both modulators. It was also determined that the main cause for this error was to circuit noise. A test was performed where the references and inputs were scaled down and it was found that the noise floor inband increased by a corresponding amount. Since noise doesn't scale with the references and inputs, it's safe to say that some noise is degrading the quality of the  $\Sigma\Delta$  Modulator. Since small capacitors were used, it's safe to say that they could result in noise, but there are also noise contributions from the clocks and opamps. A method was also presented for compensating for any mismatch in a complex  $\Sigma\Delta$  modulator by using adaptive DSP.

Finally, an entire receiver was built and tested using this complex  $\Sigma\Delta$  modulator. The receiver performance is outlined in Chapter 6. Tests were performed assuming that the receiver was going to be used for a GSM-like standard. This involved transmitting GMSK

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data at a bit rate of 100 kbits/s and a BT for the gaussian filter of 0.3. The tests showed that the receiver was able to demodulate this reasonably accurately.

## 7.2 *Conclusions*

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The modulator was designed to be a high speed architecture, and was able to perform at half its intended clock rate with little performance degradation. The fact that it worked tells us that it is feasible to use this modulator in a receiver. Currently, another complex  $\Sigma\Delta$  modulator has been reported [Jan97] which claims to get more significant performance (11-bit vs. our 8-bit) at a lower clock rate but for one quarter of the OSR. This proves that the complex  $\Sigma\Delta$  modulator can be designed to meet target specifications for PCS.

As far as the receiver goes, the SNR performance is not good enough due to the resolution of the modulator and the phase error in the front-end, but the thrust of this work was to show that it is possible to integrate a complex  $\Sigma\Delta$  modulator into a radio receiver.

## 7.3 *Future Work*

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More work needs to be done in the area of complex  $\Sigma\Delta$  modulators before they can be integrated into a receiver for production purposes. Some areas that can be explored are:

### ***High-Speed Continuous Time Complex $\Sigma\Delta$ Modulators.***

This thesis dealt with implementing a switched C modulator. The limitations for this tend to be that the maximum clock rate achievable in a typical 0.8 $\mu$ m BiCMOS process is on the order of 60-80MHz. Clocking at higher speeds means that we can have a higher IF, which puts less demand on the front-end filter to knock down the power in an image. Results have been reported for  $g_m$ -C  $\Sigma\Delta$  Modulators at 3.2GHz in a fast process (Indium

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Phosphide) [Jen95]. Research is also being done into Bandpass  $\Sigma\Delta$  Modulators with on-chip LC tank circuits operating at RF frequencies [Gao97]. Continuous time Modulators could also be designed to be tunable over a large range. This is especially good for complex  $\Sigma\Delta$  modulators, where the complex notch in the NTF can be continuously tuned over a wide range of frequencies without changing the bandwidth.

### *DSP Compensation for Nonidealities*

It was mentioned before that mismatch effects in the modulator can be compensated for in DSP. Since most of the mismatch will probably be static (like capacitor mismatch), we can do this compensation off-line. Calibration could be done by applying input tones at known frequencies and computing the corresponding ‘correction functions’ for the DSP. We have already discussed on-line compensation, which is of course a much more versatile approach, but more research needs to be done to find out whether the improvement in SNR warrants the extra DSP hardware.

### *New Architectures*

So far, most of our analysis into Complex  $\Sigma\Delta$  Modulators has been for a simple fourth-order architecture. A sixth-order design might prove to give us increased performance, although now we have to worry about stability concerns, and of course mismatch. Multi-bit architectures seems to be a logical way to go for higher order designs, and can be readily applied to Complex  $\Sigma\Delta$  Modulators. As well as this, different noise-shaping architectures (like a MASH structure) can be explored, since it is not known what kind of performance we could expect from a fourth-order MASH modulator over the conventional fourth-order design that we attempted.

In summary, Complex  $\Sigma\Delta$  Modulators may be able to hold their own in the race for higher resolution and more bandwidth, but more research needs to be done to make this a reality.

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## Appendix A : Calculation of $\Sigma\Delta$ Coefficients

The first step in calculating coefficients for a  $\Sigma\Delta$  modulator is, of course, choosing the architecture. In the preceding thesis, the architecture that was used was a Cascade-of-Delay-Cells, seen in Figure 32. This looks like a messy structure to solve, but we can simplify the structure by assuming that coefficients can be complex. The structure would then look like:

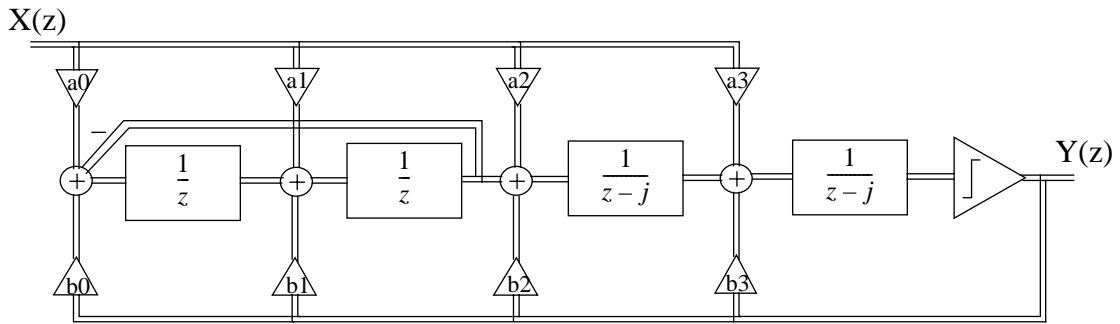


FIGURE 64. Simplified Z-Domain Block Diagram for calculating Coefficients

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We have already shown back in Figure 30 how to implement the complex integrators using delay cells. Implementing a complex coefficient is exactly the same. Figure 65 shows how to implement the coefficient in terms of its real and imaginary parts.

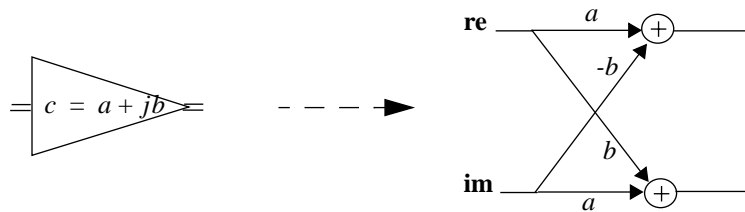


FIGURE 65. Complex Coefficient Implementation

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The first stage resonator in Figure 64 is real-valued, therefore it looks the same in both the real and imaginary channel, and it has no cross-coupling coefficients. We already stated our NTF and STF before, but as a refresher, they are:

$$NTF = \frac{(z-j)^2(z^2+1)}{(z^2+0.64)(z-0.2-0.7j)(z+0.2-0.7j)}$$

$$STF = \frac{0.5(z-0.8j)}{(z^2+0.64)(z-0.2-0.7j)(z+0.2-0.7j)}$$

From these, we can find our implementable transfer functions  $A(z)$  and  $B(z)$  which are (from chapter 3):

$$A(z) = \frac{0.5(z-0.8j)}{(z^2+1)(z-j)^2}$$

$$B(z) = \frac{-0.6j(z+1.513j)(z-0.090-0.848j)(z+0.090-0.848j)}{(z^2+1)(z-j)^2}$$

If we take a look at  $A(z)$  back in Figure 64, we can express it in terms of the coefficients  $a_0$  through  $a_3$  as:

$$A(z) = \frac{a_0 + a_1z + a_2(z^2+1) + a_3(z^2+1)(z-j)}{(z^2+1)(z-j)^2}$$

So, by equating the numerators together, we can find all the coefficients for  $A(z)$  and  $B(z)$ . These have already been summarized in Table 2 for the implemented modulator.



---

For the improved modulator outlined in Figure 34, the calculation of coefficients is exactly the same, in that  $A(z)$  and  $B(z)$  are the same. The only thing that is different in the coefficient calculation is the transfer function in terms of  $a_0$  through  $a_3$ . The new transfer function that we can equate to  $A(z)$  and  $B(z)$  to solve for the parameters is:

$$A(z) = \frac{a_0 + a_1(z - j) + a_2(z + j)^2 + a_3(z + j)^2 z}{(z^2 + 1)(z - j)^2}$$

And for this, the parameters have already been summarized in Table 3 for your convenience.

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---

## *Appendix B : Decimation Filtering in C*

```
#include <stdio.h>
#include <stdlib.h>

#define TRUE 1
#define FALSE 0
#define NO_BITS 131072

main()
{
    FILE *infile, *outfile;
    char datain[50], dataout[50], dsp_out[50], inchar;
    int i,j,flag=FALSE;
    long yre,yim,mixre,mixim,count;
    long accum1re,accum1im,accum2re,accum2im,accum3re,accum3im;
    long diff1re,diff1im,diff2re,diff2im,outre,outim,tempre,tempim;

    count = 0;
    while(!flag)
    {
        printf("Enter input filename:\n");
        scanf("%s", &datain);
        if((infile=fopen(datain, "r")) == NULL)
            printf("File does not exist.\n");
        else
            flag=TRUE;
    }
    printf("Enter output filename:\n");
    scanf("%s", &dataout);
    printf("Enter filename for DSP filtered output:\n");
    scanf("%s", &dsp_out);
    outfile=fopen(dataout, "w");
    /* inchar=fgetc(infile);*/
    /* The following lines are to test phase changes in the DSP mixer
    inchar=fgetc(infile);
    inchar=fgetc(infile);
    inchar=fgetc(infile);*/
    inchar=fgetc(infile);
    while(inchar != EOF)
```

---

```

    {
        switch(inchar)
    {
        case '0':
            fprintf(outfile,"-1 -1\n");
            break;
        case '1':
            fprintf(outfile,"1 -1\n");
            break;
        case '2':
            fprintf(outfile,"-1 1\n");
            break;
        case '3':
            fprintf(outfile,"1 1\n");
            break;
    }
    /*inchar=fgetc(infile);*/
    inchar=fgetc(infile);
    count++;
    }
    fclose(infile);
    fclose(outfile);

    infile=fopen(dataout, "r");
    outfile=fopen(dsp_out, "w");

    accum1re=0;accum2re=0;accum3re=0; accum1im=0;accum2im=0;accum3im=0;
    outre=0;diff2re=0;diff1re=0; outim=0;diff2im=0;diff1im=0;
    tempre=0;tempim=0;
    fscanf(infile, "%ld %ld", &yre, &yim);
    for(j=0;j<(count/64);j++)
    {
        for(i=0;i<64;i++)
        {
            switch(i%4)
            {
            case 0:
                mixre = yre;
                mixim = yim;
                break;
            case 1:

```

---

---

```
    mixre = yim;
    mixim = -1*yre;
    break;
case 2:
    mixre = -1*yre;
    mixim = -1*yim;
    break;
case 3:
    mixre = -1*yim;
    mixim = yre;
    break;
}

    accum1re += mixre;
    if(accum1re > NO_BITS - 1)
accum1re -= 2*NO_BITS;
    if(accum1re < -1*NO_BITS)
accum1re += 2*NO_BITS;
        accum2re += accum1re;
        if(accum2re > NO_BITS - 1)
accum2re -= 2*NO_BITS;
        if(accum2re < -1*NO_BITS)
accum2re += 2*NO_BITS;
            accum3re += accum2re;
            if(accum3re > NO_BITS - 1)
accum3re -= 2*NO_BITS;
            if(accum3re < -1*NO_BITS)
accum3re += 2*NO_BITS;

        accum1im += mixim;
        if(accum1im > NO_BITS - 1)
accum1im -= 2*NO_BITS;
        if(accum1im < -1*NO_BITS)
accum1im += 2*NO_BITS;
            accum2im += accum1im;
            if(accum2im > NO_BITS - 1)
accum2im -= 2*NO_BITS;
            if(accum2im < -1*NO_BITS)
accum2im += 2*NO_BITS;
                accum3im += accum2im;
                if(accum3im > NO_BITS - 1)
```

---

---

```
accum3im -= 2*NO_BITS;
    if(accum3im < -1*NO_BITS)
accum3im += 2*NO_BITS;

        fscanf(infile, "%ld %ld", &yre, &yim);
    }
```

```
    outre = -1*diff2re;
    diff2re = -1*diff1re;
    diff1re = -1*tempre;
        tempre = accum3re;
    diff1re += accum3re;
    if(diff1re > NO_BITS - 1)
        diff1re -= 2*NO_BITS;
    if(diff1re < -1*NO_BITS)
        diff1re += 2*NO_BITS;
    diff2re += diff1re;
    if(diff2re > NO_BITS - 1)
        diff2re -= 2*NO_BITS;
    if(diff2re < -1*NO_BITS)
        diff2re += 2*NO_BITS;
    outre += diff2re;
    if(outre > NO_BITS - 1)
        outre -= 2*NO_BITS;
    if(outre < -1*NO_BITS)
        outre += 2*NO_BITS;
```

```
    outim = -1*diff2im;
    diff2im = -1*diff1im;
    diff1im = -1*tempim;
        tempim = accum3im;
    diff1im += accum3im;
    if(diff1im > NO_BITS - 1)
        diff1im -= 2*NO_BITS;
    if(diff1im < -1*NO_BITS)
        diff1im += 2*NO_BITS;
    diff2im += diff1im;
    if(diff2im > NO_BITS - 1)
        diff2im -= 2*NO_BITS;
    if(diff2im < -1*NO_BITS)
        diff2im += 2*NO_BITS;
```

---

---

```
outim += diff2im;
if(outim > NO_BITS - 1)
    outim -= 2*NO_BITS;
if(outim < -1*NO_BITS)
    outim += 2*NO_BITS;

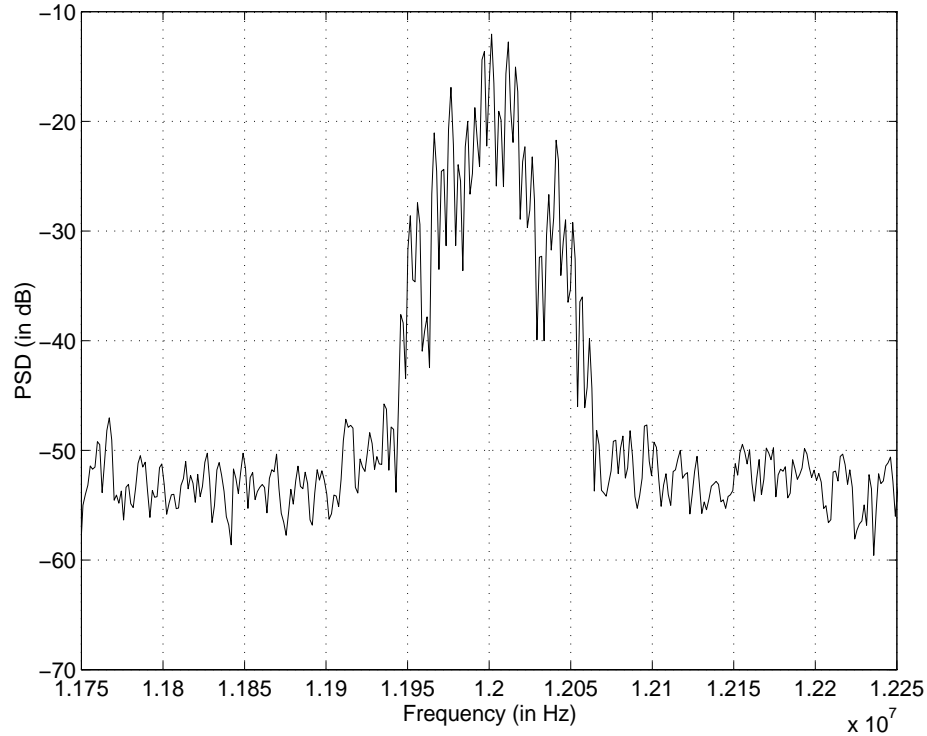
fprintf(outfile, "%ld %ld\n", outre, outim);
}
fclose(infile);
fclose(outfile);
}
```

---

---

## *Appendix C : Performance of Receiver for other GMSK inputs*

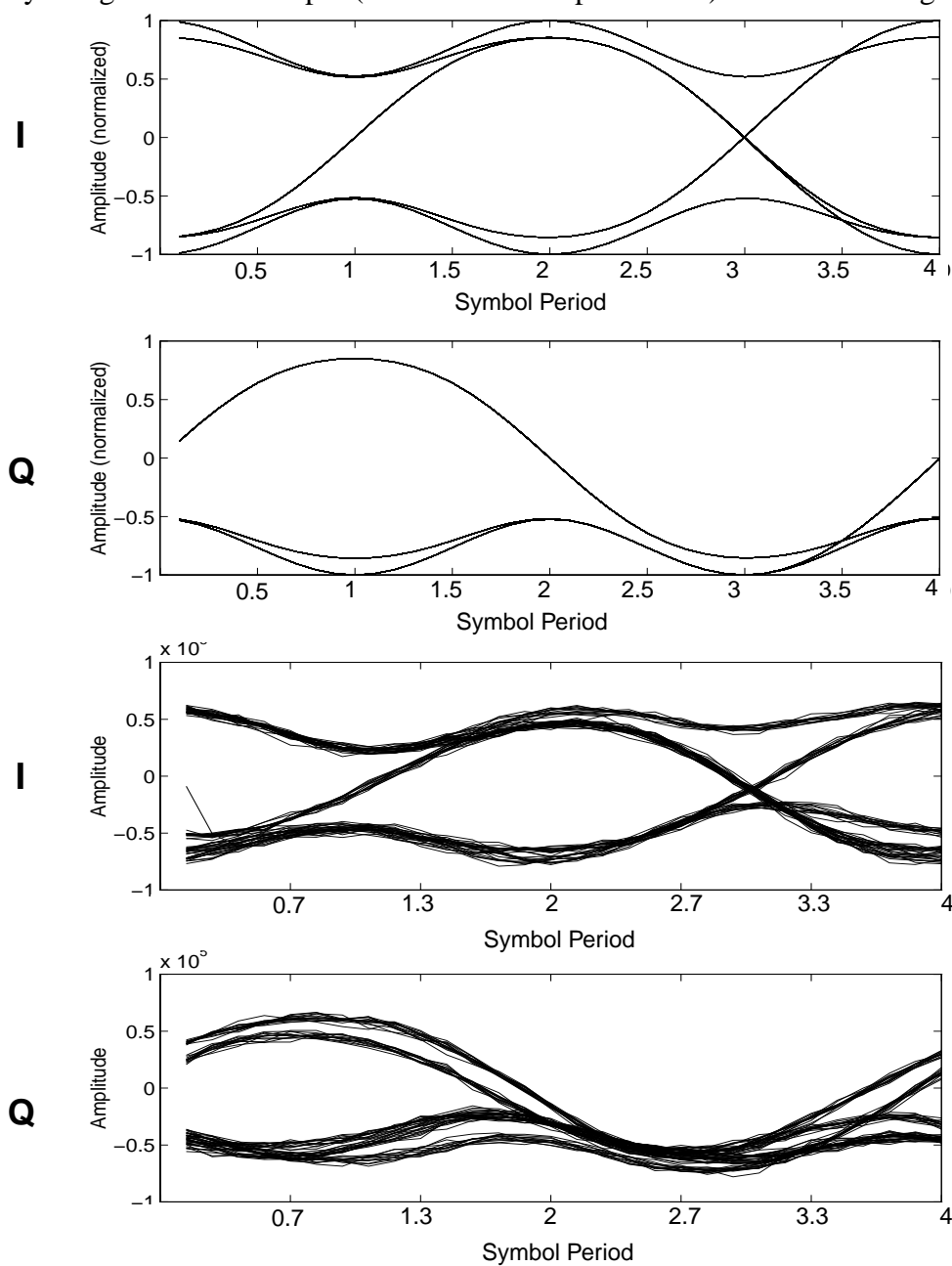
We have already shown the output of the receiver for one set of GMSK data. To get a good eye diagram, it is typical to use pseudo random data of as large a length as possible. In these cases, we used a bit sequence length of 20 bits. This explains why the output spectrum has harmonics at the data rate divided by 20 (5kHz). Below, we can see the GMSK spectrum for a sequence of length 20 with the following pseudo random pattern : [1, 1, -1, 1, -1, -1, -1, 1, 1, -1, 1, -1, 1, 1, 1, -1, -1, 1, -1, -1].



**FIGURE 66. Output Spectra of Modulator for GMSK Data**

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The eye diagrams for this input (simulated and experimental) are shown in Figure 67.



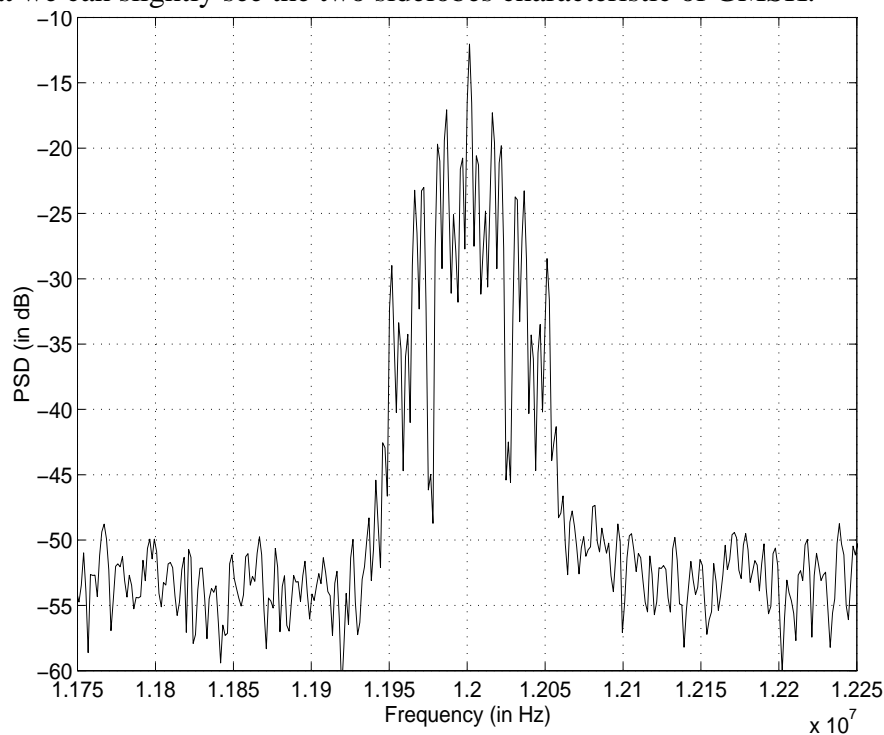
**FIGURE 67. Eye Diagrams (Simulated and Experimental) for GMSK Data**

We can see that the shape and eye openings of the experimental results correspond to the simulated results rather well. These experimental results were captured after equalizing



the phase error in the front end (it was mentioned before that this was  $19^\circ$ , by using extra cabling to add delays, we were able to get this down to  $5^\circ$ ).

Shown below is another GMSK spectrum for the following input : [-1, -1, 1, 1, -1, -1, 1, -1, -1, -1, -1, 1, 1, 1, 1, 1, 1, -1, 1]. This spectrum is slightly better than the last set of data in that we can slightly see the two sidelobes characteristic of GMSK.



**FIGURE 68. Output Spectra for GMSK Data**

And below, we have the eye diagrams for this set of input data.

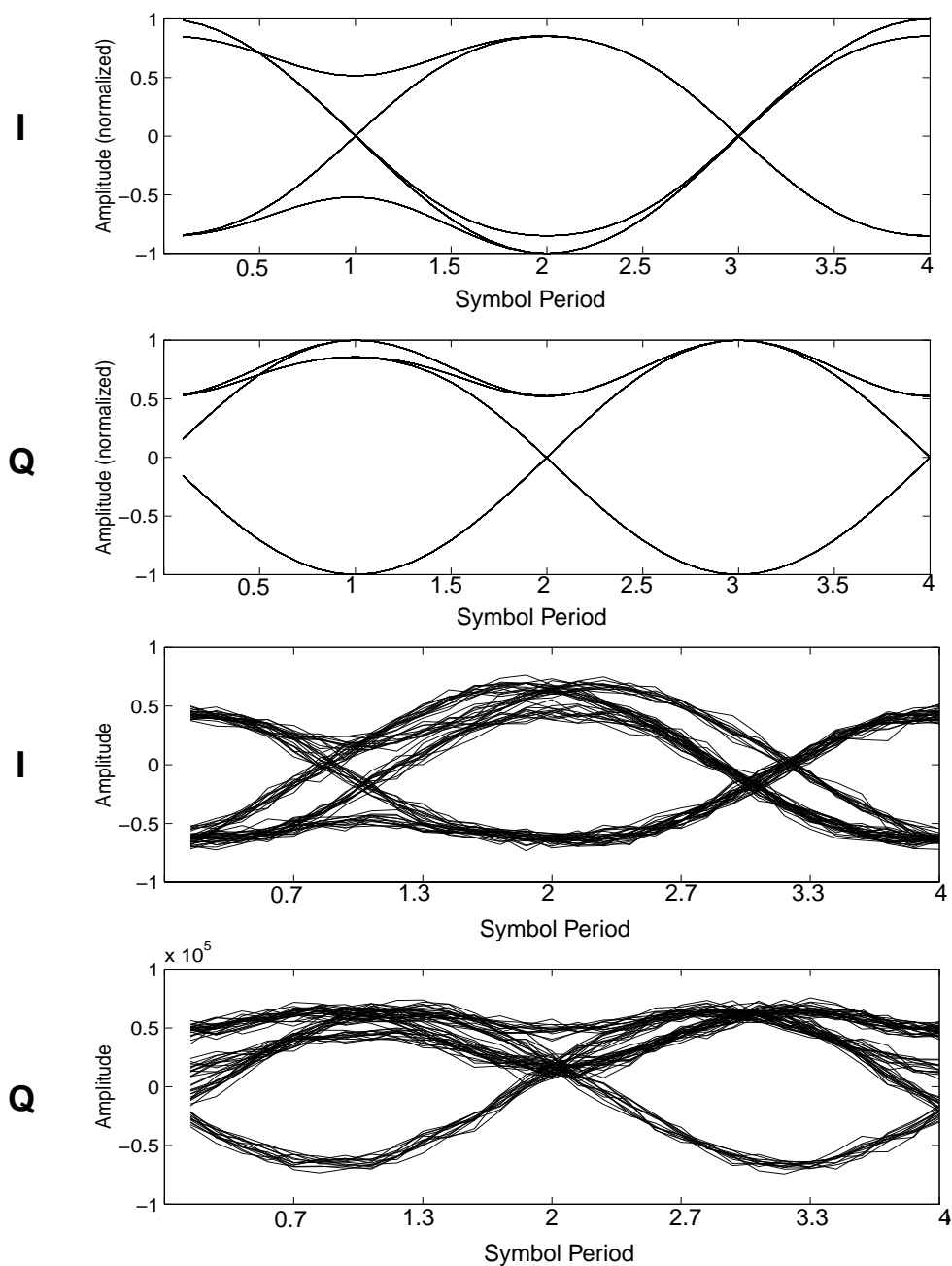


FIGURE 69. Eye Diagrams (simulated and experimental) for GMSK Data

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The results for this are the same as the previous set of data in that the eye openings and shape match the simulated results.

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