A 950-MHz IF Second-Order Integrated LC Bandpass Delta–Sigma Modulator

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***Abstract*—A second-order integrated LC bandpass delta–sigma modulator is presented. This modulator is implemented in a 0.5-μm bipolar process and can be used for digitizing radio frequency or high intermediate frequency signals. It employs an integrated LC resonator with active Q-enhancement and two nonreturn-to-zero digital-to-analog pulse-shaping feedback loops. The modulator test chip achieves a signal-to-noise ratio of 57 dB over a 200-kHz bandwidth for converting a 950-MHz signal, and dissipates 135 mW with a 5-V supply.**

***Index Terms*— Analog-to-digital converters, continuous-time circuits, delta–sigma modulators, *LC* resonators, monolithic inductors, wireless IC's.**

I. Introduction

DIGITIZING signals early in a receiver, at a high intermediate frequency (IF) or even in the radio frequency (RF) stage, makes for flexibility, simple frequency plans, and low component count at the cost of demanding specifications on the analog-to-digital (A/D) converters [1]. $\Delta\Sigma$ modulators including both lowpass modulators [2] and bandpass modulators [1] are the preferred architecture for high resolution A/D converters. A $\Delta\Sigma$ modulator can be implemented by designing the loop integrator/resonator either in the discrete-time domain such as with switched-capacitor filters [3] or in the continuous-time domain such as with RC [4], transconductor-C [5], and LC filters [6]. Most reported $\Delta\Sigma$ modulators have been implemented with the switched-capacitor technique. Continuous-time modulators are much faster and provide a certain amount of antialias filtering [5]: aliasing occurs in the delta–sigma loop and so is noise-shaped out of the band of interest. On the other hand, clock jitter modulates noise power as well as signal power in continuous-time loops, so they are more sensitive to clock phase noise. High-speed continuous-time circuits also typically have poorer linearity than switched-capacitor circuits, in which the amplifiers are linearized by feedback and in which pulse shapes during settling have no effect on the final output.

Continuous-time modulators with LC resonators in the loop have a simple structure, and have been implemented with off-chip inductors [6]–[8]. The availability of monolithic inductors on silicon makes LC integrated resonators feasible at gigahertz frequencies with good dynamic range compared to transconductor-C resonators [9], and therefore monolithic $\Delta\Sigma$ modulators with such resonators should be able to achieve bandpass conversion at gigahertz RF/IF. Because monolithic inductors typically have poor quality factors below about 1 GHz, the technology only becomes practical at very high speeds and therefore in advanced technologies.

In this paper, an integrated second-order LC bandpass $\Delta\Sigma$ modulator implemented in a 25 GHz bipolar process is described. It converts narrowband 950-MHz RF/IF signals at a sampling rate of 3.8 GHz, producing a high-speed bitstream that can then be processed digitally down to baseband. The modulator is built with an active Q-enhanced monolithic LC resonator and nonreturn-to-zero digital-to-analog (DAC) pulse-shaping feedback loops. This modulator is a proof-of-concept prototype, showing a fully monolithic active-LC $\Delta\Sigma$ modulator for the first time, and showing gigahertz bandpass operation for the first time. Some general issues and design consideration related to high speed continuous-time $\Delta\Sigma$ modulators are also addressed.

$\Delta\Sigma$ modulators with integrated LC resonators can be used to digitize IF signals for systems with carriers in the 5–30 GHz range such as local multipoint cell services or local multipoint distribution services (LMCS/LMDS, "wireless cable") and wireless LAN. If reengineered for increased sensitivity, they might even be applied to directly convert RF signals for microcell base stations.

II. Modulator Design

A. Continuous-Time Delta–Sigma Modulator Design Methodology

A continuous-time $\Delta\Sigma$ modulator is internally a discrete-time system since there is a sampler inside the loop as shown in Fig. 1. This makes the loop transfer function from the output of the quantizer back to its input have an exact equivalent z-domain transfer function as illustrated in the figure. Equivalent discrete-time and continuous-time loop filter gains are in general related by the pulse invariant transformation [5]

$$\mathcal{Z}^{-1}[\hat{A}(z)] = \mathcal{L}^{-1}[\mathrm{DAC}(s)\cdot A(s)]|_{t=nT} \tag{1}$$

where $\mathrm{DAC}(s) = (e^{-sp_1T} - e^{-sp_2T})/s$ is the arbitrary zero-order-hold pulse "transfer" function of the DAC (for the case of ideal square pulses), which in the time domain is expressed

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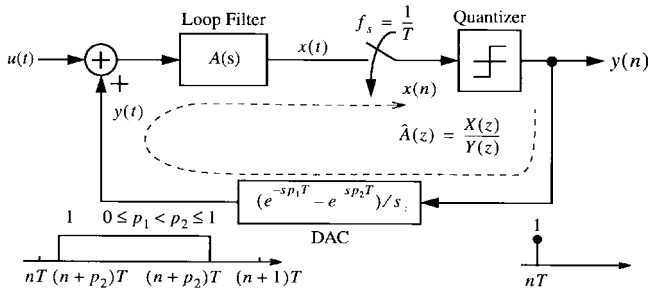


Fig. 1. Block diagram of continuous-time $\Delta\Sigma$ modulators.

as

$$\mathrm{DAC}(t) = \begin{cases} 1, & p_1 T \le t \le p_2 T \text{ where } 0 \le p_1, p_2 \le 1 \\ 0, & \text{otherwise} \end{cases}. \tag{2}$$

The set of parameters (p_1, p_2) determines the DAC pulse type, including nonreturn-to-zero (NZ, $p_1 = 0$ and $p_2 = 1$) and return-to-zero (RZ, $p_1 = 0$ and $p_2 = 1/2$) cases. From the equivalent relationship, we can have the following equation to obtain mapping relations between s-domain and z-domain functions

$$\hat{A}(z) = \mathcal{Z}\{\mathcal{L}^{-1}[\mathrm{DAC}(s) \cdot A(s)]|_{t=nT}\} \tag{3}$$

$$= z^{-1} \cdot \sum_{\text{at poles of } [A(\lambda)/\lambda]} \cdot \left[\text{residues of } \frac{A(\lambda)}{\lambda} \frac{e^{\lambda T}(e^{-\lambda p_1 T} - e^{-\lambda p_2 T})}{1 - e^{\lambda T} z^{-1}}\right] \tag{4}$$

where z^{-1} accounts for the fact that the pulse invariant transformation absorbs one clock delay for causality.

There are two steps to designing the filter architectures for continuous-time $\Delta\Sigma$ modulators. Design starts from a discrete-time prototype loop transfer function $\tilde{A}(z)$ that meets the required specifications and with desirable stability properties, and then transforms it to the continuous-time equivalent. A design example using this approach in [5] is a bandpass $\Delta\Sigma$ modulator implemented using transconductor-C filters. Transfer functions for the second-order and fourth-order bandpass $\Delta\Sigma$ modulators are of the forms

$$A(s) = (b_1 s + b_0)/(s^2 + \omega_0^2) \tag{5}$$

and

$$A(s) = \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{(s^2 + \omega_0^2)^2} \tag{6}$$

respectively.

The next step is to find a good internal structure for the loop filter, and generally starts with some simple function blocks. A general continuous-time $\Delta\Sigma$ modulator shown in Fig. 2 can be formed by a cascade of functional blocks with identical transfer functions $F(s)$, where the functional block is usually an integrator for lowpass modulators and a resonator for bandpass modulators. The equivalent discrete-time domain loop transfer function using the $\mathcal{Z}$-transform is

$$\hat{A}_l(z) = \sum_{i=1}^{l} k_i \cdot \mathcal{Z}\{\mathcal{L}^{-1}[\mathrm{DAC}(s) \cdot F^i(s)]|_{t=nT}\} \tag{7}$$

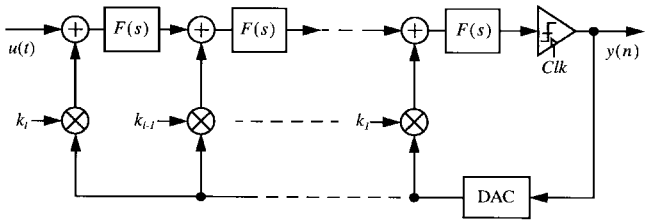


Fig. 2. A general topology of continuous-time $\Delta\Sigma$ modulators based on cascaded integrators or resonators.

TABLE I
$s \to z$ MAPPING BASED ON PULSE INVARIANT TRANSFORMATION FOR THE LC RESONATOR

Type of DAC pulses	Equivalent z-domain loop transfer function
Non-return-to-zero	$\hat{A}_{NZ} = \frac{z^{-1} - z^{-2}}{1 + z^{-2}}$
Return-to-zero	$\hat{A}_{RZ} = \frac{\left(1 - \frac{\sqrt{2}}{2}\right)z^{-1} - \frac{\sqrt{2}}{2}z^{-2}}{1 + z^{-2}}$
Half-delay return-to-zero	$\hat{A}_{HR} = \frac{\frac{\sqrt{2}}{2}z^{-1} - \left(1 - \frac{\sqrt{2}}{2}\right)z^{-2}}{1 + z^{-2}}$

where l is the number of functional blocks in cascade, and $\{k_i\}$ $(i = 1, 2, \cdots, l)$ are the DAC pulse-shaping coefficients. The pulse-shaping coefficients are calculated by equating $\hat{A}_l(z)$ to the desired discrete-time prototype transfer function $\tilde{A}_l(z)$. The functional block for lowpass modulators is typically designed as a first-order transconductor-C integrator with transfer function $1/s$, and for bandpass modulators it can be designed as an LC resonator with transfer function $\omega_0 s/(s^2 + \omega_0^2)$.

A second-order $\Delta\Sigma$ modulator constructed using an LC resonator has the continuous-time domain loop transfer function

$$A(s) = \frac{\omega_0 s}{s^2 + \omega_0^2}. \tag{8}$$

Its equivalent z-domain loop transfer function can thus be derived from (4) based on the feedback DAC pulses. Table I lists the equivalent z-domain loop transfer functions obtained for NZ, RZ, and half-clock-period delayed return-to-zero (HR) DAC pulses.

The loop transfer function of a standard discrete-time lowpass $\Delta\Sigma$ modulator prototype is

$$A_{1lp}(z) = \frac{z^{-1}}{1 - z^{-1}}. \tag{9}$$

Performing the transformation $z^{-1} \to -z^{-2}$ leads to a second-order bandpass $\Delta\Sigma$ modulator with its noise-shaping notch center at one-quarter of the sampling frequency, which has the loop transfer function

$$A_{2bp}(z) = \tilde{A}_{2bp}(z) = \frac{z^{-2}}{1 + z^{-2}}. \tag{10}$$

It can be seen that none of the equivalent z-domain loop transfer functions listed in Table I matches the desired discrete-time domain transfer function given by (10) because there are not enough degrees of design freedom. In general, a loop

of order N needs N DAC feedback coefficients to define the N numerator coefficients of (5) or (6), but because each resonator is of order 2, there are only $N/2$ DAC gains in the feedback to define the b_i. This problem is sometimes avoided with switched-capacitor circuits because transfer functions symmetric about $f_s/4$ have their odd-order b_i equal to zero, but in continuous-time design we are not so fortunate.

One approach to this problem is to add damping resistors to the resonators, which improves stability but which reduces signal-to-noise ratio (SNR) [7]. A combination of LC resonators and transconductor-C resonators can also be considered but the simplicity of continuous-time modulators with LC resonators is lost. The method used in this work is to use a linear combination of two DAC pulse feedback loops to provide a full degree of freedom to obtain the correct loop impulse response [10]. The design starts by finding coefficients for the ideal case without excess loop delay contributed by blocks in the modulator feedback loop (the comparator, the D flip-flops and the DAC's). For a modulator with l LC resonators in cascade and with two DAC pulse feedback loops, the equivalent discrete-time domain loop transfer function is

$$\begin{aligned}\hat{A}_l(z) &= \sum_{i=1}^{l} k_{ai}\mathcal{Z}\left(\mathcal{L}^{-1}\left\{\mathrm{DAC}_a(s)\cdot\left[\frac{\omega_0 s}{(s^2+\omega_0^2)}\right]^i\right\}\Bigg|_{t=nT}\right) \\ &\quad + k_{bi}\mathcal{Z}\left(\mathcal{L}^{-1}\left\{\mathrm{DAC}_b(s)\cdot\left[\frac{\omega_0 s}{(s^2+\omega_0^2)}\right]^i\right\}\Bigg|_{t=nT}\right).\end{aligned} \tag{11}$$

For the second-order bandpass modulator, (11) simplifies to

$$\begin{aligned}\hat{A}_{2bp}(z) &= k_{a1}\mathcal{Z}\left\{\mathcal{L}^{-1}\left[\mathrm{DAC}_a(s)\cdot\frac{\omega_0 s}{(s^2+\omega_0^2)}\right]\Bigg|_{t=nT}\right\} \\ &\quad + k_{b1}\mathcal{Z}\left\{\mathcal{L}^{-1}\left[\mathrm{DAC}_b(s)\cdot\frac{\omega_0 s}{(s^2+\omega_0^2)}\right]\Bigg|_{t=nT}\right\}.\end{aligned} \tag{12}$$

Equating $\hat{A}_{2bp}(z)$ to $\tilde{A}_{2bp}(z)$, we obtain the required DAC pulse-shaping coefficients $\{k_{a1}, k_{b1}\}$ to make a match between the desired second-order bandpass modulator prototype loop transfer function and the equivalent z-domain loop transfer function of the second-order LC bandpass modulator. For the modulator using RZ and HR DAC pulse feedback loops, we have

$$\begin{aligned}\hat{A}_{2bp}(z) &= k_{rz}\frac{\left(1-\frac{\sqrt{2}}{2}\right)z^{-1}-\frac{\sqrt{2}}{2}z^{-2}}{1+z^{-2}} \\ &\quad + k_{hr}\frac{\frac{\sqrt{2}}{2}z^{-1}-\left(1-\frac{\sqrt{2}}{2}\right)z^{-2}}{1+z^{-2}}.\end{aligned} \tag{13}$$

Let $\hat{A}_{2bp}(z)$ equal to $\tilde{A}_{2bp}(z)$

$$\begin{aligned}&\left[\left(1-\frac{\sqrt{2}}{2}\right)k_{rz}+\frac{\sqrt{2}}{2}k_{hr}\right]z^{-1} \\ &\quad + \left[-\frac{\sqrt{2}}{2}k_{rz}-\left(1-\frac{\sqrt{2}}{2}\right)k_{hr}\right]z^{-2} \equiv z^{-2}\end{aligned} \tag{14}$$

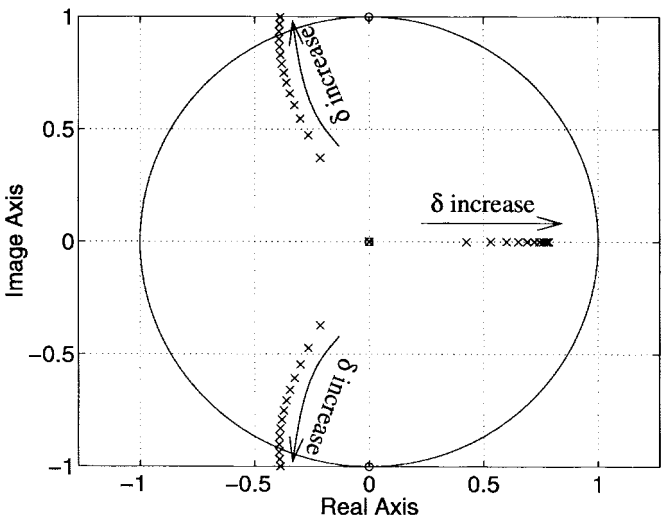


Fig. 3. Noise transfer function pole-zero locus diagram of second-order continuous-time bandpass $\Delta\Sigma$ modulators with excess loop delay.

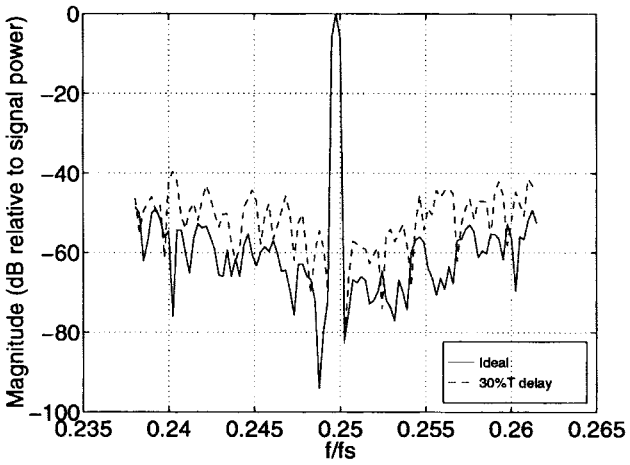
which results in $\{k_{rz} = -\sqrt{2}/2,\ k_{hr} = 1+\sqrt{2}/2\}$. Similarly, we have $\{k_{nz} = 1+\sqrt{2}/2,\ k_{rz} = -(1+\sqrt{2}/2)\}$ for the modulator using NZ and RZ DAC pulses, and $\{k_{nz} = \sqrt{2}/2,\ k_{hr} = 1+\sqrt{2}\}$ for the one using NZ and HR DAC pulses.

B. Excess Loop Delay and Nonideal DAC Effects and Their Mitigation

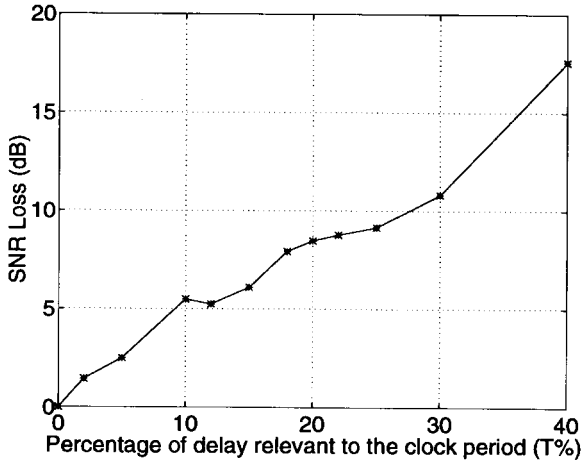
A practical continuous-time $\Delta\Sigma$ modulator suffers excess loop delay contributed by each of its building blocks in feedback. Excess loop delay can be modeled as δT, where $0 < \delta \leq 1$. With the unwanted excess loop delay in the $\Delta\Sigma$ modulator, the discrete-time domain loop transfer function moves away from the desired discrete-time $\Delta\Sigma$ modulator prototype loop transfer function since the modulator pulse response at the sampling instants is changed. The actual realized discrete-time loop transfer function can be obtained using the modified $\mathcal{Z}$-transform [11]. For the second-order bandpass $\Delta\Sigma$ modulators, we can find that the actual equivalent discrete-time loop transfer function is

$$A_{2bp}(z,\,\delta) = z^{-1}\frac{\left[z^{-1}\sin\frac{(1-\delta)\pi}{2}+z^{-2}\sin\frac{\delta\pi}{2}\right]}{1+z^{-2}}. \tag{15}$$

From the above equation, it can be seen that the excess delay in the loop changes the numerator of the resultant equivalent discrete-time loop transfer function and therefore affects the noise shaping transfer function. The actual noise transfer function becomes third-order rather than second-order since the order of the feedback open loop is increased by one. Fig. 3 plots the pole-zero loci of the actual realized noise transfer function based on (15). It shows how the poles move from the origin with an increment of excess loop delay in $0.05T$ (5% clock period) steps. It can be observed that two poles will move out of the unit circle after a delay of 58% of a period. This means that excess loop delay may eventually make continuous-time $\Delta\Sigma$ modulators unstable. Higher-order modulators suffer more severe performance degradation [11].



(a)



(b)

Fig. 4. Performance degradation due to excess loop delay: (a) output spectra and (b) SNR loss versus excess loop delay.

Fig. 3 also shows that all noise transfer function zeros are still on the unit circle with one more added to the origin. We can, therefore, expect that the signal-to-noise ratio will not degrade significantly up to a certain excess loop delay.

The analysis leading to (15) uses a simplification conventional in the $\Delta\Sigma$ literature, modeling the quantizer as a linear component and arbitrarily assigning it unity gain. This simple model predicts qualitative behavior well, but has to be backed up with nonlinear simulations. To understand how the excess loop delay affects the noise-shaping performance, s-domain simulation using ELDO was performed. Fig. 4(a) gives output spectrum plots for the ideal case and the case with 30% period excess loop delay, and Fig. 4(b) shows the signal-to-noise (SNR) loss versus the percentage of excess loop delay compared to the sampling clock period for second-order continuous-time bandpass $\Delta\Sigma$ modulators (for an oversampling ratio of 250).

We consider two nonidealities associated with the 1-bit DAC: one is the unavoidable propagation delay which contributes a certain amount of delay between the sampling instant and the DAC pulse; another is the nonzero rise and fall times which make the actual DAC pulse nonrectangular in form. If the DAC pulses do not extend into the next sampling instant (i.e., if $p_2 \leq 1$), both DAC nonidealities only make the actual equivalent discrete-time domain transfer function exhibit different numerator coefficients compared to the one based on the ideal DAC pulse. We can then adjust the feedback gains $\{k_i\}$ to achieve the correct discrete-time domain transfer function for noise-shaping. If the DAC nonidealities make the DAC pulses cross into the next sampling instant, the order of the actual equivalent discrete-time domain loop transfer function will increase by one compared to the transfer function obtained from the ideal DAC pulse [12].

The basic method for mitigating the excess loop delay and nonideal DAC effects is to find a way to provide a full degree of freedom to make the equivalent discrete-time domain loop transfer function match the desired transfer function. Continuous-time $\Delta\Sigma$ modulator designs using RZ DAC pulses may avoid increasing the loop order, because they have $0.5T$ of margin before crossing into the next time slot. The excess loop delay and DAC nonidealities in this case can be compensated simply by tuning the feedback coefficients. If one more order is added, the adjustment of feedback gains can only compensate the excess loop delay and DAC nonidealities partially, and it is necessary to introduce an extra independent design parameter. Applying an extra DAC feedback loop to the front-end building block might be the simplest method.

C. Modulator Design Using Nonreturn-to-Zero Feedbacks

Because of the speed limitations of the 0.5-μm silicon bipolar process that we used for the modulator implementation, NZ and half-clock-period delayed nonreturn-to-zero (HN) DAC pulses were selected for feedback; the RZ style produces very narrow pulses. The equivalent discrete-time domain loop transfer function using HN DAC pulse for feedback is

$$\hat{A}_{\mathrm{HN}}(z) = \hat{A}_{\mathrm{HR}}(z) + \hat{A}_{\mathrm{RZ}}(z) \cdot z^{-1} \tag{16}$$

i.e.,

$$\hat{A}_{\mathrm{HN}}(z) = \frac{\sqrt{2}}{2} z^{-1} \left(\frac{1 - z^{-2}}{1 + z^{-2}} \right) \tag{17}$$

which shows that DAC feedback loop using the HN pulse has an equivalent discrete-time domain loop transfer function with an order higher than the continuous-time loop transfer function. This is due to the fact that HN DAC pulse extends (even ideally) into the next sampling instant. The combination of NZ and HN DAC pulse feedback loops results in

$$\hat{A}_{2bp}(z) = k_{nz} \frac{z^{-1} - z^{-2}}{1 + z^{-2}} + k_{hn} \frac{\sqrt{2}}{2} z^{-1} \left(\frac{1 - z^{-2}}{1 + z^{-2}} \right). \tag{18}$$

Collecting numerator terms, we obtain

$$\hat{A}_{2bp}(z) = \frac{\left(k_{nz} - \frac{\sqrt{2}}{2} k_{hn} \right) z^{-1} - k_{nz} z^{-2} - \frac{\sqrt{2}}{2} k_{hn} z^{-3}}{1 + z^{-2}}. \tag{19}$$

It can be seen that the numerator contains an additional term in z^{-3}, but we have only two independent coefficients k_{nz} and k_{hn} for control. Tuning k_{nz} and k_{hn} cannot make the actual realized discrete-time domain loop transfer function match

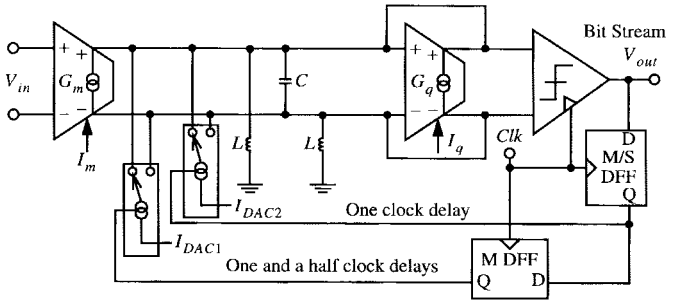


Fig. 5. Block diagram of the second-order LC bandpass $\Delta\Sigma$ modulator.

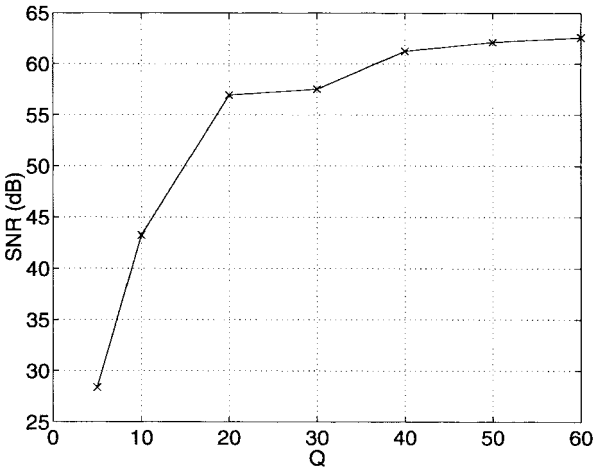


Fig. 6. Effect of the active-LC filter Q on SNR.

the desired transfer function, but can still somewhat optimize modulator noise-shaping performance. As an example of a solution, one could add a feedback loop with a one-quarter-period delay NZ DAC pulse (QN) (or a three-quarter-period delay NZ DAC pulse) to obtain an equivalent discrete-time domain loop transfer function

$$\hat{A}_{2bp}(z) = k_{nz}\cdot\hat{A}_{\mathrm{NZ}}(z)+k_{hn}\cdot\hat{A}_{\mathrm{HN}}(z)+k_{qn}\cdot\hat{A}_{QN}(z). \quad (20)$$

Substituting for $\hat{A}_{\mathrm{NZ}}(z)$ and $\hat{A}_{\mathrm{HN}}(z)$ and $\hat{A}_{\mathrm{QN}}(z)$, we have as shown in (21), at the bottom of the page. Equating $\hat{A}_{2bp}(z)$ to $\tilde{A}_{2bp}(z)$ yields $\{k_{nz} = -4.87,\ k_{hn} = -4.87,\ k_{qn} = 9.01\}$.

Fig. 5 shows the block diagram of our experimental second-order LC bandpass $\Delta\Sigma$ modulator, which has only two coefficients. Transconductor G_m translates the input differential voltage to an output differential current which is summed with DAC feedback switching currents and then fed into the differential LC resonators. Transconductor G_q is placed in positive feedback to operate as a negative resistor for compensating the losses in the monolithic inductors. The clocked comparator acts as a signal sampler and one-bit quantizer. The comparator output signal is latched twice (for one full clock delay) for one DAC feedback loop, and three times (one-and-one-half clock delays) for another feedback loop before it is used for noise shaping. Feedback DAC pulse-shaping gains are adjusted by tuning DAC switching currents to achieve a good noise shaping behavior and to provide partial compensation of time-domain nonidealities.

III. Circuit Design

For the circuit implementation of the LC bandpass $\Delta\Sigma$ modulator, the nonidealities of the circuit building blocks need to be taken into consideration. These nonidealities include circuit noise, finite quality factor (Q), nonlinearity of the active-LC filter, and time-domain nonidealities such as excess loop delay, finite rise and fall times, and clock jitter.

A. Linear Active Q-Enhanced LC Filter

Ideally, to achieve the best noise shaping performance, the LC resonator should have an infinite Q to put the loop-filter poles exactly on $j\omega$ axis. However, it is well known that monolithic inductors are lossy with a typical quality factor of 3–8 in the low gigahertz range. Fig. 6 plots the signal-to-noise ratio performance versus the value of the quality factor for the second-order LC bandpass $\Delta\Sigma$ modulator. It can be seen that (for a measurement bandwidth of 5 MHz or an oversampling ratio of 400) the noise shaping performance is degraded drastically for Q less than 20. The low Q of the filter makes the noise transfer function flatten out in the center of the passband instead of continuing to fall off. The losses of the monolithic inductor therefore need to be compensated to boost the Q of the LC filter to the value required for good noise shaping.

As shown in the second-order LC bandpass $\Delta\Sigma$ modulator block diagram (Fig. 5), the differential LC tanks plus transconductor G_m and transconductor G_q give a second-order bandpass filter response with Q-enhancement. Internal node signal swings define the linearity requirement of both transconductors, but are not linearly related to Q as they would be for the filter on its own: the quantizer feedback acts as a type of damping. The simulated output spectra with the transconductors operating in the linear and nonlinear ranges are shown in Fig. 7. It can be observed that the transconductor nonlinearity introduces strong intermodulation products in the signal band which fill in the noise shaping notch, and therefore the noise shaping performance is reduced significantly.

Reducing internal signal swings to control nonlinearity is undesirable not only because it reduces internal SNR but because it makes the design of the subsequent comparator more difficult: at these high speeds, the additional delay in a comparator that comes from having to amplify small signals is a serious problem. Linearizing transconductors with simple emitter degeneration is not a good solution either, because the resulting circuits do not have the tunability needed (at least

$$\hat{A}_{2bp}(z) = \frac{\left[k_{nz} + \frac{\sqrt{2}}{2}k_{hn} + \cos\left(\frac{\pi}{8}\right)k_{qn}\right]z^{-1} + \left\{\left[\sin\left(\frac{\pi}{8}\right) - \cos\left(\frac{\pi}{8}\right)\right]k_{qn} - k_{nz}\right\}z^{-2} - \left[\sin\left(\frac{\pi}{8}\right)k_{qn} + \frac{\sqrt{2}}{2}k_{hn}\right]z^{-3}}{1+z^{-2}} \quad (21)$$

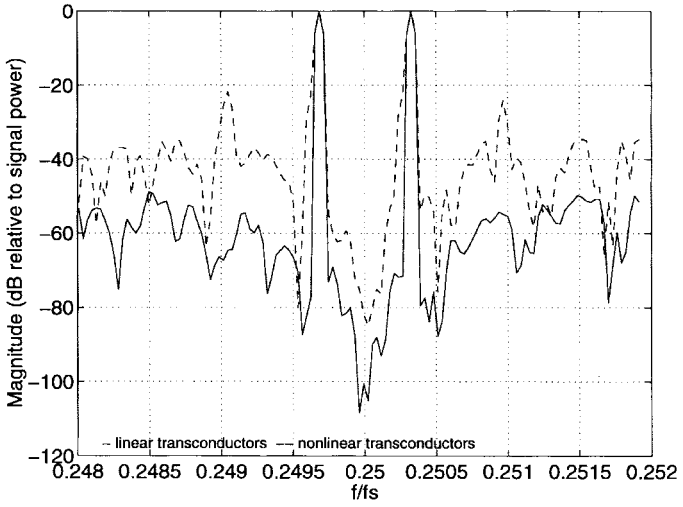


Fig. 7. Effect of transconductor nonlinearity.

for G_q) to compensate for process and temperature variability.

Transconductors implemented using multi-tanh translinear circuits have excellent tunability and are not noisy. However, their achievable input linear operation range is still limited, typically less than 100 $\mathrm{mV_{pp}}$ in general, and about 40 $\mathrm{mV_{pp}}$ for a multi-tanh doublet (two unbalanced differential pairs) at 1% transconductance falloff [13]. To further improve the usable signal swing while maintaining tunability, the emitter-coupled differential pair can be degenerated by adding diodes in series between the emitters of input transistors [14]. A series-diode-doublet shown in Fig. 7 is used to implement G_m for obtaining a reasonable linear range with tunability. It consists of two unbalanced series-diode-connected emitter-coupled pairs connected in parallel. The "4×" ratioed transistors are formed by connecting four unit transistors in parallel to be relatively independent of process. The left differential pair has an offset voltage of $3V_T \ln 4$, while the right pair has an offset of $-3V_T \ln 4$ ($V_T = kT/q$ is the thermal voltage). The resultant input linear range of the transconductor is therefore approximately $6V_T \ln 4$, i.e., 216 mV at room temperature. The transconductance in the linear range is

$$G_m = \frac{16 I_m}{75 V_T} \tag{22}$$

which is 820 μS for I_m = 100 μA, and the equivalent input noise voltage is

$$\frac{\tilde{V}_{nm}}{\sqrt{\Delta f}} \approx \sqrt{\frac{75}{4} kT \left(2R_{bb} + \frac{V_T}{I_m}\right)} \tag{23}$$

where R_{bb} is the base resistance of the transistor.

Multi-tanh circuits have residual nonlinearities, and can have a "multiple maximum" shape to their G_m as signal varies. This in turn can make a Q-enhancement circuit difficult to control, because increasing gain with signal level can cause jump oscillation phenomena. We therefore adopted a more conservative diode linearization technique, introduced in [15] to achieve a large linear range and tunability, for the implementation of G_q as shown in Fig. 8. This circuit is basically a Gilbert gain cell—a logarithmic compression

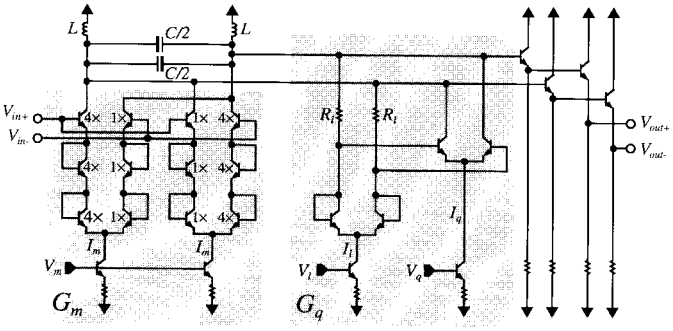


Fig. 8. Linear Q-enhanced LC filter schematic.

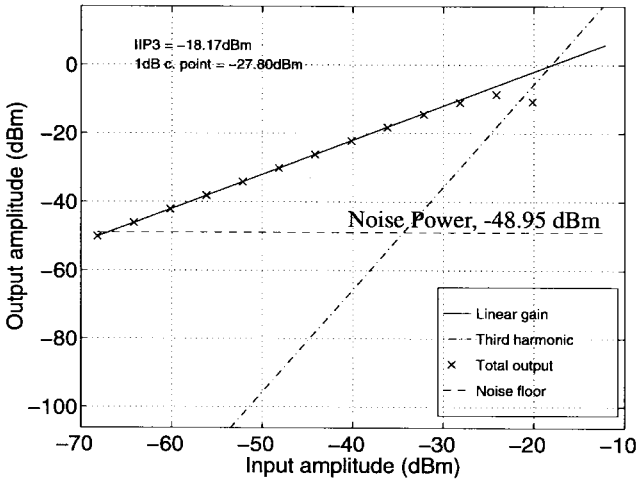


Fig. 9. Third-order intercept point plot of the active LC filter.

circuit that compensates for the exponential expansion of the differential emitter-coupled pair. The input linear range is increased over that of a simple differential pair by a factor of $\eta = (1 + R_l I_l / 2V_T)$. The circuit has a transconductance tunable by bias currents of

$$G_q = \frac{2I_q}{R_l I_l} \tag{24}$$

which is 15.4 mS for $I_q = 5.22$ mA, $I_l = 2.26$ mA, and $R_l = 300\ \Omega$. The input referred noise voltage is

$$\frac{\tilde{V}_{nq}}{\sqrt{\Delta f}} \approx \sqrt{4kT\left(2\eta^2 R_{bb} + R_l + \frac{\eta I_q V_T}{2I_l^2}\right)}. \tag{25}$$

Fig. 8 gives the circuit schematic of the second-order band-pass filter. Taking into account the parasitic resistance of the LC tank which is modeled by R_p, the filter transfer function is

$$\frac{V_{\mathrm{out}}(s)}{V_{\mathrm{in}}(s)} = \frac{\left(\frac{G_m}{C}\right)s}{\left[s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2\right]} \tag{26}$$

where

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{27}$$

$$Q = \frac{R_p C}{1 - R_p G_q}\,\omega_0. \tag{28}$$

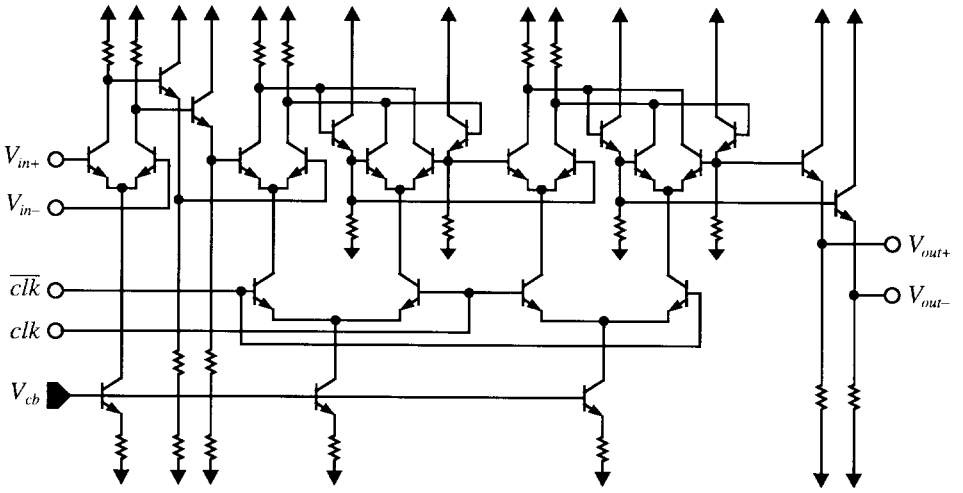


Fig. 10. Master/slave-type ECL clocked comparator.

The LC filter was designed for a nominal center frequency of 1 GHz in a 0.5-μm bipolar technology based on SPICE simulation. Two identical capacitors are connected back to back in parallel as shown in the figure to maintain balance in the presence of substrate parasitics. The component values in the design are: $L = 7.0$ nH and $C = 1.1$ pF. The spiral inductors were selected from a library and have a nominal Q of 4 at 1 GHz. The capacitors were designed using a metal-insulator-metal structure to achieve the best quality factor and the best tolerance.

Two-tone simulation was performed to extract the intermodulation distortion products for the stand-alone active-LC filter with its Q enhanced to 40, and Fig. 9 is the resultant IP3 plot. The input intercept point (IIP3) is -18.17 dBm, and the 1 dB compression point is -27.8 dBm. This test is very pessimistic, because the high Q gives the filter high in-band gain and induces internal distortions; in the actual modulator we operate with lower internal gains because of the damping effects of the $\Delta\Sigma$ loop.

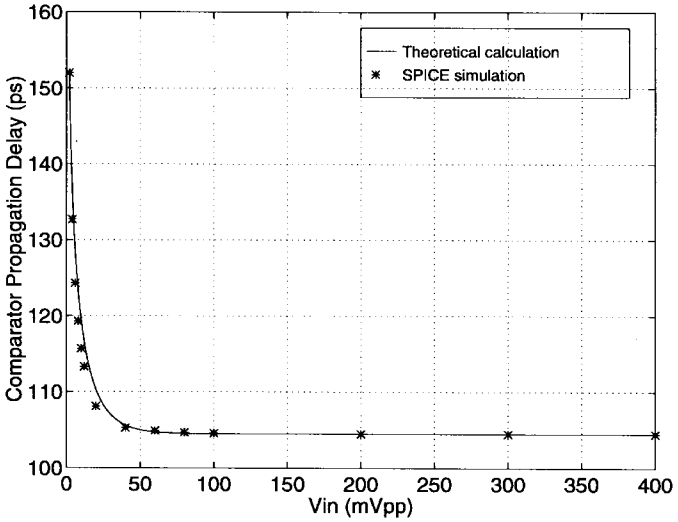


Fig. 11. Comparator propagation delay versus its input voltage.

B. Comparator

The one-bit quantizer shown in Fig. 10 is a clocked comparator which is a conventional master/slave-type differential ECL latching comparator with a preamplifier [16]. The preamplifier helps to increase operation speed and reduce clock flashback to the previous stage. It also helps to reduce the input dependent jitter effect [17]. The gain of the preamplifier was designed to be 7.6. The designed comparator output voltage swing is 600 mV peak to peak. The emitter followers in the circuit provide a level shift and further reduction of flashback. Large transistors were used in the emitter followers. Sampling takes place on every falling edge of the clock signal. The SPICE simulated rise and fall times are about 145.6 ps, at a comparator input level of 4 $\mathrm{mV_{pp}}$; while the propagation delay for both rising and falling edges is about 132.7 ps at this level. The comparator propagation delay is input-signal dependent for small signals, dominated by the recovery time. This is the time required in the sample mode for an input voltage to change the output of the latching comparator from one logic state to the midpoint of the logic states, whose relation to the input voltage is [18]

$$t_{rec} \propto \ln\left[1 + \frac{1}{\tanh\left(\frac{V_{\mathrm{in}}}{2V_T}\right)}\right]. \tag{29}$$

For large comparator inputs, the propagation delay is roughly a constant which is about 104.5 ps based on SPICE simulation, and is mainly determined by the regeneration time. Fig. 11 gives a plot of the comparator propagation delay as a function of its input voltage.

The differential ECL structure in the comparator was applied for both the master/slave D flip-flop and the master-only D flip-flop design. Metastability is caused by the comparator's inability to resolve a small differential input into a valid output binary level. It results in a timing error in the signal and noise transfer functions. As described in Fig. 5, the comparator output signal will be latched twice or three times before it is used. This should reduce metastability to a negligible level.

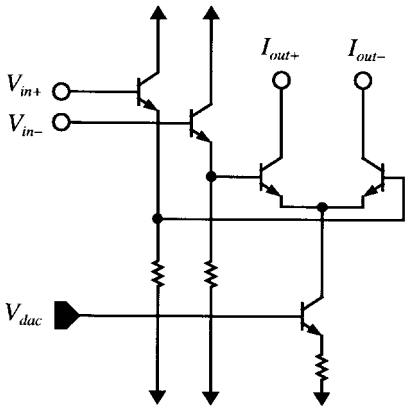


Fig. 12. Schematic of the current switched one-bit DAC.

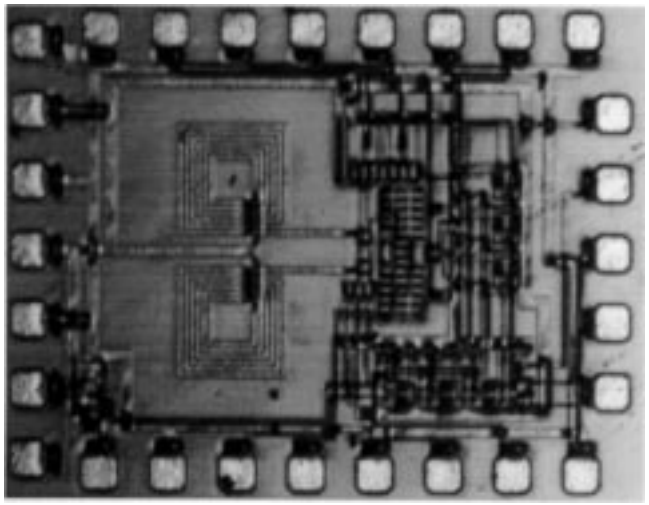


Fig. 13. Microphotograph of the LC bandpass $\Delta\Sigma$ modulator.

C. Current-Switching DAC

The feedback DAC is key to good linearity and ideal noise-shaping behavior, because pulse-memory effects can cause input-referred nonlinearity and a nonideal noise-shaping loop transfer function. Unmatched rise and fall times can generally be controlled by using RZ waveforms and/or by using balanced circuits, and a desired noise-shaping transfer function might be achieved by RZ. But RZ waveforms are not practical when clocking at one-sixth of the maximum cutoff frequency of the IC process.

Fig. 12 shows the one-bit current switching DAC. It is formed by input emitter followers and a simple current steered differential pair. The current switching DAC combined with the previous D flip-flop produces nonreturn-to-zero pulse waveforms. The excess delay from the sampling instant to the DAC pulse waveforms is determined by the propagation delay of the previous D flip-flops in the loop; while the rise and fall times of the DAC pulses are determined by the rise and fall times of these D flip-flops. For the master-slave flop-flop in the loop, the simulated propagation delay is about 77.8 ps, and the rise and fall times are about 78.2 ps. For the master-only flip-flop, we have the simulated propagation delay of 72.4 ps, and the rise and fall times of 64.7 ps.

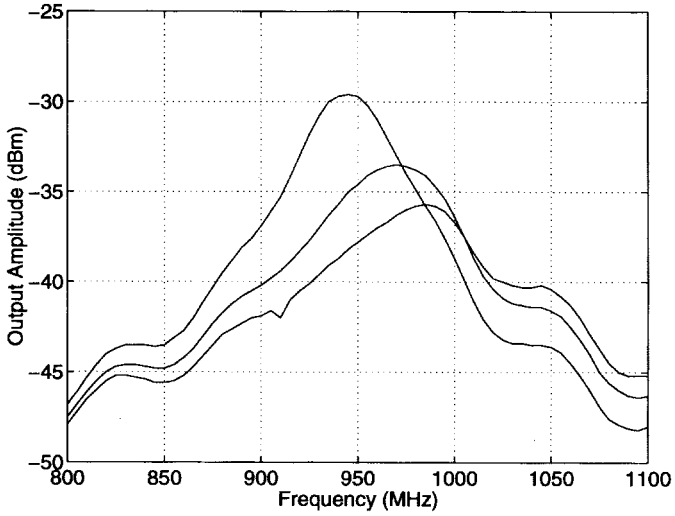


Fig. 14. Measured frequency response of Q tuning for the active-LC filter.

TABLE II
MODULATOR MEASURED PERFORMANCE

Parameters	Experimental
Technology	0.5 μm double-poly bipolar
Power Supply	5 V
Power Consumption	135 mW
Center frequency	950 MHz
Sampling frequency	3.8 GHz
Maximum SNR	57 dB SNR (200 kHz bandwidth) 45 dB SNR (3 MHz bandwidth)

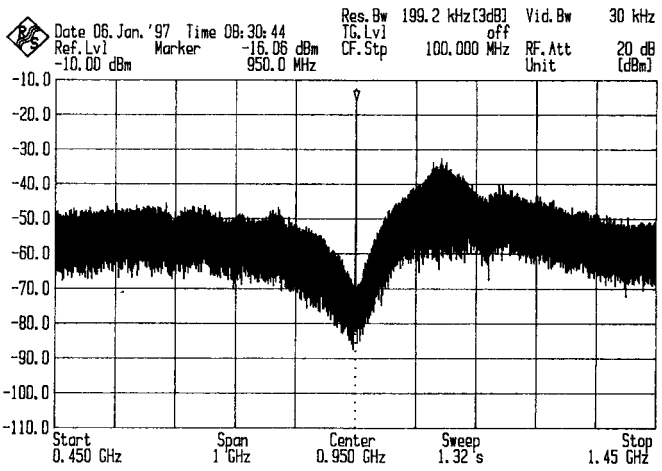


Fig. 15. Measured output spectrum of the modulator.

IV. EXPERIMENTAL RESULTS

The modulator was implemented in a 0.5-μm double-polysilicon bipolar process with maximum f_t of 25 GHz. Two output differential buffers with 50 Ω termination resistors were designed for the Q-enhanced LC filter and the modulator to test their performance. The implemented core circuit of the modulator consumes a silicon area of 700 $\times$ 900 μm^2. The test chip was bonded in a CQFP package with 44 pins. The chip microphotograph is given in Fig. 13.

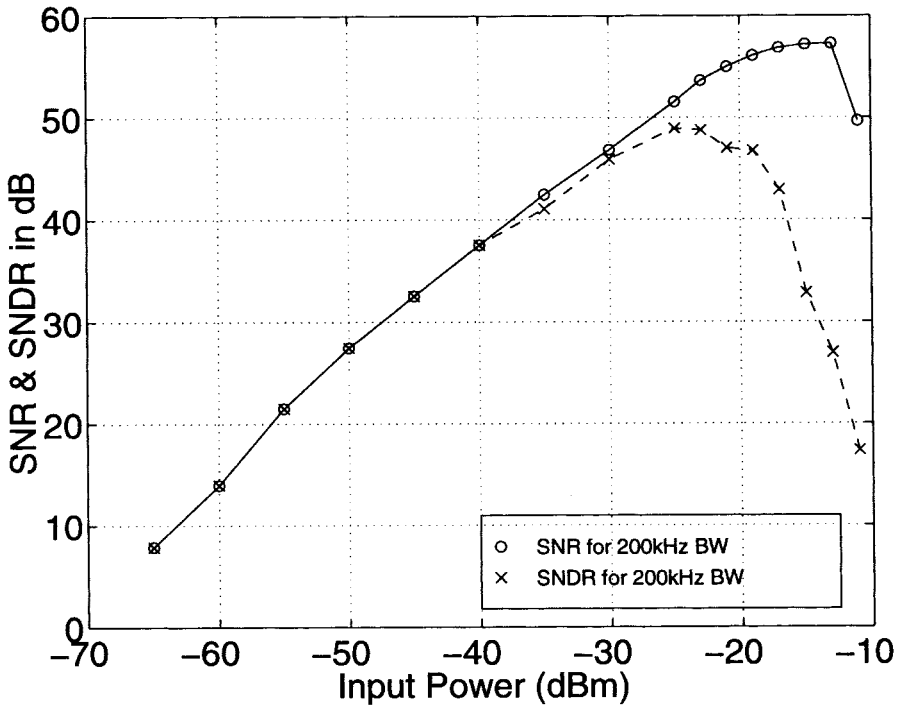


Fig. 16. Measured SNR and SNDR versus input power.

To test the chip differentially, we used a pair of two-way 180° broadband power splitters/combiners to implement the single-ended-to-differential and differential-to-single-ended converters required at the input and output of the modulator. The combiners/splitters have almost flat responses from 200 kHz to 17 GHz. The test results described below were calibrated based on the loss between the instruments and chip PCB board.

The filter frequency responses measured using a network analyzer are shown in Fig. 14, in which it can been seen that the filter Q can be tuned to a high value. The curves show several nonidealities, including compression effects. When tuning the stand-alone filter, care has to be taken to avoid oscillation, but the modulator loop stabilizes the filter even if its poles are slightly in the right half-plane, so this is not a problem in practice.

The measured performance of the modulator is summarized in Table II. Fig. 15 shows the measured output bitstream spectrum with a −20 dBm input signal at 950 MHz, and a 3.8-GHz clock frequency. The measured maximum SNR is 57 dB over a 200-kHz bandwidth, or 45 dB in a 3-MHz bandwidth. For comparison, the simulated maximum SNR's over a 3-MHz bandwidth from ELDO for an ideal case (with RZ and HR feedback loops) and for the extracted circuit are about 70 and 54 dB, respectively. Fig. 16 plots measured SNR and signal-to-noise plus distortion ratio (SNDR) in a bandwidth of 200 kHz as a function of input signal level for an input tone offset from $f_s/4$ by 50 kHz. This choice of frequencies puts a dominant spur, the alias of the third harmonic, 100 kHz on the other side of $f_s/4$ and just in-band, and this spur limits SNDR at high input levels. The modulator draws a total current of 27 mA from a 5-V supply, of which the Q-enhanced LC resonator consumes 12 mA.

V. Conclusions

An integrated second-order LC bandpass $\Delta\Sigma$ modulator implemented in a 0.5-μm bipolar technology was demonstrated for digitizing 950-MHz RF/IF signals. The input transconductor and the feedback transconductor of the active Q-enhanced LC filter were designed using the multi-tanh technique and the diode linearization technique, respectively. The modulator chip achieved 8-bit resolution (or 49 dB SNDR) over a 200-kHz bandwidth and consumed 135 mW for a 5-V supply. It demonstrates the feasibility of bandpass A/D conversion using on-chip inductors. SNDR is limited by an alias of a third harmonic, which may be due to transconductor nonlinearity. A redesign to move the input frequency away from $f_s/4$ might mitigate this by moving the aliased harmonic out of band, but the closely related third-order intermodulation products would remain a problem. The "noise" component is about 9 dB worse than in simulation, and we are still investigating possible causes.

It can be expected that the second-order modulator performance can be improved by: 1) using two return-to-zero DAC pulse feedback loops, perhaps one without delay and another one with one-quarter-clock delay; 2) adding another nonreturn-to-zero delay DAC loop if the technology is not fast enough; and 3) improving the active-LC filter linearity. For commercial application, it would be necessary to design the modulator in a higher order form. We have designed two fourth-order integrated LC bandpass modulators in a faster 0.5-μm SiGe HBT technology.

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