Signal-dependent timing jitter in continuous-time ΣΔ modulators

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A previously unpublished mechanism of signal-to-noise ratio (SNR) loss specific to continuous-time ΣΔ modulators is illustrated. It arises from increased quantiser resolution time for small-amplitude quantiser inputs, and is related to metastability.

Clock jitter in ΣΔ modulators: In sampled-data systems, a time jitter in the sampling clock ('sampling jitter' or 'clock jitter') leads to non-uniform sampling, which adds noise to the sampled signal. A clock jitter in Nyquist-rate analogue-to-digital converters (ADCs) thus leads to a loss in the SNR (signal-to-noise ratio) and hence in the converter resolution [1]. Likewise, a sampling jitter in a discrete-time ΣΔ ADC increases the total error power in the quantiser output [2]. For a sampling time deviation which is an uncorrelated Gaussian process with variance σ_j^2, this power is proportional to σ_j^2/OSR^2, where OSR is the oversampling ratio; in comparison, the quantisation noise power for an order-M converter is inversely proportional to OSR^{2M+1}. The tolerable level of clock jitter decreases with increasing OSR, since eventually jitter noise power will exceed quantisation noise power.

ΣΔ modulators that employ continuous-time circuitry [3, 4] are popular for high speed applications. A typical continuous-time design is depicted in Fig. 1, which is similar to that in [5]. Its feedback DACs convert voltage to current pulses which remain at a constant level throughout a clock period. In such circuits, the integral of the current over the clock period determines modulator behaviour, and this integral varies linearly with timing variations, i.e. clock jitter. In contrast, in a typical discrete-time, e.g. switched capacitor (SC), design, the variation in the amount of charge transferred per clock cycle due to the clock jitter is relatively low because the majority of the charge is transferred at the beginning of a clock period. Hence, continuous-time designs are more sensitive to clock jitter than SC designs [6].

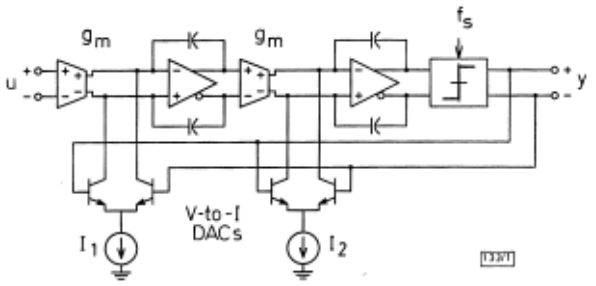

Fig. 1 *Second-order continuous-time ΣΔ modulator*

Jitter due to small quantiser inputs: Even with a perfectly uniform sampling clock, an insidious type of timing jitter can creep into a design, such as that of Fig. 1. The one-bit quantiser operates as a voltage comparator with a reference level of zero. A non-negative quantiser input voltage produces a +1 output whence a positive full-period current pulse emanates from the one bit DACs, while a negative input produces a –1 output and a negative DAC current pulse.

Ideally, the comparator would make a decision a fixed amount of time after the sampling clock edge. However, a practical comparator has a finite gain, hence very small comparator inputs lead to a longer time before the output switches fully to ±1. We define 'loop delay' as the length of time between the sampling clock edge and the DAC current pulse edge. Fig. 2 shows the loop delay against comparator input voltage magnitude for a transistor-level simulation of the circuit in Fig. 1 designed to operate with a 1GHz sampling clock. Indeed, loop delay is constant for large inputs, but rises for increasingly small inputs.

The quantiser input has a zero-mean Gaussian-type shape [2] for modulators of order 2 and above. For these modulators, the quantiser input is essentially uncorrelated with the overall circuit input and appears 'random'; thus, quantiser inputs near 0V will occur at times that appear random. Since 'jitter' usually implies a random error, it is appropriate to denote the variable loop delay due to variable quantiser decision time as a 'signal-dependent timing jitter'. This is a subtle manifestation of the classic metastability problem in digital latches.

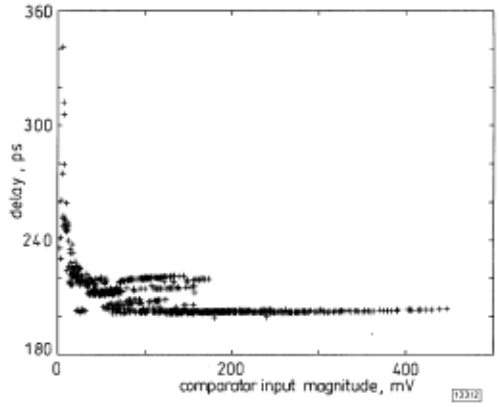

Fig. 2 *Quantiser delay against quantiser input*

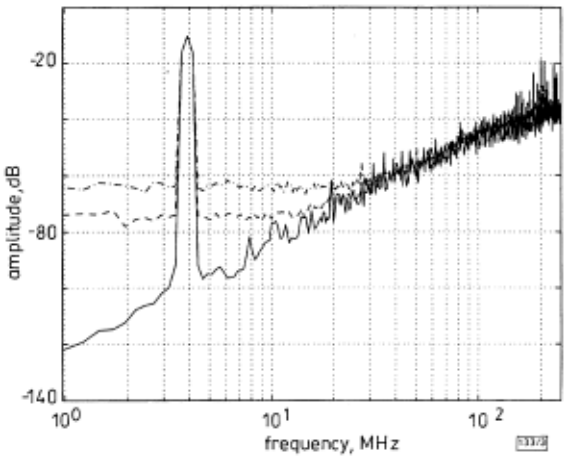

Fig. 3 *Output bit stream periodograms*

——— fixed quantiser delay
– – – – quantiser with some signal-dependent jitter
–·–·–·– quantiser with more signal-dependent jitter

Impact on SNR: Fig. 3 shows the effect of this type of jitter on the noise-shaping behaviour of a ΣΔ modulator. A computer program that implements Fig. 1 mathematically was employed, with the quantiser delay modelled as

$$\text{delay} = d_0 + \frac{d_1}{|v_{in}|^{x_1}} \qquad (1)$$

where v_{IN} is the quantiser input voltage and d_0, d_1, and x_1 are parameters. For the curve in Fig. 2, estimated values are d_0 = 200ps, x_1 = 2, and d_1 = 0.2ps · V². 32 averaged Hanning-windowed 4096-point periodograms of the output bit stream are shown in Fig. 3 for these parameter values, plus two additional cases: d_1 = 0 and d_1 = 20ps · V². d_1 = 0 corresponds to a quantiser with a fixed (unjittered) delay; the SNR for an OSR of 64 is 77.4dB. The other two cases correspond to a quantiser with a signal-dependent jitter. The spectrum becomes flat (white) at DC; while a finite op-amp gain could also cause this, the spectrum would exhibit greater harmonic content in that case. The SNRs are 55.7 and 45.0dB for d_1 = 0.2 and d_1 = 20, respectively. Clearly, signal-dependent jitter is detrimental to converter resolution.

Circumventing the problem: One or more pre-amplification stages could be inserted immediately prior to the quantiser, or the quantiser gain itself could be increased, reducing the probability of the quantiser input being too close to zero to resolve quickly. Or, as in [5], a latch might be inserted between the quantiser output and the DACs. This latch could be clocked, for example, one half sample after the quantiser, which gives the quantiser up to half a sample to settle. The DAC current pulse edge would then depend only on the jitter in the latch clock.

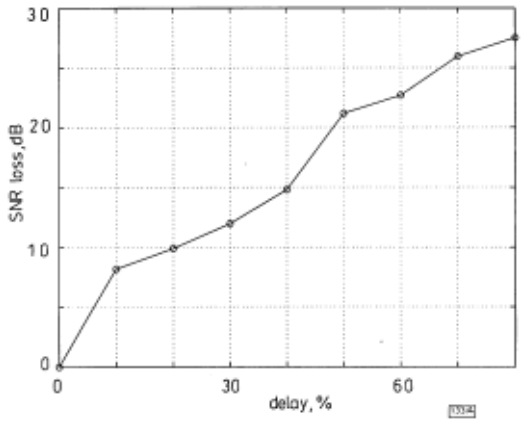

Fig. 4 *Effect of loop delay on SNR*

The problem with either method, or even both combined, is that increasing the loop delay, even by a fixed amount, is detrimental to the SNR [3]. Fig. 4 shows how much the SNR is lost against fixed quantiser delay for the circuit of Fig. 1, where the delay is expressed as a percentage of the sampling clock period and the OSR is 64. It is seen that a latch that introduces half a sample delay, as was apparently implemented in [5], leads to an SNR loss of 21dB. It may be that a signal-dependent jitter causes less SNR loss than introducing a fixed loop delay; a compromise that depends on the architecture and system parameters must usually be sought.

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