On the Design of a Fourth-Order Continuous-Time *LC* Delta–Sigma Modulator for UHF A/D Conversion

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***Abstract*—We consider the design and test of a fourth-order bandpass delta-sigma modulator ($\Delta\Sigma$M) for conversion of UHF analog signals to the digital domain for heterodyning and processing there. A prototype modulator in 0.5-μm SiGe [1] presented in the second part of the paper achieved 40 dB of dynamic range in a 20-MHz bandwidth centered at 1 GHz and consumed 450 mW from a single 5-V supply. At the time this modulator was designed, no explicit design procedure to achieve a certain modulator performance level had been established. The first part of this paper, therefore, is devoted to explaining the tradeoffs involved in choosing the parameters for a gigahertz-clocking transconductor/*LC* -based $\Delta\Sigma$M and formulating such an explicit design procedure. Finally, we elucidate some further design considerations, redesign the prototype to improve its simulated performance, and discuss lthe general appropriateness of high-speed continuous-time $\Delta\Sigma$M for UHF analog-to-digital conversion.**

***Index Terms*—Analog-to-digital converters, continuous-time systems, delta-sigma modulation.**

I. Introduction

DELTA-SIGMA modulation ($\Delta\Sigma$M) [2] has proved valuable in relatively narrowband (less than 100 kHz), high-resolution analog-to-digital conversion (ADC) applications, such as digital audio converters [3], [4]. Recent years have seen an increasing interest in using $\Delta\Sigma$M for conversion of wider bandwidths (a few megahertz and more). At practical oversampling ratios (OSR's), this necessitates clocking the modulators at a few hundred MHz or more, which in turn requires that the modulators' loop filters be built as continuous-time (CT) circuits (e.g., using transconductors and integrators) [5], [6] rather than discrete-time circuits (e.g., switched capacitor) where op-amp bandwidths and settling-time constraints limit the maximum clocking rate.

A few recent papers [1], [7]–[9] have investigated the use of CT $\Delta\Sigma$M bandpass (BP) converters for digitization of a VHF or UHF signal at an intermediate frequency (IF) in a radio receiver. A typical architecture of such a receiver appears in Fig. 1. After a stage of analog amplification and mixing, the entire IF band is digitized and mixed down to baseband, and the spectrum is filtered and the signal details sorted out using DSP. There is particular interest in using a modulator with a sampling rate f_s of four times the IF because the mix to baseband then becomes particularly simple in the digital domain, as the diagram illustrates. This architecture is akin to a direct-conversion receiver [10], only better in that it avoids the self-mixing problem associated with such circuits.[1]

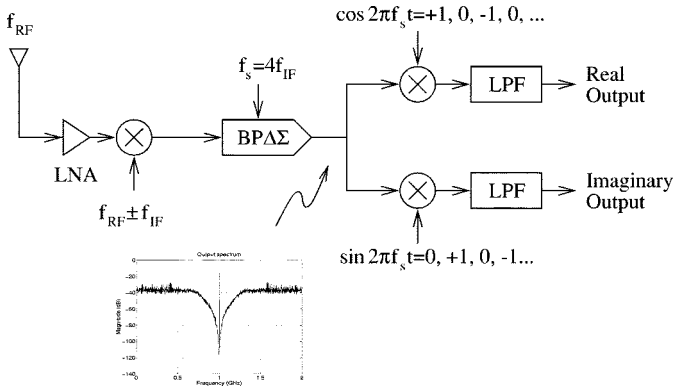

Fig. 1. Typical radio receiver application for a BP $\Delta\Sigma$M.

Test results on these modulators have yielded somewhat disappointing performance: ADC's with bandwidths of 20–25 MHz have achieved resolutions of only 6–7 bits, not nearly enough to meet the high dynamic range (DR) requirements of many radio applications. The problem is not with the order of modulator chosen: [1], [7], [8] are fourth-order BP $\Delta\Sigma$M's clocking at 3–4 GHz, which can theoretically achieve 12-bit resolution in a bandwidth of $f_N = 25$ MHz. A $\Delta\Sigma$M uses its loop filter to "shape" the quantization noise away from the band of interest; in this manner, a doubling of $\mathrm{OSR} \equiv f_s/(2 \cdot f_N)$ achieves much more than the mere 3-dB improvement in DR which would result if the in-band noise were white. In practice, most gigahertz-speed modulators achieve noise shaping only up until an OSR of approximately 15 [6, Table 3.2], whereupon the in-band noise becomes white rather than shaped and the advantage of oversampling further is greatly reduced. This in-band white noise is the cause of the poor performance of published modulators to date.

The authors presented test results on a prototype SiGe HBT BP modulator which clocks at $f_s = 4$ GHz for conversion of 1-GHz IF signals [1]. A block diagram of the circuit appears in Fig. 2. An input voltage is fed through a transconductor G_g,

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[1]Nonlinearities which generate third-order harmonics at $3f_s/4$, which alias in-band to $f_s/4$, are nonproblematic in a CT $f_s/4$ DSM; tones at $3f_s/4$ are greatly attenuated both by the internal modulator resonators and by the antialiasing inherent in CT modulators [5].

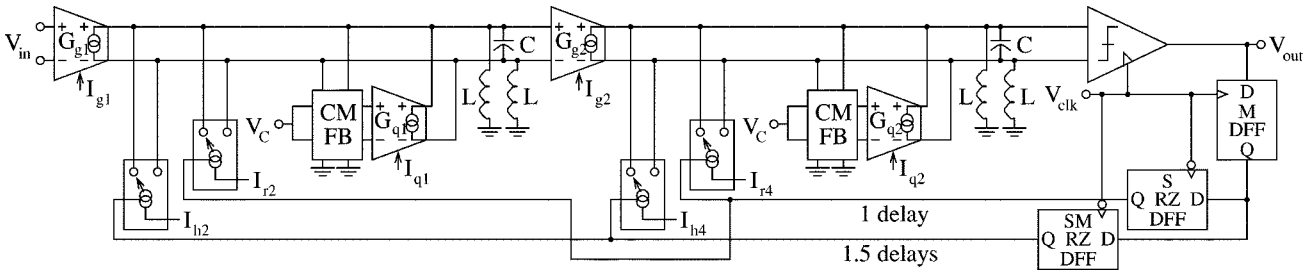


Fig. 2. A 4-GHz fourth-order BP CT $\Delta\Sigma$M.

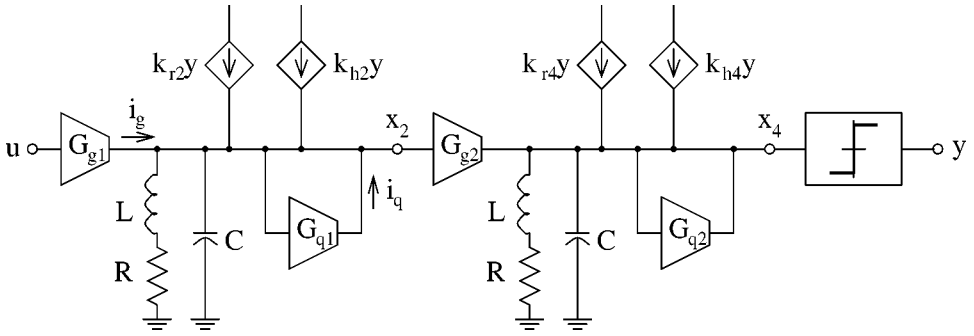


Fig. 3. Approximate single-ended model for modulator.

which produces a current $i_g = G_g v_i$ to drive an on-chip parallel LC tank. This gives the tank output voltage v_o a bandpass shape:

$$V_o = I_G Z_{LC} = \frac{G_g V_i}{sC + 1/sL} = \frac{(G_g/C)s}{s^2 + 1/LC} V_i. \qquad (1)$$

This is a second-order transfer function, so the series connection of two resonators yields a fourth-order modulator. The integrated inductor has a poor quality factor Q_L, so a Q-enhancement transconductor G_q is connected as a negative resistor to cancel the positive resistance of the inductor. Both the gain A_0 and the Q of the resonator $Q_{\rm res}$ are tunable. The quantizer and latches are such that this is a so-called one digital delay multifeedback architecture [5], and the feedback operates via current-summing with simple tunable current-switching DAC's.

At the time this modulator was designed, we did not have a rigorous procedure for how to choose the component values. The first goal of this paper is to rectify this. We have since developed a design procedure for this type of modulator which formalizes the selection of, and explains the tradeoffs among, circuit component and design parameter values. Our second goal is to present more detailed test results than were given in [1], which yields insight into other aspects of the design and test of such modulators. Our final goal is to draw from our derivations and experience to discuss in general the practicality of high-speed $\Delta\Sigma$M for UHF ADC in radios.

The remainder of the paper is organized as follows. Section II states the design problem we are trying to solve and makes some preliminary observations. The next four sections explore the relationship between component values and performance, each concentrating on a particular part of the modulator: the input transconductor in Section III, the resonator components and positive-feedback transconductors in Section IV, the DAC currents and interstage transconductor in Section V, and the effect of transconductor nonlinearity in Section VI. Section VII summarizes the design procedure, while Section VIII describes our fabricated circuit in detail and presents some interesting and useful test results. Section IX comments on our test results and gives some specific design improvements for better performance. Finally, Section X discusses the merits of UHF ADC using CT $\Delta\Sigma$M's.

II. Design Problem Statement

Let us begin with a discussion of how to choose component values in a fourth-order $f_s/4$ BP design. A simplified single-ended model of our modulator appears in Fig. 3. The design problem may be stated as follows. Given that we desire a certain center frequency, OSR, and SNR, how do we choose the parameters L, C, R, G_g, G_q, k_2, and k_4? We make the following initial comments.

- To simplify our discussion we assume resonator L and C are identical in both stages. There is no particular need for this to hold in general.
- One way to provide a sufficient number of degrees of freedom in the implementation of a given noise-shaping transfer function is to use two kinds of feedback DAC with separately-tunable pulse amplitudes [6, Ch. 2], as we did in the prototype. We assume the presence of two DAC's, and we define

$$k_2 \equiv k_{r2} + k_{h2}, \quad k_4 \equiv k_{r4} + k_{h4} \qquad (2)$$

i.e., the single feedback coefficients in Fig. 3 are found by summing the amplitudes of the two DAC currents that feed back to the same place.

The selection of the modulator parameters is done by considering four main areas.

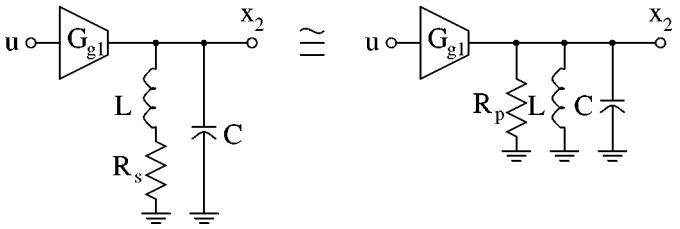


Fig. 4. Series/parallel tank equivalence near resonance.

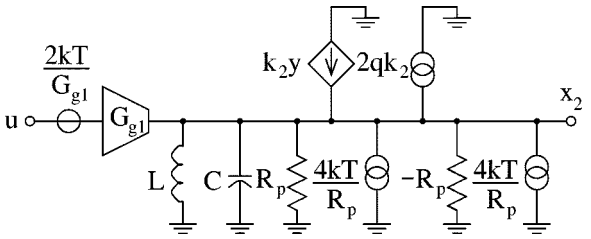


Fig. 5. Input transconductor equivalent circuit for noise considerations.

1) The input transconductor (Section III) determines to a large extent the overall modulator DR. We derive expressions for the dynamic range of this transconductor in terms of its input-referred noise voltage and linearity.
2) The tank components and G_q (Section IV) are chosen based on the desired center frequency, inductor Q, and die area.
3) The feedback DAC currents (Section V) must be selected to give the correct modulator noise-shaping characteristic and resonator node voltage scaling.
4) Nonlinearity of the transconductors other than the input transconductor (Section VI) leads to the folding of out-of-band noise into the signal band, and so must be controlled.

We consider each of these areas in turn.

III. Input Transconductor G_{g1}

Many published high-speed modulators, this one included, operate predominantly in current mode. The input transconductor G_{g1} is a separate circuit that is not really part of the design flow. However, overall modulator dynamic range can be no better than the DR of G_{g1} [11], [12]. The minimum modulator input voltage $u_{\min}$ is in large part determined by the input-referred noise of G_{g1}, while the maximum voltage $u_{\max}$ is constrained by its linearity. Obtaining a high-enough DR from G_{g1} is a circuit-design problem that is beyond the scope of this paper. Our interest here is to derive approximate expressions for $u_{\min}$ and $u_{\max}$ in terms of other parameters.

Let us begin with $u_{\min}$. We employ a series/parallel tank transformation as follows. The resistor R_s on the left of Fig. 4 represents the finite Q_L of the inductor

$$Q_L = \omega_0 L/R_s. \tag{3}$$

It can be shown [13, Sec. 4.4], that over a suitably restricted frequency range near resonance, the series LR circuit with a parallel C is approximately equivalent to a purely parallel RLC circuit as on the right of Fig. 4 when

$$R_p = R_s\left(Q_L^2+1\right), \quad L_p = L_s\left(\frac{Q_L^2+1}{Q_L^2}\right). \tag{4}$$

This is useful because in a parallel RLC circuit, the impedances of L and C cancel at resonance, leaving only R_p. Next, we assume that G_{q1} is tuned such that it makes a resistance $-R_p$ to ground as depicted in Fig. 5. We would tune G_{q1} this way because at resonance, the positive and negative R_ps cancel, which means we will have an infinite resonator Q. Ideally, this leads to an infinitely deep notch in the quantization noise and thus good converter resolution. It now becomes possible (Fig. 5) to write simplified expressions for the noise currents of each resistor and the feedback DAC.

Each resistor R_p and $-R_p$ has a noise current density $4kT/R_p$ A^2/Hz. If we assume the DAC is a bipolar transistor with collector current $I_c = k_2$, its noise-current density term will be of the form $2qk_2$ A^2/Hz [14, Ch. 11], assuming collector current shot noise dominates other noise sources such as base current and extrinsic base resistance. All these currents can be seen to drive node x_2 from ground, and therefore they may be referred to the modulator input by dividing them by G_{g1}^2, whence they become noise *voltage* densities. The input transconductor itself has a certain input-referred noise voltage density, and if we assume once again that it is a bipolar-based circuit, we may write its noise-voltage density as $2kT/G_{g1}$ V^2/Hz.

All the noise voltages at the input are uncorrelated, so we add them to get a total input noise voltage density of

$$\overline{v_{ng1}^2} = \frac{2kT}{G_{g1}} + \frac{2qk_2}{G_{g1}^2} + \frac{8kT\omega_0 C}{G_{g1}^2 Q_L} \text{ V}^2/\text{Hz} \tag{5}$$

where we have used the fact that $R_p \equiv Q_L/(\omega_0 C)$ and have assumed the noise is white in the (narrow) signal band. The total in-band noise voltage is, by definition, the minimum detectable signal

$$u_{\min} \equiv \sqrt{\overline{v_{ng1}^2} \times \frac{f_s}{2\cdot \text{OSR}}}. \tag{6}$$

Immediately, we see from (5) that in order to be able to detect small signals, we wish for G_{g1} to be *large*. Our first design constraint, therefore, is to make G_{g1} "large enough" to have small in-band noise. G_{g1} is proportional to current; as is often the case, high DR requires high power dissipation.

The maximum input signal $u_{\max}$ is constrained by the required modulator SNR. Clearly

$$u_{\max} = u_{\min} \times 10^{\text{SNR}/20} \tag{7}$$

which in turn determines the linearity of G_{g1}. Making the (reasonable) assumption that G_{g1} is a differential circuit with a weak cubic nonlinearity and an input–output description

$$i_{g1} = G_{g1}u - \epsilon_{g1}u^3 \tag{8}$$

then the input-referred third-order intercept point IIP_3 can be written[2]

$$\mathrm{IIP}_3 \quad \text{for } G_{g1} \equiv \sqrt{\frac{G_{g1}}{3\epsilon_{g1}}}. \tag{9}$$

The required linearity for G_{g1} is then straightforward to state in terms of $u_{\max}$ and SNR. At $u_{\max}$, we require harmonics caused by nonlinearity to be at least SNR dB below the fundamental. A simple geometrical argument [13, Sec. 6.6], says that we require

$$\mathrm{IIP}_3 \text{ for } G_{g1} = 20\log_{10} u_{\max} + \mathrm{SNR}/2 \text{ dB} \tag{10}$$

because the third harmonic has a slope of 3 dB/dB with u, while the linear term has a slope 1 dB/dB. All of this is useful when one has an actual transconductor circuit with a known dynamic range; (6), (7), and (10) can be used to see if its DR will impose an upper bound on overall modulator DR.

Although we have made a number of simplifying assumptions about the form of the transconductor circuit, it remains illustrative to write an expression for modulator SNR. We use the following fact. In order to keep the modulator stable, the feedback current must be at least as large as the maximum input current. Using (2), we may state

$$k_2 \geq u_{\max} G_{g1}. \tag{11}$$

Put another way, we require

$$u_{\max} \leq \frac{k_2}{G_{g1}} \tag{12}$$

where $u_{\max}$ is the full-scale input voltage in (7). Assuming we choose k_2 no larger than necessary, the inequality in (12) becomes an equality, and therefore, the signal power is $(k_2/G_{g1})^2$. Combining this with the expression for the integrated noise power in (6) and simplifying leads to

$$\mathrm{SNR}_{\max} = \frac{k_2^2}{kTG_{g1}f_N\left(1 + \frac{k_2}{i_{g1}} + \frac{4}{Q_L}\frac{\omega_0 C}{G_{g1}}\right)} \tag{13}$$

where f_N is the Nyquist bandwidth and we have used the fact that small-signal $g_m \equiv I_c/V_T$, and hence $G_{g1} = i_{g1}/(kT/q)$ for a bipolar transistor.

This expression shows that the noise is made up of the sum of three components. The one that dominates will depend on the actual design. One of the interesting insights this equation offers us is that even if G_{g1} and the DAC were noiseless, SNR would still be limited by finite Q_L. If Q_L is poor, then we need either high G_{g1} or low C to ensure that the third denominator term does not dominate; thus, poor inductor Q either increases our power dissipation or constrains our choice of capacitor size. Conversely, infinite inductor Q (i.e., $R_p \to \infty$) means our resonator components L and C are unconstrained from an SNR improvement point of view.

[2]Simply equating the two terms on the right-hand side of (8) yields (9) with no $\sqrt{3}$ denominator term, but this measures the third harmonic amplitude, which falls outside the signal band. The $\sqrt{3}$ is needed for the in-band intermodulation, which is the distortion component of concern in a BP $\Delta\Sigma$M.

IV. Tank Components and G_q

In order to explain how to choose L, C, and the G_q's, we write an expression for x_2 in Fig. 3. Assuming the G_{q1} transconductor draws negligible input current, we may write an equation for the Laplace transform of x_2

$$\begin{aligned} X_2 &= [I_g + I_q + k_2 Y]Z_{eq} \\ &= [G_{g1}U + G_{q1}X_2 + k_2 Y]\frac{1}{\frac{1}{sL+R} + sC}. \end{aligned} \tag{14}$$

Solving for X_2 gives

$$X_2 = [G_{g1}U + k_2 Y]\frac{\frac{1}{C}s + \frac{R}{LC}}{s^2 + \left(\frac{R}{L} - \frac{G_{q1}}{C}\right)s + \frac{1}{LC}(1 - RG_{q1})}. \tag{15}$$

A similar equation could be written for x_4 in terms of x_2 and the second resonator parameters. The center frequency of a biquadratic transfer function is determined by the coefficient of the s^0 term in the denominator; assuming for the moment that RG_{q1} is small, we arrive at the (unsurprising) design constraint

$$\omega_0 \approx \frac{1}{\sqrt{LC}}. \tag{16}$$

Choosing one of L or C then fixes the other according to (15). Usually, the inductor series resistance R is given once L is known because one has little control over integrated inductor Q. A deep noise-shaping notch requires a high-Q resonator; a rule of thumb that ensures adequate noise-shaping for negligible performance loss is [6, Sec. 3.1.1]

$$Q_{\mathrm{res}} \approx \mathrm{OSR}. \tag{17}$$

Integrated inductor Q's typically range from 5 to 10, and hence, for a typical OSR of 64, we require Q-enhancement of some kind. As we have said, this is provided by the G_{q1} transconductor. A high-Q biquad has a denominator s^1 coefficient of near zero; thus, in (14) we need

$$\frac{R}{L} - \frac{G_{q1}}{C} \approx 0. \tag{18}$$

G_{q1} may now be found because it is the only unknown in (17), and G_{q2} may be found in a similar manner.

What are some of the considerations for how we should choose L and/or C? Equation (13) shows that small C is good for noise. But smaller C means larger L, which for an integrated inductor means larger die area. Also, we can only reduce C so much before parasitics start to become significant relative to C—this could matter if C is tunable to counter process variations, and increased parasitics reduce the relative tuning range of ω_0. On the other hand, if Q_L is a function of L, then instead of choosing C, it may be more sensible to choose L so that Q_L is maximized.

V. Feedback DAC Currents and G_{g2}

Our choice of the feedback DAC k's and G_{g2} fixes two things: the modulator noise-shaping characteristic and the range spanned by the (stochastic) resonator voltage signals. We consider the former in this section. The latter affects the

linearity of the internal modulator transconductors (i.e., those other than G_{g1}), and we treat it in the following section.

In this paper, we are discussing the design of a fourth-order $f_s/4$ BP modulator with a full sample of delay in the feedback path. This has a discrete-time (DT) transfer function

$$H_{\rm BP}(z) = z^{-1}\frac{2z^{-1}+z^{-3}}{(1+z^{-2})^2} \tag{19}$$

which can be obtained by performing the substitution $z^{-1} \to -z^{-2}$ in the transfer function of a double-integration low pass modulator [5]. DT modulators can be transformed to an equivalent CT modulator [15], which for (18) yields [5]

$$\hat{H}_{\rm BP}(s) = \frac{-1.0354(sT_s)^3 + 1.0652(sT_s)^2 - 1.3210sT_s + 4.5661}{\left((sT_s)^2 + \left(\frac{\pi}{2}\right)^2\right)^2}. \tag{20}$$

Our design employs both return-to-zero (RZ) and half-delayed RZ (HRZ) DAC's to give us four individually-tunable coefficients, namely the DAC currents. This gives us exactly the right number of degrees of freedom to control the numerator of our CT filter $\hat{H}_{\rm BP}(s)$.

For an ideal CT modulator, the DAC levels required to implement (19) are known to be [6, eq. 4.26]

$$(k_{r2}, k_{r4}, k_{h2}, k_{h4}) = (-0.4502, -0.6339, 1.0868, 2.9874). \tag{21}$$

These are normalized for $T_s = 1$ and resonator numerators of $(\pi/2)s$, hence they must be scaled for the practical circuit. First, k_{r2} and k_{h2} are scaled by $(\pi/2)^2$ and the remaining k's are scaled by $\pi/2$; second, the effects of G_{g2}, C, and $T_s \neq 1$ are included, resulting in final scaled values of

$$(\bar{k}_{r2}, \bar{k}_{r4}, \bar{k}_{h2}, \bar{k}_{h4}) = \left(-1.1107\frac{C}{G_{g2}T_s}\frac{C}{T_s}, -0.9957\frac{C}{T_s}, +2.6815\frac{C}{G_{g2}T_s}\frac{C}{T_s}, +4.6927\frac{C}{T_s}\right) \tag{22}$$

(the reason for the bars over the names will be explained in the next section). These k's have units A/V, which (as expected) give currents when multiplied by the ± 1-V quantizer output. C and T_s have already been determined, so $\bar{k}_{r4}$ and $\bar{k}_{h4}$ are calculable from (21). Moreover, the sum $\bar{k}_2 \equiv \bar{k}_{r2} + \bar{k}_{h2}$ is known from (11). The only remaining unknown is thus G_{g2}, which is found to be

$$G_{g2} = \frac{\pi/2}{\bar{k}_2}\frac{C^2}{T_s^2}. \tag{23}$$

The design is now almost complete, save the second issue above: the linearity of the internal modulator transconductors.

VI. Linearity of Internal Transconductors

When the modulator is operating, the voltages at x_2 and x_4 are stochastic in nature with approximately Gaussian distributions [16]; let us denote their standard deviations σ_{x_2} and σ_{x_4}. It is not difficult to see that these values are directly proportional to the feedback current levels: driving more DAC current into x_2 and x_4 produces proportionally more voltage across the (fixed) tank impedance. If we simulate the ideal modulator in (19) with the DAC currents scaled as in (21) and zero input voltage, we find

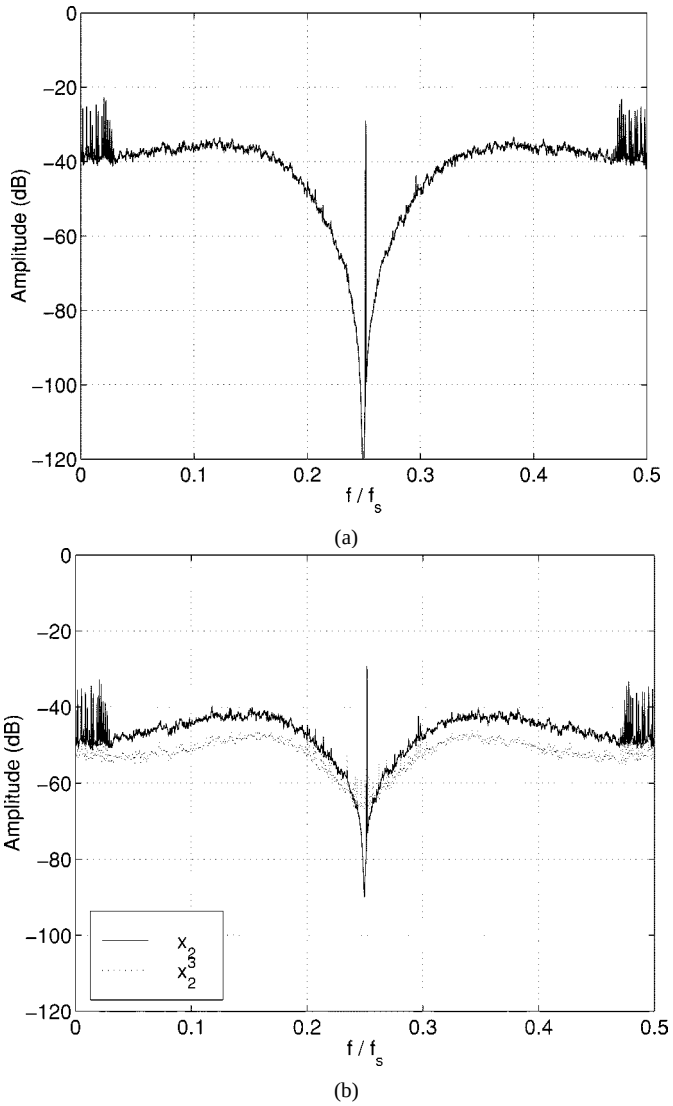


Fig. 6. Spectrum of (a) y and (b) x_2 and x_2^3.

$$(\sigma_{x_2}, \sigma_{x_4}) \approx \left(\frac{1}{\sqrt{2}}\frac{C}{G_{g2}T_s}, 1.157\right) \text{ V}. \tag{24}$$

$\sigma_{x_4} = 1.157$ V will, in many designs, overwhelm the linearity of G_{q2}, and σ_{x_2} in (23) will often do likewise to G_{q1} and G_{g2} for practical parameter values. It is thus preferable to scale all DAC currents by a parameter γ_k

$$(k_{r2}, k_{r4}, k_{h2}, k_{h4}) = (\gamma_k\bar{k}_{r2}, \gamma_k\bar{k}_{r4}, \gamma_k\bar{k}_{h2}, \gamma_k\bar{k}_{h4}) \tag{25}$$

and

$$G_{g2} = \frac{\pi/2}{k_2}\frac{C^2}{T_s^2}\gamma_k \tag{26}$$

where k_2 is from (11). This merely scales the transfer function in (19), which does not alter its noise-shaping characteristics, while simultaneously scaling resonator voltages

$$(\sigma_{x_2}, \sigma_{x_4}) \approx \left(\frac{1}{\sqrt{2}} \frac{C}{G_{g2} T_s} \gamma_k, 1.157 \gamma_k \right). \tag{27}$$

Therefore, γ_k lets us reduce voltage swings so as to meet any linearity requirements on G_{q1}, G_{g2}, and G_{q2}. The overbars in (21) are thus to denote nominal feedback levels; actual levels are found from (24).

Suppose these three transconductors have known IIP_3 with a form similar to (9). We normally think of linearity in terms of the harmonics produced in response to multiple sinusoidal inputs. Such thinking is not helpful here, because the internal transconductors are mainly driven by the modulator output (a wideband stochastic signal) rather than a sinusoid. Understanding the effect of nonlinearity is aided by writing out the time-domain differential equations (DE's) for the state variables.

For simplicity, assume G_{q1} is the only nonlinear transconductor and that $R = 0$. A second-order DE for x_2 can be written as two coupled first-order equations by introducing an auxiliary state variable x_1

$$\begin{aligned} \frac{dx_1}{dt} &= \frac{1}{LC} x_2, \\ \frac{dx_2}{dt} &= -x_1 + \frac{1}{C} \left[G_{g1} u + \epsilon_{q1} x_2^3 + k_2 y \right]. \end{aligned} \tag{28}$$

We divide the discussion into two cases.

1) Suppose first that $\epsilon_{q1} = 0$ (i.e., that G_{q1} is linear). The term inside square brackets in (27) for dx_2/dt then reduces to $[G_{g1}u + k_2 y]$. This term describes ideal modulator operation: the input u is combined with the fed-back output bit y, *and* the amplitude of u in the spectrum of y is determined from k_2/G_{g1} as in (12).
2) Now suppose there is no input ($u = 0$) and $\epsilon_{q1} \neq 0$ (G_{q1} is nonlinear). The square-bracketed term becomes $[\epsilon_{q1} x_2^3 + k_2 y]$. By analogy to the first case, the input u has been replaced with x_2^3; therefore, by analogy, we expect the spectrum of x_2^3 to appear in the spectrum of y with an amplitude related to the ratio k_2/ϵ_{q1}.

From theory, the spectrum of $x_2(t)^3$ is $X_2(s) * X_2(s) * X_2(s)$, where the asterisk denotes convolution. Simulated spectra of y, x_2, and x_2^3 appear in Fig. 6. We observe that x_2 has a noise-shaped look similar, but not identical, to that of the output bit stream y. The convolution causes folding of some of the out-of-band noise into the signal band, but how much?

We can answer that question with the help of normalization. If we simulate the modulator and plot its DR and peak SNR, $\mathrm{SNR}_{\max}$ as a function of normalized ϵ_{q1}

$$\bar{\epsilon}_{q1} \equiv \frac{\epsilon_{q1} \sigma_{x_2}^3}{k_{r2} + k_{h2}} \tag{29}$$

the graphs appear as in Fig. 7(a) and look the same for a given OSR. The form of $\bar{\epsilon}_{q1}$ is logical given (27) and case 2 above. Similar normalizations can be found for the other two nonlinear parameters

$$\bar{\epsilon}_{g2} \equiv \frac{\epsilon_{g2} \sigma_{x_2}^2}{G_{g2}} \tag{30}$$

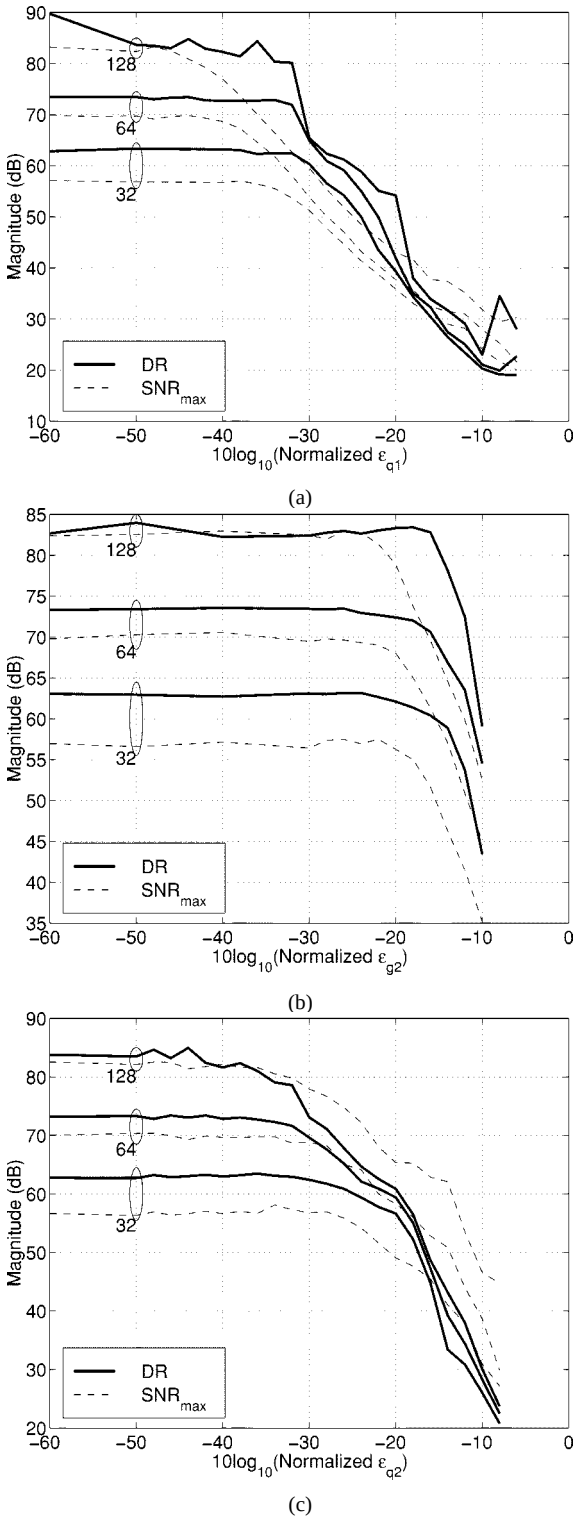


Fig. 7. DR and SNR_{max} for (a) $\bar{\epsilon}_{q1}$, (b) $\bar{\epsilon}_{g2}$, and (c) $\bar{\epsilon}_{q2}$. Numbers on curves are OSR values.

$$\bar{\epsilon}_{q2} \equiv \frac{\epsilon_{q2} \sigma_{x_4}^3}{k_{r4} + k_{h4}}. \tag{31}$$

Graphs of DR and $\mathrm{SNR}_{\max}$ are plotted in Fig. 7(b) and (c). From these graphs, we may derive the following rules of thumb for the

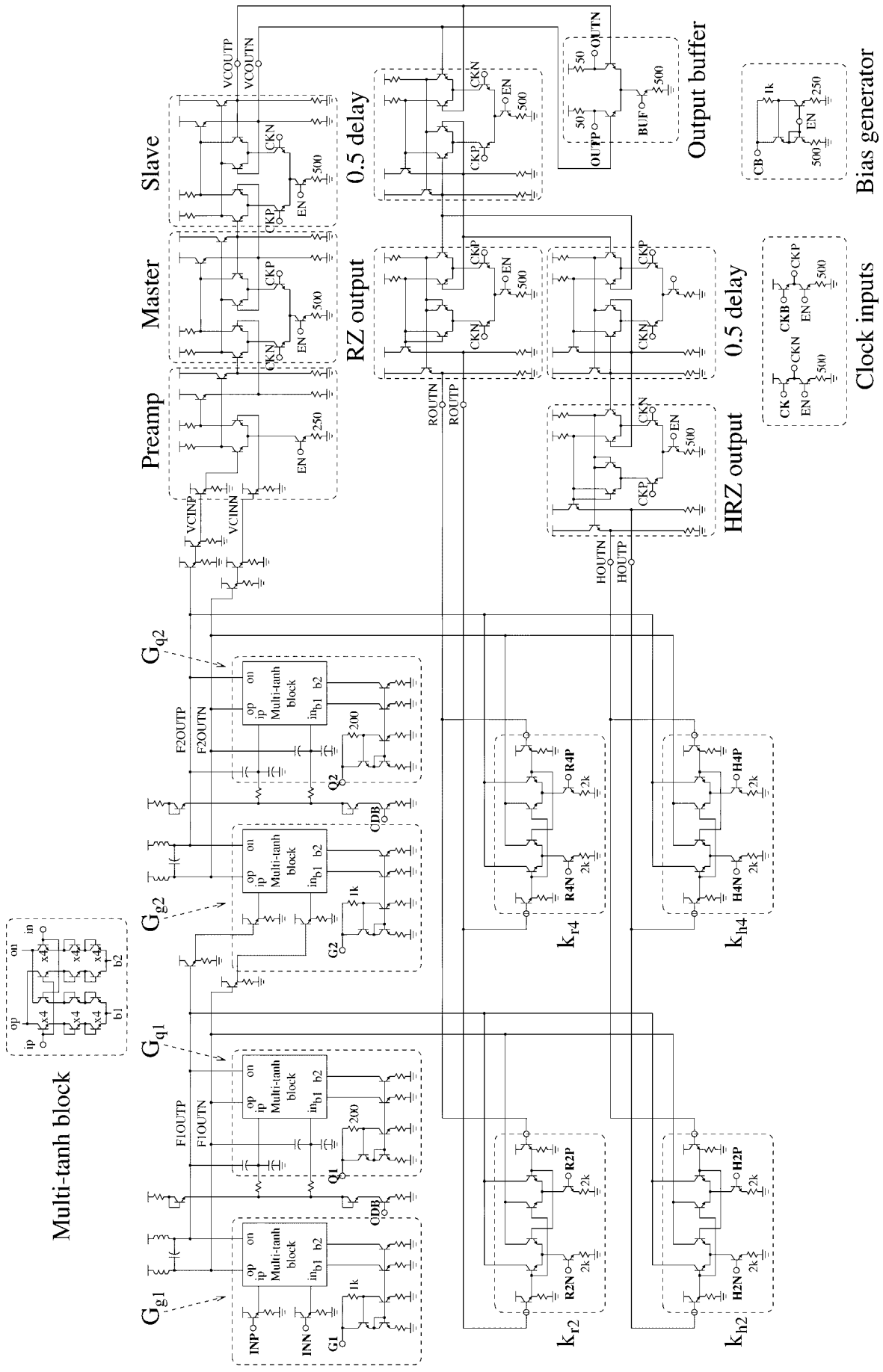


Fig. 8. Complete transistor-level schematic.

restrictions on the $\bar{\epsilon}$'s for each internal transcondcutor that will not affect DR significantly:

$$\bar{\epsilon}_{q1} < 10^{-3}, \quad \bar{\epsilon}_{g2} < 10^{-2},$$
$$10\log_{10}\bar{\epsilon}_{q2} < -5 - \log_2 \mathrm{OSR}. \tag{32}$$

The final portion of the design procedure can now be described. The nominal feedback $\bar{k}$s and signal levels σ_x's are found from the other known parameters by using (25) for G_{g2} followed by (24) and (26), where to start we assume $\gamma_k = 1$. The IIP_3's for the internal transconductors are characterized, and the normalized $\bar{\epsilon}$'s are calculated using (28)–(30). If they are large enough to violate (31), then γ_k can be lowered, which will lower the $\bar{\epsilon}$'s by a factor of γ_k^2.

We should also keep in mind that we can also alter the signal levels σ_{x_2} and σ_{x_4} by altering the tank impedance, if for some reason changing γ_k is found to be unsatisfactory. This will require iteration in the procedure, but such iteration will likely be required in other parts of the procedure anyway.

VII. Design Procedure Summary

We summarize the salient points of our design method here. Take as given center the frequency f_0 ($f_0 = \omega_0/2\pi = f_s/4$), SNR (assumed for simplicity equal to DR), and conversion bandwidth $f_N/2 = f_s/(2\cdot\mathrm{OSR})$. For the input transconductor:

- design the circuit and find the achieved G_{g1} and ϵ_{g1} in (8);
- use SPICE to find the total input-referred noise voltage over the Nyquist band;
- calculate $u_{\min}$ from (6), $u_{\max}$ from (7);
- ensure IIP_3 satisfies (10).

For the tank parameters:

- calculate the first feedback current k_2 from (11);
- calculate the LC product from (15);
- determine the inductor series resistance;
- calculate the required G_{q1} and G_{q2} from (17);
- with DAC and G_{q1} circuits present, resimulate input-referred noise in SPICE and ensure the input transconductor still has the necessary dynamic range.

For the feedback DAC levels and internal transconductors:

- calculate the required G_{g2} from (25);
- calculate the nominal $\bar{k}$s and σ_xs from (24) and (26) using $\gamma_k = 1$;
- design the other transconductors to meet G_q and G_{g2} specs and find the achieved ϵ_q and ϵ_{g2};
- calculate the normalized $\bar{\epsilon}$'s from (28) to (30);
- check if performance loss is significant with (31) and adjust γ_k and/or tank impedances.

As we have said, application of this procedure will involve a good deal of iteration. Moreover, we recommend SPICE or some other full-circuit simulator for noise measurements; our estimates in (5) and (13) are only very approximate.

VIII. A 4-GHz Fourth-Order Bandpass ΔΣM

A. Transistor-Level Schematic

Fig. 8 shows a complete transistor-level schematic of our fabricated fourth-order modulator with major blocks labeled. It was designed in a 50-GHz SiGe HBT process [17]. The transconductors are all multi-tanh circuits [18] which have much improved linearity over a simple differential pair while suffering only a small noise penalty. The output current of G_{g1} drives one LC resonator with $L = 3.5$ nH, $C = 6.1$ pF; the resonator output voltage is sampled with a capacitive divider and fed to G_{q1}. The second resonator stage drives a preamplifier with a gain of about six, which in turn drives the master stage of an M/S latch whose nominal clock speed is $f_s = 4$ GHz. Additional latching stages are inserted to provide the appropriate number of delays, and half-latches with RZ outputs are effected by an appropriate connection of the bases of the final differential pair. RZ and HRZ outputs drive current-switching DAC's whose output nodes also draw current from the resonators; feedback in this circuit works

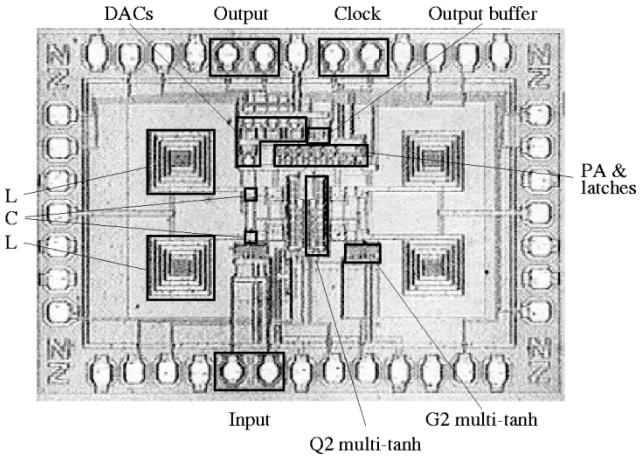


Fig. 9. Die photomicrograph of NRZ modulator.

TABLE I
Parameters for Fabricated Design

Tank element values		$L = 3.5$ nH
		$C = 6.1$ pF
		$R = 2.45\Omega$
G_g	Range	$2 \rightarrow 8$ mA/V
ϵ_g	Typical	9×10^{-3} mA/V^3
G_q	Range	$2 \rightarrow 9$ mA/V
	For $Q = \infty$, calc	4.3 mA/V
	For $Q = \infty$, meas	9.0 mA/V
ϵ_q	Typical	5×10^{-4} mA/V^3
k_r, k_h	Range	$0 \rightarrow 500$ μA
σ_{x_2}, σ_{x_4}	Range	$4 \rightarrow 12$ mV
$\overline{v_{ng1}}$	Calc (typical)	3.5 nV/$\sqrt{\mathrm{Hz}}$
	Sim (typical)	20 nV/$\sqrt{\mathrm{Hz}}$
u_{min}	Typical	90 μV
G_{g1} IIP_3	Sim	-2.3 dBV
$\bar{\epsilon}_{q1}$	Maximum	$2.3 \times 10^{-6} = -56.4$ dB
$\bar{\epsilon}_{g2}$	Maximum	$1.8 \times 10^{-4} = -38.5$ dB
$\bar{\epsilon}_{q2}$	Maximum	$2.6 \times 10^{-6} = -55.8$ dB
SNR limit	u_{min}, IIP_3	52 dB

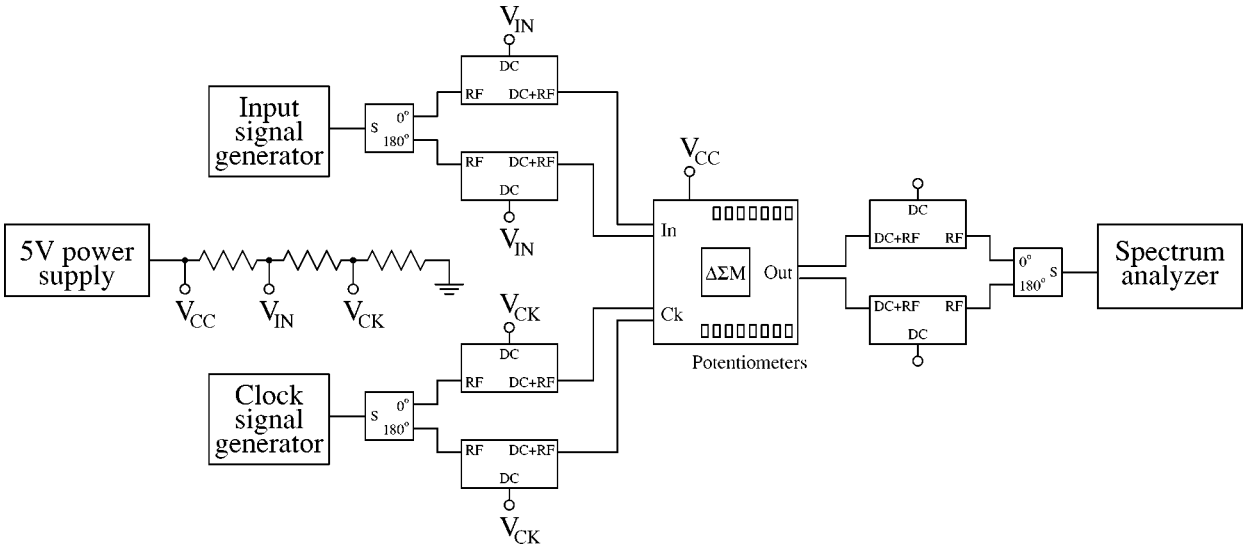


Fig. 10. Measurement test setup.

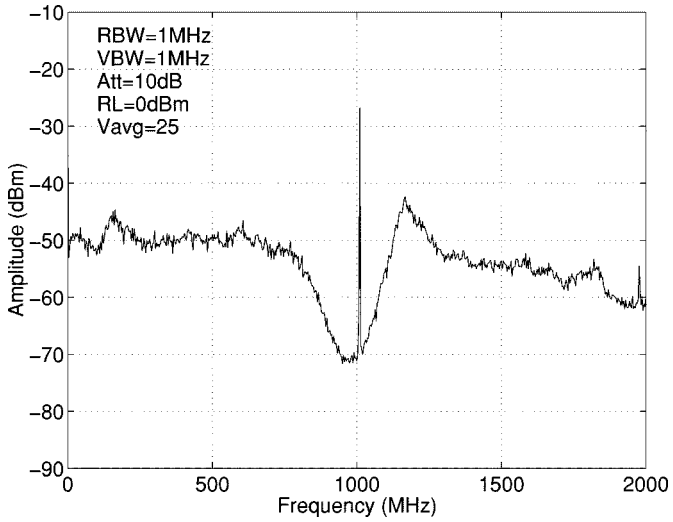


Fig. 11. Output spectrum plot.

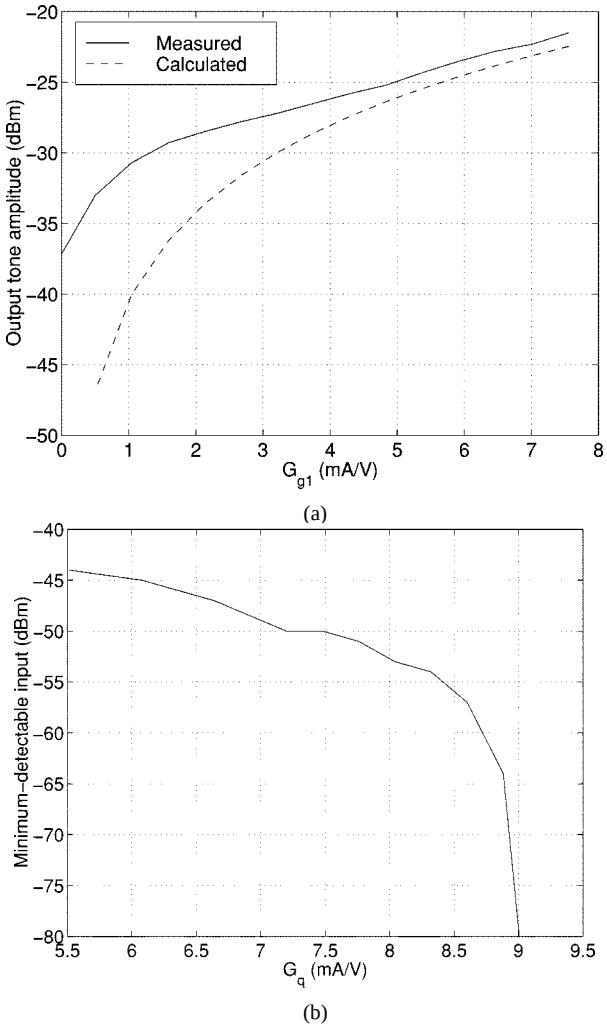


Fig. 12. (a) Tone magnitude in output spectrum against G_{g1}. (b) Minimum-detectable input magnitude against G_q.

by current summing. A die photomicrograph appears in Fig. 9; the complete circuit measures 2.40×1.65 mm^2 including the pads.

As noted in the Introduction, this circuit was designed long before the procedure in Section VII was formalized. We have nonetheless calculated its parameters as defined in Section VII for a bandwidth of 20 MHz in Table I, which corresponds to an OSR of 100. Worthy of mention are the following points.

1) SPICE measures typical in-band noise voltage densities of 20 nV/$\sqrt{\text{Hz}}$, but our approximate formula (5) is too optimistic: It predicts 3.5 nV/$\sqrt{\text{Hz}}$. This is hardly surprising since the formula was based on one transistor and no base-resistance noise, neither of which is true in our circuit. SPICE *does* validate the assumption that the noise is white across the signal band. Moreover, the general trends implied by (5) are found to hold true in SPICE (e.g., raising G_{g1} lowers the total in-band noise).
2) The swings at the resonator outputs σ_{x_2} and σ_{x_4} can be made only as large as about 12 mV because the DAC currents were chosen very small in this design. As a result, when we find the normalized $\bar{\epsilon}$ values and compare them

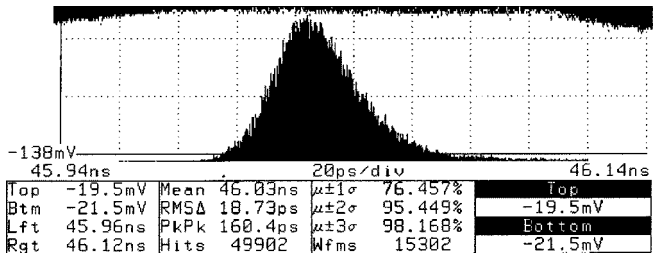


Fig. 13. Histogram of time-domain output bit zero crossings.

to (31), it happens that none of them are large enough to affect DR appreciably at $\mathrm{OSR} = 100$.

3) The 20 nV/$\sqrt{\mathrm{Hz}}$ input-referred noise for G_{g1} in a 20-MHz bandwidth gives a minimum-detectable input signal of $u_{\min} = 90\ \mu$V. The linearity of that transconductor is such that $\mathrm{IIP}_3 = -2$ dBV or so, and calculation with (7) and (9) gives a maximum SNR of 52 dB.

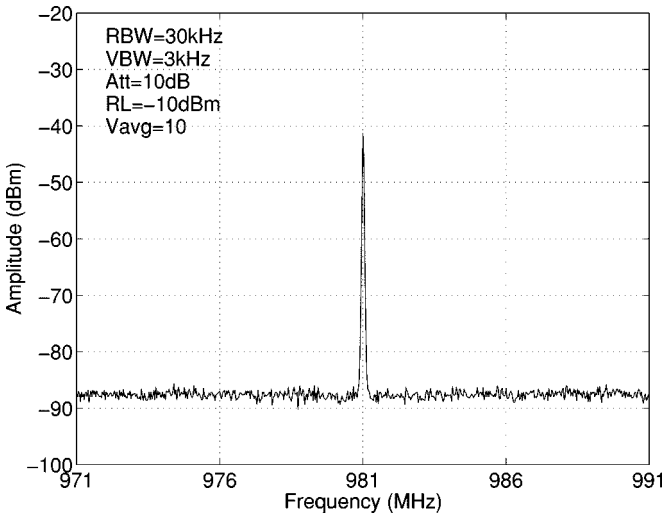
Thus, we predict at the outset that measurements will show this to be no better than about an 8-bit converter.

B. Test Results

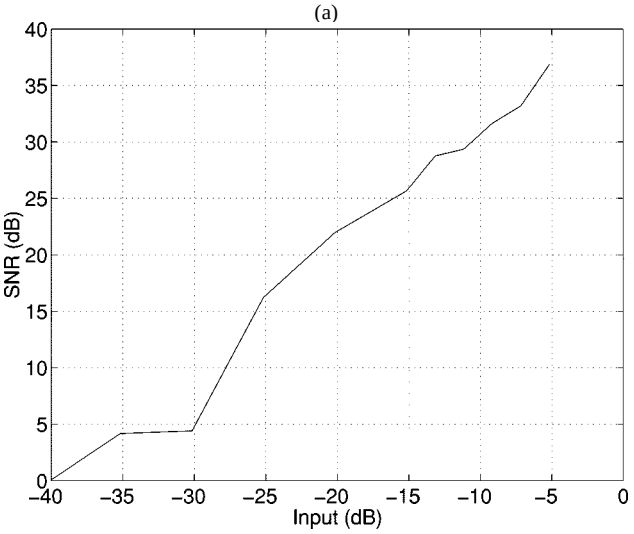
A block diagram of our test setup appears in Fig. 10. Input and clock signals were driven onto the board through power splitters. Common-mode levels were set off-chip with a single supply and resistive divider driving bias tees. Chip dc biases to set parameters such as the transconductances G_g and G_q and DAC feedback currents were controlled with potentiometers on the printed circuit board to which the packaged chip was mounted. The output bit stream was driven directly onto a spectrum analyzer. We presented preliminary test results in [1], and detailed results appear in [6, Ch. 7]. Some highlights of our measurements are reproduced here.

A representative output spectrum from 0 to 2 GHz is plotted in Fig. 11. The modulator draws 90 mA from a single 5-V supply, and the noise-shaping notch at 1 GHz is evident. The slight spectral peak at about 1.15 GHz is caused by the particular settings of the feedback DAC's. Unfortunately, we were unable to test the $\Delta\Sigma$M's blocks (like the transconductors and latch) individually, but with some ingenuity, we can verify they are functioning as expected.

As an example, recall that both G_g and G_q are tunable in this design. From (11) and (12), we know that changing G_g will affect the full-scale input voltage, while from (14), G_q affects the noise notch depth, and hence the sensitivity of the modulator to small inputs. For an input tone fixed at 1.003 GHz and -26 dBm, the solid line in Fig. 12(a) plots the amplitude of the output tone at 1.003 GHz as a function of G_{g1}. With the help of SPICE, we can calculate the expected shape of the curve [6, Sec. 7.3.1]; the dashed line gives good agreement to the measured value. In Fig. 12(b), we plot the minimum-detectable input level as a function of $G_q = G_{q1} = G_{q2}$; lower G_q means a lower-Q resonator and a reduced ability to encode a small signal, and the graph follows this trend qualitatively at least. The measured value for which $Q_{\mathrm{res}} = \infty$ is $G_q = 9.0$ mA/V, but from (17) and the known component values we calculate the value to be $G_q = 4.3$ mA/V. The discrepancy is likely due to parasitic capacitance on the divider which feeds the G_q multi-tanh circuits in Fig. 8.



(a)



(b)

Fig. 14. (a) Measured in-band modulator spectrum. (b) Dynamic range plot.

TABLE II
MODULATOR PERFORMANCE SUMMARY

Process	0.5μm SiGe HBT
Die area with pads	2.4mm × 1.6mm
Die area without pads	1.6mm × 0.85mm
Supply voltage	5V
Sampling frequency	4GHz
Signal bandwidth	20MHz
Oversampling ratio	100
Dynamic range	40dB
Peak SNR	37dB
Peak SFDR	48dB
Power consumption	450mW

An important potential source of nonideality in a high-speed $\Delta\Sigma$M is metastability in the quantizer [19]. At a clocking instant, quantizer inputs near zero take longer to resolve than large inputs because the quantizer has a finite regeneration gain;

output edge transitions will be delayed at these instants, resulting in variable-width feedback DAC pulses. This has much the same effect as clock jitter: Out-of-band noise modulates into the quantization noise notch, degrading SNR. Fig. 13 shows a histogram of output bit-zero crossings made using a high-speed sampling oscilloscope, and evidence of metastability can be seen in the following asymmetry. The trailing histogram edge falls to zero more slowly than the leading edge. This histogram also indicates a relatively large amount of jitter in the output bit transitions. Considering only the left half of the distribution, we estimate a 1σ value of 12 ps, almost 5% of the 250-ps bit period. We comment further on this in the next section.

In terms of overall performance, jitter and metastability have a serious impact: the in-band quantization noise is unshaped and large [Fig. 14(a)]. A plot of SNR in a 20-MHz band versus input amplitude normalized to full scale yields the dynamic range plot in Fig. 14(b). Although it is not plotted past -5 dB, the SNR does in fact stay positive for inputs all the way up to 0 dB, but its harmonic content is strong and the curve falls off from its peak. From [6, Fig. 7.37b)], we estimate an IIP_3 for this modulator of $+1$ dBm $= -9$ dBV, 7-dB worse than simulation. Measured peak SNR is 37 dB at a -5-dB input level, and spurious-free DR here is 48 dB. Overall modulator DR is 40 dB, making this a 6.3-bit converter. Table II summarizes the measured modulator performance.

IX. Result Commentary

To some degree, we were hampered by the fact that during the design phase we did not anticipate how we would test this modulator. Circuit blocks were not broken out individually, and on-wafer test was infeasible, meaning package and board design had to be done carefully. Even without these problems, clock jitter appears to be the major limit to the observed performance. Unfortunately, we are unsure of the main reason for the observed jitter and poor performance [6, Sec. 7.4]. In fairness, it must be noted that a spectrum analyzer is not the best way to characterize the performance of a high-speed $\Delta\Sigma$M because it is sensitive to analog imperfections in the output bit stream waveform. Vastly preferable is to capture the high-speed bits themselves, either through a sampling scope capable of storing a large number of samples (say 32 ksamples or more), or through a custom circuit like a 16:1 demultiplexer, which would allow bits to be captured on a fast logic analyzer [11]. Using an FFT to find the spectrum would almost certainly yield higher SNR than is found on a spectrum analyzer.

Overall, we were pleased that our first-cut deisgn functioned, but we would make a number of changes in a redesign.

1) We would design appropriate impedance matching networks for both the input and clock.
2) Some degree of performance loss caused by quantizer metastability could be alleviated by taking the output bit from the one-sample delayed latch output rather than the M/S output as we did in our design. This would provide the regeneration of two additional half-latches, which would lead to less of a tail on the right side of the zero-crossing histogram in Fig. 13 and hence a somewhat lower white noise floor observed on a spectrum analyzer.

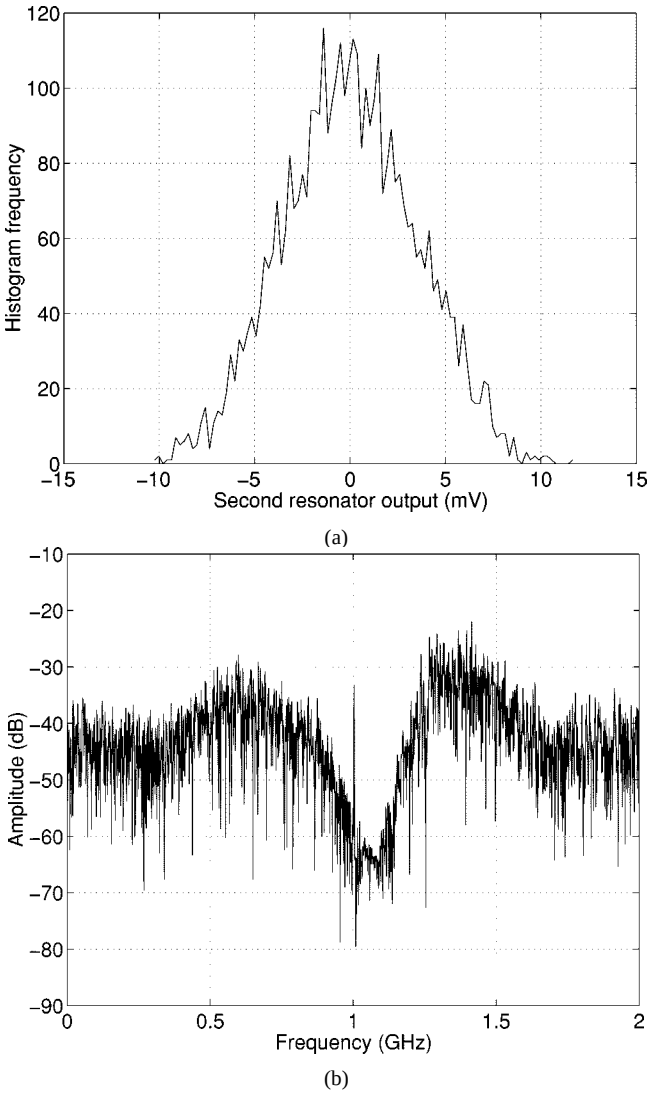


Fig. 15. (a) Quantizer input voltage histogram. (b) Output spectrum from SPICE.

3) We discovered after fabrication that we had scaled the DAC currents improperly. Fig. 15(a) plots a histogram of the voltage at the input of the quantizer from a SPICE simulation; the maximum quantizer input magnitude is a mere 10 mV. Fig. 15(b) shows the FFT of 4096 output bits, and it is readily apparent that the in-band noise is flat rather than shaped. We are clocking the quantizer (which is an ECL-style latched comparator) at 4 GHz in a process with $f_T = 50$ GHz, and this is aggressive enough that there needs to be a much larger voltage swing at the quantizer input for it to reliably switch. SPICE can be used to show the solution to this problem lies in lowering the 2-kΩ emitter degeneration resistors in the DAC's, which provides more DAC current, and hence, more voltage swing at the expense of higher power consumption.
4) The previous two points could be rendered moot by including a method of capturing the digital bits.
5) For manufacturability, we would likely replace the fixed resonator capacitors with varactors which could be tuned to counter process variations. To tune them, we could

clock the modulator with an on-chip VCO also containing a varactor; tuning of both varactors could perhaps be accomplished simultaneously.

6) Likewise, instead of scaling DAC currents with tunable voltages, we might consider replacing the bipolar sources with ratioed nMOS transistors to provide the appropriate feedback scaling for best noise-shaping. This obviates the need for DAC current tuning circuitry.

If all these changes worked to best effect, modulator DR would be limited by the G_{g1} transconductor to 52 dB or so. We feel that with careful redesign of this transconductor, we could achieve 60 dB (10 bits) of dynamic range. The authors of [8] concluded that a similar performance level could be achieved in their 3.2-GHz $f_s/4$ modulator with a 25-MHz bandwidth.

X. Conclusion

We have described a procedure which may be used to choose the parameters for a high-speed continuous-time $f_s/4$ bandpass $\Delta\Sigma$M. We presented test results on a 4-GHz modulator of our own design and found that in a 20-MHz bandwidth at 1 GHz, 6.3 bits of resolution were achieved. In a redesign, and with a method for capturing the output bits, we feel we could improve this to 10 bits. The design procedure assumed an unjittered sampling clock, something which cannot be taken for granted in a real design.

We close by addressing the following question: Is wideband UHF ADC practical with high-speed $\Delta\Sigma$M's? For bandwidths into the tens of megahertz, it is a major challenge to get resolutions much above 10 bits with these circuits. The use of BP modulators followed by digital mixing and filtering is a tempting architecture choice, but a converter that works on an entire cellular band while maintaining a high-enough DR seems like a virtual impossibility. Apart from jitter problems, thermal noise is a serious problem at high conversion bandwidths. Consider an audio converter with a bandwidth of 44 kHz that achieves 16-bit resolution with a $\Delta\Sigma$M whose performance is limited by white thermal noise rather than shaped quantization noise. A similar thermal noise power level in a modulator clocking 1000 times faster with the same OSR (i.e., with a 44-MHz bandwidth) would have 30 dB more in-band thermal noise, and hence a resolution of only 11 bits. Perhaps one solution is to use an AGC amplifier in front of the $\Delta\Sigma$M; another is to perform the conversion at a much lower IF where circuit nonidealities and jitter problems are more easily overcome.

This is not at all to say high-speed $\Delta\Sigma$M is impractical in all cases. Three published circuits of interest are as follow.

1) Narrowband high-speed $\Delta\Sigma$M: [7] reports a 15-bit ADC with a 370-kHz bandwidth with a center frequency programmable from 0 to 70 MHz. Even with white in-band noise, oversampling still improves resolution, albeit at the slow rate of 0.5 bits per octave. With enough oversampling, high resolution can be achieved.
2) Hybrid mixer/modulator: [12] uses two low-pass modulators for I and Q channel demodulation with wideband mixers built right into the front end. A desired narrowband channel can simultaneously be mixed to dc and converted to digital for filtering. Once again, high-speed $\Delta\Sigma$M's are good for high-resolution narrowband conversion, and the modulator has no complicated tuning circuitry: channel selection is done by tuning a VCO.
3) Wideband ADC with a hybrid architecture: [20] reports a 1.25-MHz modulator with 16-bit resolution that uses a multibit $\Delta\Sigma$M front-end oversampled eight times, and a Nyquist-rate pipelined back end. The strengths of the individual circuits are exploited, the $\Delta\Sigma$M for high DR but limited bandwidth and the pipelined converter for high bandwidth but limited DR.

$\Delta\Sigma$M's are complicated circuits, particularly at high sampling rates. In our opinion, it is more useful to place the emphasis on finding architectures which exploit the strengths of $\Delta\Sigma$M rather than pushing the clock speed of the modulator.

Acknowledgment

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References

[1] W. Gao, J. A. Cherry, and W. M. Snelgrove, "A 4 GHz fourth-order SiGe HBT band pass $\Delta\Sigma$ modulator," in *Proc. VLSI Circuits Symp.*, 1998, pp. 174–175.
[2] S. R. Norsworthy, R. Schreier, and G. C. Temes, Eds., *Delta-Sigma Data Converters: Theory, Design, and Simulation*. Piscataway, NJ: IEEE Press, 1997.
[3] R. Adams, "Design and implementation of an audio 18-bit analog-to-digital converter using oversampling techniques," *J. Audio Eng. Soc.*, pp. 153–166, Mar./Apr. 1986.
[4] E. J. van der Zwan, "A 2.3 mW CMOS $\Sigma\Delta$ modulator for audio applications," *Int. Solid-State Circ. Conf. Tech. Dig.*, pp. 220–221, 1997.
[5] O. Shoaei and W. M. Snelgrove, "Design and implementation of a tunable 40 MHz–70 MHz Gm-C bandpass $\Delta\Sigma$ modulator," *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 521–530, July 1997.
[6] J. A. Cherry and W. M. Snelgrove, *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion: Theory, Practice, and Fundamental Performance Limits*. Norwell, MA: Kluwer, 1999.
[7] G. Raghavan, J. F. Jensen, R. H. Walden, and W. P. Posey, "A bandpass $\Sigma\Delta$ modulator with 92 dB SNR and center frequency continuously programmable from 0 to 70 MHz," *Int. Solid-State Circuits Conf. Tech. Dig.*, pp. 214–215, 1997.
[8] A. Jayaraman, P. Asbeck, K. Nary, S. Beccue, and K.-C. Wang, "Bandpass delta-sigma modulator with 800 MHz center frequency," in *Proc. GaAs Int. Circuits Symp.*, 1997, pp. 95–98.
[9] W. Gao and W. M. Snelgrove, "A 950 MHz second-order integrated LC bandpass $\Delta\Sigma$ modulator," in *Proc. VLSI Circuits Symp.*, 1997, pp. 111–112.
[10] T. Yamaji and H. Tanimoto, "A 2 GHz balanced harmonic mixer for direct-conversion receivers," in *Proc. Custom Integrated Circuits Conf.*, 1997, pp. 193–196.
[11] J. F. Jensen, G. Raghavan, A. E. Cosand, and R. H. Walden, "A 3.2-GHz second-order delta-sigma modulator implemented in InP HBT technology," *IEEE J. Solid-State Circuits*, pp. 1119–1127, Oct. 1995.
[12] M. A. Morin, "A 1.6 Gb/s delta-sigma modulator with integrated wideband mixer for RF applications," in *Proc. Bipolar/BiCMOS Circuits Technical Mtg.*, 1998, pp. 148–151.
[13] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, MA: Cambridge Univ. Press, 1998.
[14] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd ed. New York: Wiley, 1993.
[15] F. M. Gardner, "A transformation for digital simulation of analog filters," *IEEE Trans. Commun.*, pp. 676–680, July 1986.
[16] B. E. Boser and B. A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1298–1308, Dec. 1988.

[17] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J. Y.-C. Sun, B. S. Meyerson, and T. Rice, "Si/SiGe epitaxial-base transistors—Part I: Materials, physics, and circuits," *IEEE Trans. Electron Devices*, pp. 455–468, Mar. 1995.
[18] B. Gilbert, "The multi-tanh principle: A tutorial overview," *IEEE J. Solid-State Circuits*, pp. 2–17, Jan. 1998.
[19] J. A. Cherry and W. M. Snelgrove, "Clock jitter and quantizer metastability in continuous-time delta-sigma modulators," *IEEE Trans. Circuits Syst. II*, vol. 46, pp. 661–676, June 1999.
[20] T. L. Brooks, D. H. Robertson, D. F. Kelly, A. Del Muro, and S. W. Harston, "A 16 b $\Sigma\Delta$ pipeline ADC with 2.5 MHz output data-rate," *Int. Solid-State Circ. Conf. Tech. Dig.*, pp. 208–209, 1997.

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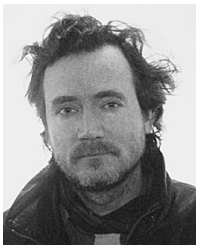

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