# A 160-MHz Fourth-Order Double-Sampled SC Bandpass Sigma–Delta Modulator

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***Abstract*— A fully differential double-sampled switched-capacitor (SC) architecture for a fourth-order bandpass $\Sigma\Delta$ modulator is presented. This architecture is based on a double-sampled SC delay circuit. The effect of opamp nonidealities (finite dc gain and nonzero input capacitance) on the notch frequency of this modulator is analyzed. The modulator is implemented in a 0.5-$\mu$m CMOS technology and operates at a clock frequency of 80 MHz, making the effective sampling rate 160 MHz. The image signal is about 40 dB below the fundamental signal. The measured signal-to-noise-plus-distortion (SNDR) is 47 dB (not including the image) over a 1.25-MHz bandwidth centered at 40 MHz. The circuit operates at 3 V and consumes 65 mW.**

## I. Introduction

HIGH-SPEED bandpass $\Sigma\Delta$ modulators are desired in applications that require A/D conversion of narrow-band signals at IF frequencies such as digital radios and high-speed modems. Increasing the sampling frequency of a bandpass $\Sigma\Delta$ modulator allows A/D conversion of the signal at higher IF frequencies and increases the A/D resolution. In a fourth-order bandpass modulator, increasing the sampling frequency by 2 reduces the quantization noise by 15 dB adding 2.5 bits to the resolution of the A/D converter. Digitizing the analog signal at a high IF and processing the signal in the digital domain is also desirable due to the robustness of the digital circuits.

Switched capacitor (SC) is the preferred analog technique for the implementation of $\Sigma\Delta$ modulators due to its high circuit accuracy. The operating speed of an SC circuit is determined by the settling time of the opamp used in the circuit. A method of increasing the sampling frequency is to use the opamp during both phases of a clock [1], i.e., double-sampling. This technique increases the sampling frequency by a factor of two without requiring a faster opamp. Double-sampling technique has already been applied to the design low-pass $\Sigma\Delta$ modulators [2], [3]. Two recently published works have utilized the double-sampled SC technique in the design of fourth-order band-pass $\Sigma\Delta$ modulators [4], [5]. A major limitation of double-sampled SC circuits is due to mismatch in the two paths [6] that causes an in-band image of the signal. However, in many digital radio systems the required image suppression is about 20–25 dB [7]. This requires an amplitude mismatch of less than $\pm$10% to $\pm$5.6% between the two paths. In the double-sampled SC circuit described here, path mismatch is dominated by capacitor matching. Specifically, since the first sampling capacitors determine the matching of the two paths and also dominate the total thermal noise budget $(kT/C)$, they are typically chosen to have the largest values in the modulator. In many CMOS processes capacitor mismatch typically ranges from a fraction of 1% to few percent depending on capacitor size and layout proximity. Thus, a path mismatch of less than 5.6% is easily achieved in this double-sampled bandpass sigma–delta modulator.

This paper starts by introducing a $z$-domain architecture for a fourth-order bandpass $\Sigma\Delta$ modulator. The modulator is obtained by transforming integrators to resonators in a second-order (double integration) low-pass $\Sigma\Delta$ modulator. The resulting bandpass modulator is a double-resonator $\Sigma\Delta$ modulator. In the sampled-data domain, an efficient method of implementing resonators uses two delay cells in a negative feedback loop. A double-sampled SC delay cell is presented. The impacts of nonideal circuit behaviors on the performance of a simple SC delay cell and the double-sampled SC delay circuit are analyzed. Specifically, the effect of low dc gain of the opamp on the performance of this modulator is analyzed. It is shown that a low dc gain will shift the notch frequency to a lower value and increases the in-band quantization noise. Then a SC implementation of the fourth-order bandpass $\Sigma\Delta$ modulator is presented along with Eldo [8] simulation results. Finally, the design of the modulator in a 0.5 $\mu$m CMOS process is considered and measured results of the modulator are presented.

## II. Double-Sampled SC Bandpass $\Sigma\Delta$ Modulator

In a bandpass $\Sigma\Delta$ modulator, the quantization noise is pushed away from the signal band at the desired center frequency $f_0$ by placing the quantization noise nulls at $f_0$. A simple way of designing bandpass $\Sigma\Delta$ modulators is to perform a low pass to bandpass transformation. One such transformation in the discrete-time domain is achieved by the following change of variable:

$$z^{-1} \rightarrow -z^{-2}. \tag{1}$$

This transformation maps the zeros of the low-pass prototype from dc to $\pm f_s/4$, suppressing the noise in the bandpass modulator around the $f_s/4$ and $3f_s/4$ the frequencies. The stability and signal-to-noise ratio (SNR) characteristics of this

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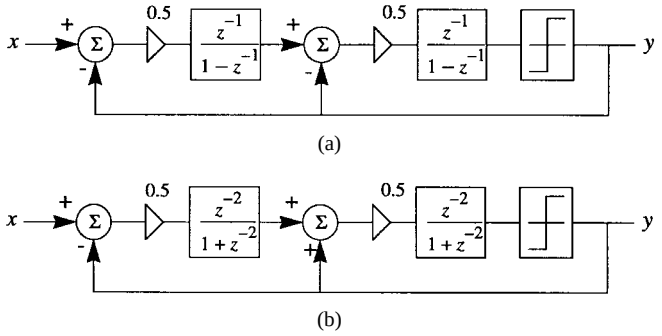



Fig. 1. A second-order low-pass sigma–delta modulator (a) mapped to a fourth-order bandpass sigma–delta modulator. (b) By transforming integrators to resonators.

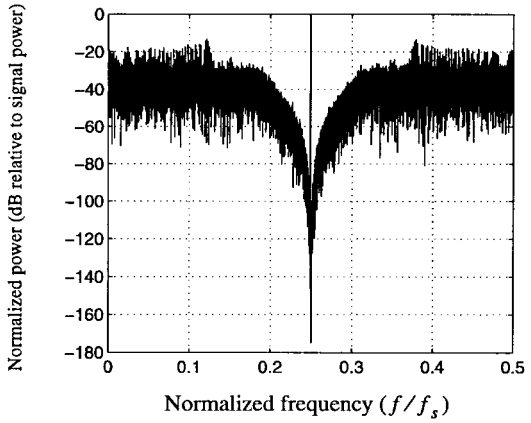



Fig. 2. Simulated output spectrum of the fourth-order bandpass sigma–delta modulator in Fig. 1(b) for a sinusoidal input.

bandpass modulator will be identical to that of the low-pass prototype [9].

A fourth-order bandpass sigma–delta modulator is obtained by performing the above mapping to a second-order low-pass $\Sigma\Delta$ modulator as shown in Fig. 1. Assuming the quantization error to be white noise and the comparator gain to be unity, the output–input transfer characteristic of this bandpass modulator is

$$Y(z) = z^{-4}X(z) + (1+z^{-2})^2 E(z). \tag{2}$$

The noise transfer function of this modulator has a pair of complex-conjugate zeros located at $z = \pm j$. In the frequency domain, this corresponds to notches around $(2n+1)f_s/4$, where $n = 0, 1, 2, \cdots$, and $f_s$ is the sampling frequency. The $z$-domain simulated output spectrum of this modulator is shown in Fig. 2.

The noise shaping is clearly seen at around a quarter of the sampling frequency. As discussed before, this fourth-order modulator is guaranteed to be stable because of the stability of the second-order low-pass prototype.

The $f_s/4$ resonator can be implemented in several different ways using SC techniques. In [10], resonators are implemented using Lossless Discrete Integrators (LDI) and Forward-Euler (FE) integrators. Another approach is to use two delay cells in a negative feedback loop [11], as shown in Fig. 3. The latter design is chosen here for SC implementation because it operates at a higher speed [10] and also a SC delay circuit is

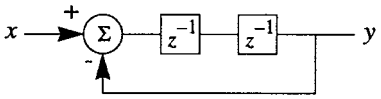
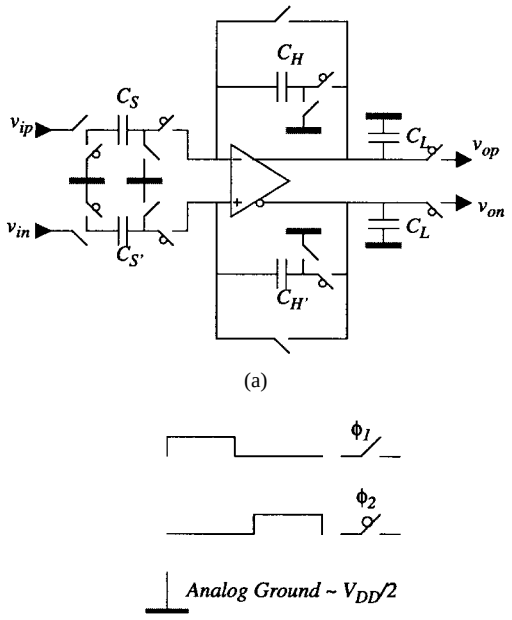



Fig. 3. Resonator using two delay cells.



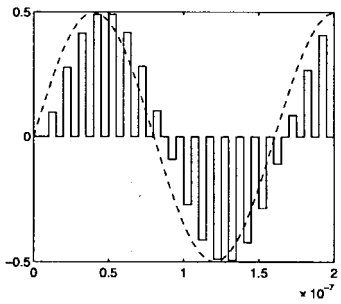




Fig. 4. (a) SC half-delay gain stage. (b) Two-phase nonoverlapping clock. (c) Input (dashed line) and output (solid line) waveforms.

immune to capacitor nonlinearity [12] which is useful when a SC circuit is implemented by weakly nonlinear MOSFET capacitors.

The circuit of a fully differential SC amplifier is shown in Fig. 4. A two-phase nonoverlapping clock, as shown in Fig. 4(b), is required for the operation of this circuit. The output is delayed by a half-clock period and has a gain of $C_S/C_H$. Assuming infinite opamp dc gain and denoting the differential input and output by $v_{od}$ and $v_{id}$, where

$$v_{od} = v_{op} - v_{on} \quad \text{and} \quad v_{id} = v_{ip} - v_{\text{in}} \tag{3}$$

the $z$-domain transfer function of this amplifier (output sampled during $\phi_2$) is

$$\frac{V_{od}(z)}{V_{id}(z)} = \frac{C_S}{C_H} z^{-1/2}. \tag{4}$$

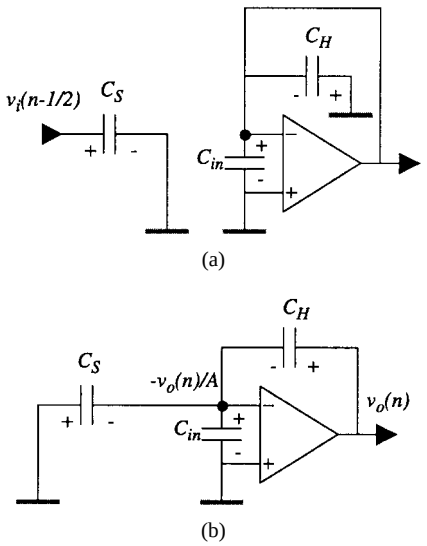



Fig. 5. Single-ended equivalent circuit of Fig. 4(a) during (a) $\phi_1$ and (b) $\phi_2$ phases.

If the sampling capacitor, $C_S$, and the holding capacitor, $C_H$, are identical, the circuit is called a unity gain buffer or sample-and-hold circuit.

Finite dc opamp gain $(A)$ and a nonzero opamp input capacitance $(C_{\text{in}})$ introduce gain error in (4), as analyzed below. Fig. 5 shows single-ended equivalent circuits of Fig. 4(a) during $\phi_1$ and $\phi_2$ phases.

Charge conservation on capacitors $C_S, C_H$, and $C_{\text{in}}$ before and after $\phi_2$ yields the following difference equation:

$$C_S\left[v_i(n-1/2)-\frac{v_o(n)}{A}\right]-C_H\left[v_o(n)+\frac{v_o(n)}{A}\right] = C_{\text{in}}\frac{v_o(n)}{A} \tag{5}$$

In the $z$-domain the actual transfer function of the fully differential SC amplifier becomes

$$H_{HD}(z)=\frac{V_{od}(z)}{V_{id}(z)}=\frac{C_S}{C_H}\cdot\frac{1}{1+\dfrac{1}{A\beta}}\cdot z^{-1/2} \tag{6}$$

where $\beta$ is the feedback factor and is given by

$$\beta=\frac{C_H}{C_H+C_S+C_{\text{in}}}. \tag{7}$$

Here, $C_{\text{in}}$ represents the sum of all parasitic capacitances appearing at the input of the opamp, including opamp input capacitance. If $A\beta \gg 1$, the transfer function of (6) can be simplified to

$$H_{HD}(z)=\frac{C_S}{C_H}\left(1-\frac{1}{A\beta}\right)\cdot z^{-1/2}. \tag{8}$$

Another source of error in the half delay circuit is incomplete settling. During the hold phase $(\phi_2)$ the opamp is connected in a negative feedback configuration and is modeled by Fig. 6. If the opamp is a single-stage circuit with a gain of $A=\omega_u/s$, the closed-loop transfer function will be

$$\frac{V_{od}}{V_{id}}(s)=\frac{A(s)}{1+\beta A(s)}=\frac{\omega_u}{s+\beta\omega_u}. \tag{9}$$

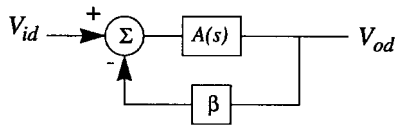



Fig. 6. Opamp in the closed-loop configuration during $\phi_2$.

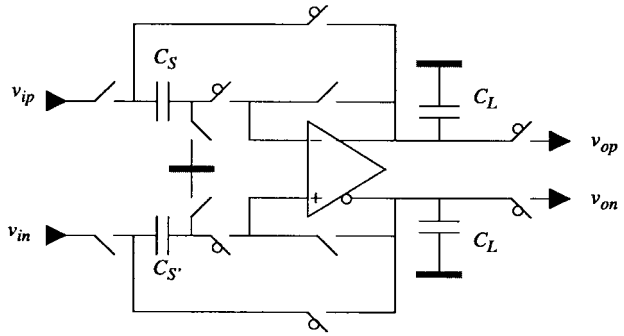



Fig. 7. One-capacitor sample-and-hold circuit.

Thus, the output of the SC half delay amplifier follows an exponential behavior as follows:

$$v_{od}=v_F(1-e^{-t/\tau}). \tag{10}$$

Here, $v_F$ is the final output value and $\tau$ is the closed-loop time constant given by

$$\tau=\frac{1}{\beta\omega_u} \tag{11}$$

where $\omega_u$ is the open-loop unity gain frequency of the opamp given by $\omega_u = g_m/C_{TL}$. Here, $g_m$ is the opamp transconductance and $C_{TL}$ is the total load capacitance appearing at the output of the opamp during hold phase which is

$$C_{TL}=C_L+\beta(C_S+C_{\text{in}}). \tag{12}$$

where $C_L$ is the opamp load capacitance plus all parasitic capacitances at the output of the opamp.

The capacitor mismatch between $C_S$ and $C_H$ introduces gain error. An efficient architecture for unity gain SC sample-and-hold exists which is immune to capacitor mismatch and requires one capacitor to perform both sample and hold operations, as shown in Fig. 7 [14].

In this circuit, during $\phi_1$ input voltage is stored on sampling capacitor $C_S$ and during $\phi_2$ capacitor $C_S$ is switched to the output and plays the role of holding capacitor. Thus, gain error due to mismatch between sampling capacitor and holding capacitor is irrelevant. Furthermore, the one-capacitor sample-and-hold structure has other advantages over the two-capacitor version. In the one-capacitor sample-and-hold circuit, finite opamp gain $A$ still causes gain error and the transfer function is

$$H(z)=\frac{V_{od}}{V_{id}}(z)=\frac{1}{1+\dfrac{1}{A\beta}}\cdot z^{-1/2}\approx\left(1-\frac{1}{A\beta}\right)\cdot z^{-1/2} \tag{13}$$

where the feedback factor $\beta$ is given by

$$\beta=\frac{C_S}{C_S+C_{\text{in}}}. \tag{14}$$

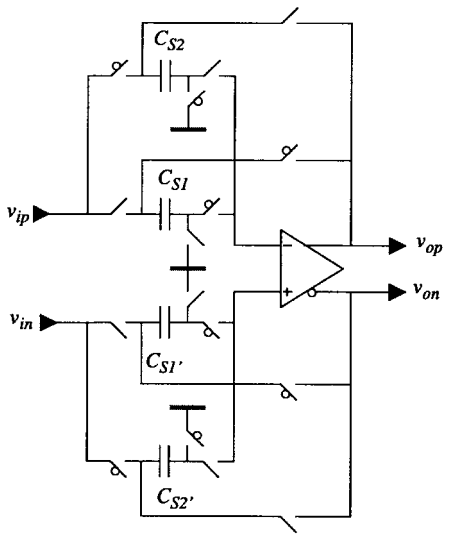



Fig. 8. Double-sampled SC delay circuit.

Compared to the two-capacitor sample-and-hold circuit, the one-capacitor sample-and-hold structure has a higher $\beta$ and, therefore, a lower sensitivity to op-amp gain.

The total load capacitance in this sample-and-hold circuit is

$$C_{TL} = C_L + \frac{C_S C_{\text{in}}}{C_S + C_{\text{in}}}. \tag{15}$$

The value of $C_{TL}$ is less in a single capacitor sample-and-hold circuit than in a two-capacitor sample-and-hold circuit. A lower equivalent output capacitance results in a higher unity gain frequency $\omega_u$. Therefore, the closed loop time constant of the one-capacitor sample-and-hold is smaller than the closed-loop time constant of a two-capacitor sample-and-hold circuit due to both higher $\omega_u$ and higher $\beta$.

The opamp in the one-capacitor sample-and-hold circuit of Fig. 7 is idle during the sampling phase $\phi_1$. By duplicating the sampling circuitry and using an alternate clock phase for it, a two-path SC sample-and-hold is obtained, as shown in Fig. 8.

In this circuit, the input signal is sampled every half clock period $(T_S/2)$ and appears at the output with a half-clock period delay. Thus the transfer function of this cell is

$$\frac{V_{od}}{V_{id}}(\hat{z}) = \hat{z}^{-1} \tag{16}$$

where $\hat{z} = e^{j\omega(T_S/2)}$.

Therefore, the effective sampling frequency in this two-path sample-and-hold circuit is twice the clock frequency. This structure is also called a double-sampled SC circuit [1]. The factor-of-two improvement in the speed of the double-sampled SC delay cell is achieved without increasing the clock rate or requiring a faster opamp settling time. In return, mismatch and uneven clock phases create image errors as discussed later.

Finite opamp gain $(A)$ and nonzero opamp input capacitance $(C_{\text{in}})$ cause error in the ideal transfer function of the double-sampled SC delay circuit and the actual transfer function is given by [12]

$$\frac{V_{od}(z)}{V_{id}(z)} = H_{aD}(z) = \left[\frac{g_0}{1 - p_0 z^{-1}}\right] z^{-1} \tag{17}$$

where $g_0$ and $p_0$ are given by

$$g_0 = \frac{1}{1 + \frac{1}{A} + \frac{C_{\text{in}}}{C_S} \cdot \frac{1}{A}} \qquad p_0 = \frac{C_{\text{in}}}{C_S} \cdot \frac{g_0}{A}. \tag{18}$$

Thus, finite opamp gain and nonzero input capacitance modify the transfer function of the double-sampled delay cell by a damped integrator term from its ideal response. This change of transfer function causes both gain and phase error in the response of the delay circuit. Following an analysis similar to the one in [15], the actual transfer function becomes

$$H_{aD}(z) = [m_{aD} e^{j\theta_{aD}}] \cdot z^{-1} \tag{19}$$

where $m_{aD}$ and $\theta_{aD}$ are the magnitude and phase of the error term in the double-sampled delay circuit. Assuming $A \gg 1$, the magnitude and phase error are given by

$$m_{aD} \approx 1 - \frac{1}{A\beta} + \frac{\cos\omega T}{A}\left(\frac{C_{\text{in}}}{C_S}\right) \tag{20}$$

$$\theta_{aD} \approx -\frac{\sin\omega T}{A}\left(\frac{C_{\text{in}}}{C_S}\right). \tag{21}$$

A double-sampled SC resonator is obtained by cascading two double-sampled delay circuits as shown in Fig. 9. The ideal transfer function of this circuit is

$$H_{iR}(z) = \frac{C_I}{C_{S1}} \cdot \frac{z^{-2}}{1 + z^{-2}}. \tag{22}$$

In this configuration, capacitance mismatch (between $C_I$ and $C_{S1}$) causes a gain error on the input signal $v_{id} = v_{ip} - v_{\text{in}}$ that is added to the feedback signal using a two-capacitor sample-and-hold architecture. If the error due to capacitor mismatch is $\delta$, the transfer function of the double-sampled resonator will be

$$H(z) = (1 + \delta)\frac{C_I}{C_{S1}} \cdot \frac{z^{-2}}{1 + z^{-2}}. \tag{23}$$

Therefore, the location of resonator poles is not affected by the capacitor mismatch. However, finite opamp gain $(A)$ causes errors in the ideal transfer function of a double-sampled SC delay circuit (given by (22))and the transfer function of a double-sampled resonator becomes

$$H_{dR}(z) = \frac{C_I}{C_{S1}} \cdot \frac{[(m_{dD1} \cdot e^{j\theta_{dD1}}) \cdot (m_{FD2} \cdot e^{j\theta_{dD2}})]z^{-2}}{1 + [(m_{dD1} \cdot e^{j\theta_{dD1}}) \cdot (m_{dD2} \cdot e^{j\theta_{dD2}})]z^{-2}}. \tag{24}$$

Poles of this resonator are

$$z_{p1,p2} = \pm j\sqrt{m_{dD1} \cdot m_{dD2}} \cdot e^{j[(\theta_{dD1} + \theta_{dD2})/2]}. \tag{25}$$

The poles are inside the unit circle, close to the intersection of $j\omega$-axis and the unit circle. The phase error of the poles of this resonator in radians is

$$\theta_{dR} = -\frac{\sin\omega T}{2A}\left[\frac{C_{in1}}{C_{S1}} + \frac{C_{in2}}{C_{S2}}\right]. \tag{26}$$

Both magnitude and phase errors are inversely proportional to the dc gain of the opamp. A double-sampled double-resonator SC bandpass $\Sigma\Delta$ modulator is constructed using

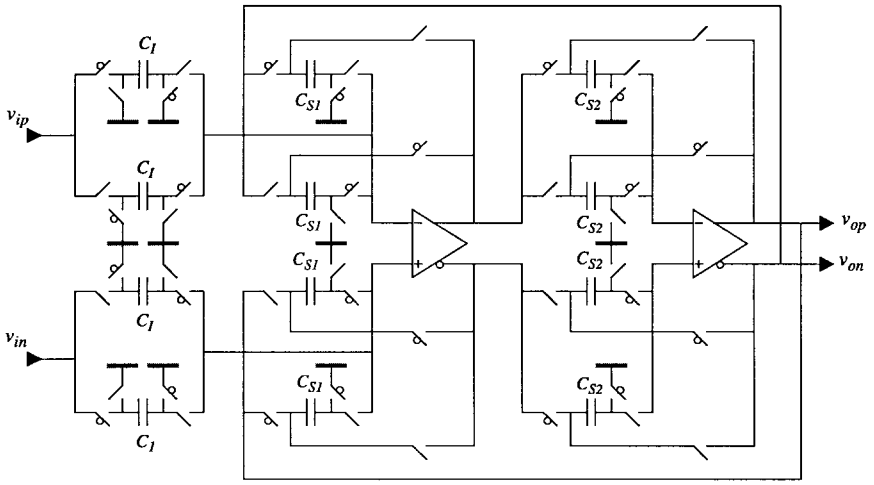



Fig. 9. SC resonator using two delay cells.

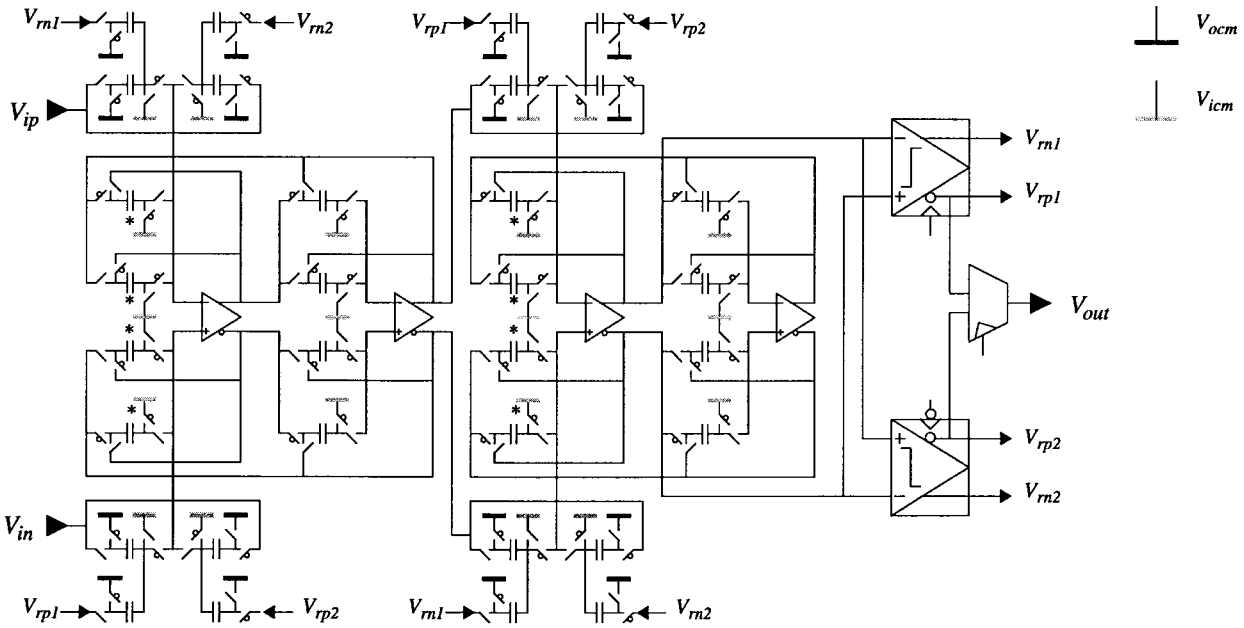



Fig. 10. A double-sampled SC fourth-order bandpass sigma—delta modulator.

two double-sampled resonators and a quantizer in a feedback loop, as shown in Fig. 10.

All the capacitors are unit size capacitors $(C_u)$, except for the eight marked by asterisks which have a value of $2C_u$ and are made of two unit size capacitors in parallel. The gain of resonators is set by these eight capacitors to the required value of 0.5.

The functionality of this double-sampled SC bandpass $\Sigma\Delta$ modulator was verified in Eldo using near ideal components. The on-resistance of the switches was set to 200 $\Omega$ and the dc gain of opamps was assumed to be 60 dB. Fig. 11 shows the output spectrum of the modulator for a sinusoidal input signal at 40.08 MHz. The amplitude of the signal was 12 dB below full scale (DAC reference voltage) and the clock frequency was 80 MHz.

Simulated SNR is about 106 and 63 dB for bandwidths of 200 kHz and 1.25 MHz, respectively. For the same clock frequency and signal bandwidth, the oversampling ratio of this modulator is twice as large as the single-sampled modulator. Thus, the SNR of this modulator is 15 dB higher than that of a single-sampled counterpart.

## III. Mismatch Analysis in the Double-Sampled SC Modulator

A major limitation of double-sampled SC circuits is due to mismatch in the two paths [6] that causes an in-band image of the signal as described here. A diagram of a two-path circuit and its corresponding clock phases is shown in Fig. 12.

The nonoverlapping clock has a frequency of $f_{\text{clock}}$ and the effective sampling frequency $(f_S)$ of a double-sampled SC circuit is $f_S = 2f_{\text{clock}}$. The sequence of the signals during $\phi_1$ (odd samples) is denoted by an "$o$" superscript and the sequence of the signals during $\phi_2$ (even samples) is denoted by an "$e$" superscript. The odd and even sequences have a

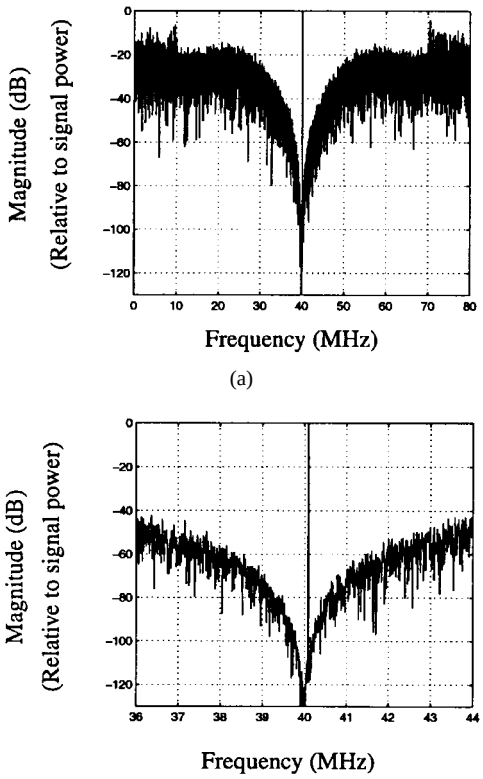



Fig. 11. Output spectrum from Eldo simulation: full view and expanded view of passband.

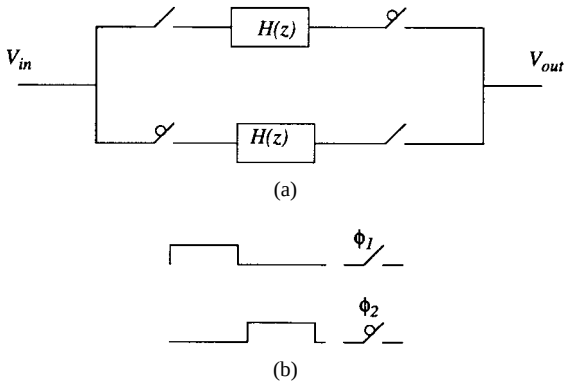



Fig. 12. Two-path SC circuit and clock phases.

sampling frequency of $f_{\text{clock}} = f_S/2$. The input sequence $v_{\text{in}}$ is a time-interleaved vector sum of odd $(v_{\text{in}}^o)$ and even $(v_{\text{in}}^e)$ sequences and in the $z$-domain we have

$$V_{\text{in}}(z) = V_{\text{in}}^o(z) + V_{\text{in}}^e(z) \tag{27}$$

Similarly, the output sequence is expressed as

$$V_{\text{out}}(z) = V_{\text{out}}^o(z) + V_{\text{out}}^e(z) \tag{28}$$

where odd and even sequences are related by

$$V_{\text{out}}^o(z) = H(z)V_{\text{in}}^o \qquad V_{\text{out}}^e(z) = H(z)V_{\text{in}}^e. \tag{29}$$

If the two paths are not symmetric and, for instance, there is a gain mismatch of between them, the input-output relation is

$$V_{\text{out}}(z) = (1+\delta)H(z)V_{\text{in}}^o H(z)V_{\text{in}}^e. \tag{30}$$

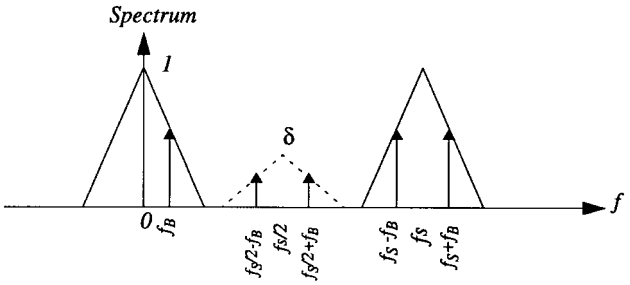



Fig. 13. Spectrum of the input signal $V_{\text{in}}$ (solid line) and the attenuated odd samples of the input signal (dotted line).

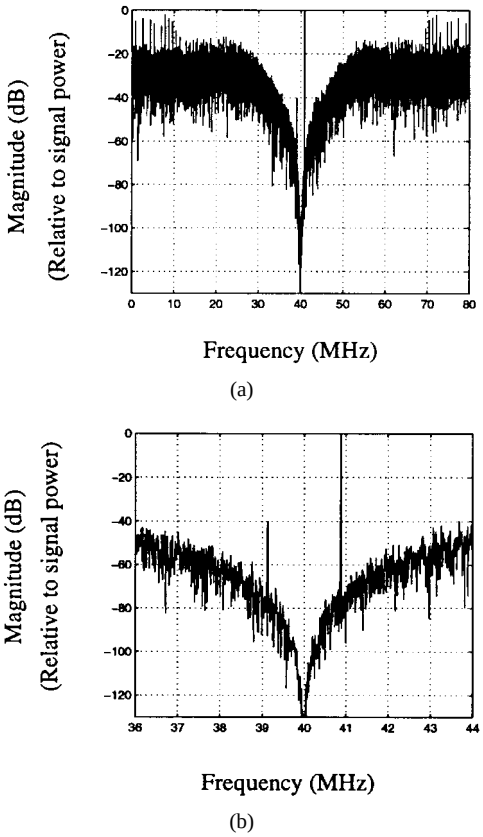



Fig. 14. Output spectrum of the double-sampled bandpass sigma–delta modulator with 1% capacitor mismatch between the two paths. Note that the image power is 40 dB below the signal power.

This equation can be expressed as

$$V_{\text{out}}(z) = H(z)[V_{\text{in}}(z) + \delta V_{\text{in}}^o(z)]. \tag{31}$$

Therefore, a mismatch between the two channels is equivalent to having an attenuated image of the signal being applied at the input along with the real input. Fig. 13 shows the spectra of the input signals $V_{\text{in}}$ and $\delta V_{\text{in}}^o$.

In the frequency domain, a sampled input signal $V_{\text{in}}$ with a frequency $f_B$ will have a periodic spectrum with the signal appearing at $nf_s \pm f_B$. The odd sequence of the signal has a sampling frequency of $f_s/2$ and thus attenuated images appear at $n(f_s/2) \pm f_B$.

Non-uniform sampling due to uneven $\phi_1$ and $\phi_2$ phases has a similar effect and causes an in-band image [16]. If phase $\phi_1$

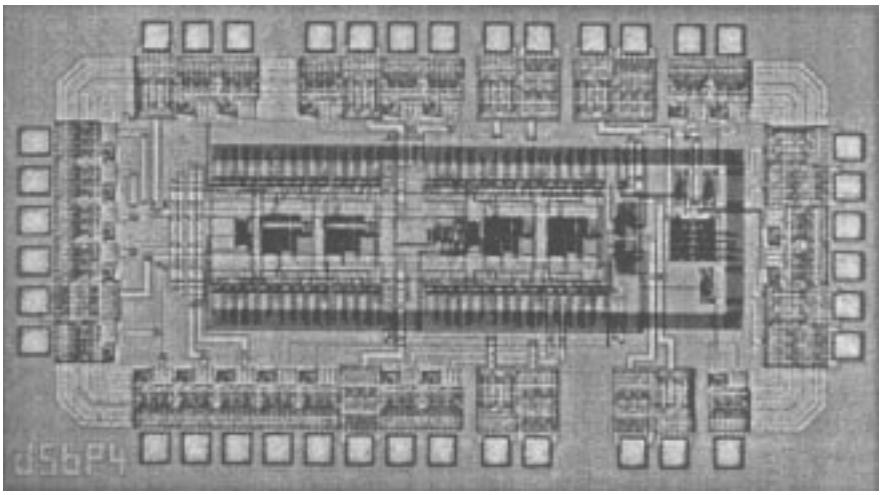


Fig. 15. Chip microphotograph of the fourth-order double-sampled SC bandpass sigma–delta modulator.

is longer by an amount $\tau$ compared to the $\phi_2$ phase, then we can write $1+\delta = e^{-s\tau} \approx 1 - s\tau$, so $\delta \approx -s\tau$.

Thus, double-sampled SC circuits are sensitive to path mismatch and any mismatch between the two channels will produce image problems. Mismatch in the second stage of the modulator is noise shaped (second-order noise-shaping) and will not cause a noticeable image signal. This image suppression is also frequency dependent and signals closer to the notch frequency produce smaller images. However, mismatch in the first stage of the modulator is critical and must be avoided. Simulations were carried out using different capacitor mismatches to verify the above argument. A path mismatch of $\pm 5\%$ in the second stage will produce an image 45 dB below full scale for a signal at 0.8 MHz offset from $f_s/4$. A path mismatch of $\pm 1\%$ on the input in the first stage of the modulator will produce an image signal which is only 40 dB below the signal. Fig. 14 shows the output spectrum of the modulator with a capacitor mismatch of $\pm 1\%$ between the input sampling capacitors (during $\phi_1$ and $\phi_2$). As we discussed before, an image suppression of only 25 dB is sufficient in many digital radio systems. Using layout techniques such as common-centroid, good capacitor matching—in the order of $\pm 0.1\%$—can be achieved. A capacitor mismatch of $\pm 0.1\%$ will reduce the power of image signal to about 60 dB below the signal power. This kind of accuracy, ten bits, is acceptable for other high-speed wide-band applications, such as cable modems and PCS basestations. If higher image suppression is needed, channel mismatch might be compensated for by using an LMS algorithm in DSP [13].

## IV. Implementation

The fourth-order double-sampled SC bandpass $\Sigma\Delta$ modulator in Fig. 10 was designed and fabricated in a 0.5 $\mu$m double-poly CMOS process. Fig. 15 illustrates the chip microphotographs of the modulator. The active chip area of this circuit is about 1.1 mm$^2$.

The main objective of the design was to demonstrate high-speed SC capabilities in submicron CMOS technologies. In [10], it is shown that SC circuits operating at 40 MHz are feasible in a 0.8-$\mu$m BiCMOS process. Here, the target clock frequency was set to be 80 MHz—the effective sampling frequency was 160 MHz. Therefore the IF frequency was at 40 MHz.

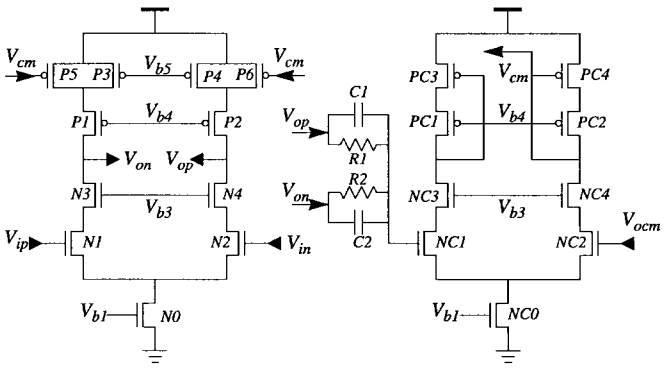



Fig. 16. Fully differential cascode opamp.

To achieve high speed at moderate power, the unit capacitors are chosen to be small, 300 fF. The total in-band $kT/C$ noise of this modulator is calculated to be less than $-76$ dB relative to 2 $V_{pp}$ signal.

Switches are parallel nMOSFET and pMOSFET transistors with a worst case on-resistance of 333 $\Omega$. This ensures the settling error to be less than 0.1%.

A single stage cascode opamp (also called a telescopic opamp) is used to achieve the high speed and adequate dc gain needed for the opamp. The schematic of a fully differential cascode opamp designed to fulfill these requirements is shown in Fig. 16. A continuous time common-mode feedback circuit sets the output common mode to the desired value. Resistors in the common-mode feedback circuit have a high value of 68 k$\Omega$ to ensure the opamp dc gain does not drop below 54 dB. The capacitors in the common mode feedback circuit have a value of 400 fF.

This opamp was simulated in Eldo using SPICE level 3 MOSFET models. Output conductance of transistors is poorly modeled in SPICE level 3 models. Therefore, simulations typically predict an optimistically high dc gain for the opamp.

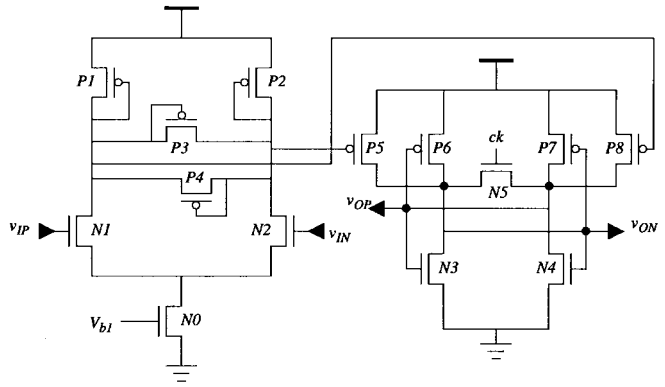



Fig. 17. Fully differential comparator.

A safety margin of 12 dB was added to the required simulated opamp dc gain (not including the loading by resistor divider in the CMFB circuit) because of this modeling error. The opamp was simulated by itself and the dc gain was about 66 dB. The resistor divider in the CMFB circuit reduces the dc gain to 54 dB.

This opamp operates at 3.3 V, has a simulated dc gain of 54 dB, a unity gain bandwidth of 650 MHz, a phase margin of 70° when driving a 1-pF load, and consumes 8.8 mW. Due to model inaccuracy of MOS output conductance, the measured opamp dc gain was about 40 dB.

In a $\Sigma\Delta$ modulator circuit, the required specification of the comparator is relatively easy to achieve. The comparator hysteresis can be modeled as an additive white noise at the input of the comparator. Both the input referred noise and the comparator hysteresis are noise-shaped (similarly to quantization noise) by the feedback loop and will be band-rejected around the center frequency $(f_s/4)$. Eldo SC simulations of the fourth-order $\Sigma\Delta$ modulators show that for a hysteresis voltage of 10% of the full scale (reference levels), the in-band noise power is increased by about 1.5 dB.

The schematic of a fully differential comparator used in the design of both modulators is shown in Fig. 17. The first stage is a preamplifier with a gain of 22 dB and a unity gain bandwidth of 650 MHz. The second stage is a cross-coupled latch reset by $N5$. Gain and unity gain bandwidth of the second stage are 28 dB and 620 MHz, respectively. This comparator is followed by a cross-coupled NAND latch. In the bandpass $\Sigma\Delta$ modulator, this comparator is followed by a latch. Thus, the outputs of the comparator have to drive a single logic gate with an input capacitance of 25 fF. For a 2-mV differential input signal, the delay time (from clock going low to output becoming ready) of the comparator driving 50-fF capacitor loads (gate capacitance and interconnect) is about 2 ns. The power consumption of the comparator at 3.3 V is about 3 mW.

## V. Measurements

The double-sampled bandpass SC $\Sigma\Delta$ modulator was tested at 3 V and a clock frequency of 80 MHz and consumes 65 mW. Fig. 18 shows the output spectrum of the modulator for an input sinusoid at 40.8 MHz with a peak amplitude of 6 dB below full scale (i.e. DAC reference voltage). The output bit-stream was captured by a logic analyzer for 16 384 clock cycles. In Matlab [17], a 16 384-point FFT was carried out to compute the output spectrum. The image signal is at 39.2 MHz and is 39 dB below the signal. This suggests that the capacitor mismatch is about 1%. As we discussed before, using layout techniques such as common-centroid, good capacitor matching—in the order of 0.1%—can be achieved. A capacitor mismatch of 0.1% will reduce the power of image signal to about 60 dB below the signal power. DSP techniques can also be used to postprocess the data and cancel the image [13].

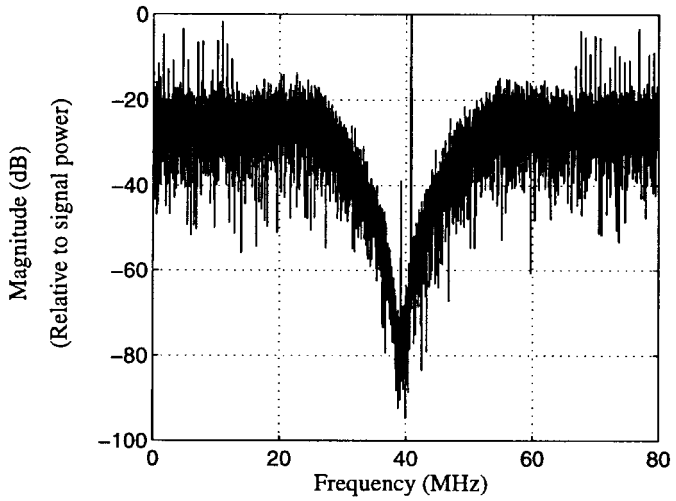



Fig. 18. Measured output spectrum of the double-sampled fourth-order SC bandpass sigma–delta modulator for an input signal of 6 dB below full scale. Note that image signal is about 39 dB below the fundamental signal.

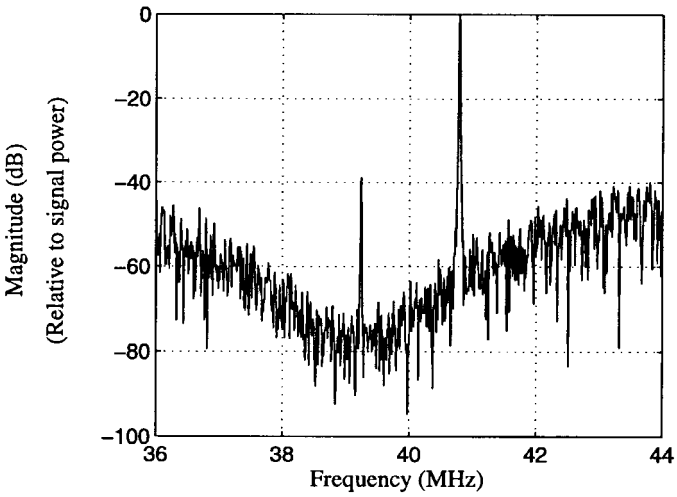



Fig. 19. Expanded view of the output spectrum around the notch. Note that the notch frequency is shifted by about 1 MHz.

Measured SNDR of this modulator is 47.1 dB in a bandwidth of 1.25 MHz if the image is ignored. This is about 16 dB less than the expected value of 63 dB. Opamp's low gain appears to be responsible for the reduced SNDR. Finite gain compensation SC techniques may be a good candidate for reducing the effect of a low opamp gain [18].

Fig. 19 illustrates an expanded view of the output spectrum around 40 MHz. As we can observe, the notch frequency of the modulator is shifted to about 39 MHz, which is 1 MHz below the expected value of 40 MHz. This is also due to low

opamp dc gain. Using (26), the opamp dc gain is calculated to be 40 dB. This is consistent with the estimated opamp dc gain obtained from measured MOSFET's output conductances.

## VI. Conclusions

A new double-sampled SC bandpass $\Sigma\Delta$ modulator was presented. An analytical expression for the notch shift due to low opamp dc gain was derived. Design and measurement results in a 0.5-$\mu$m CMOS process were also presented.

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