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A 5-GHz SiGe HBT Return-to-Zero Comparator for RF A/D Conversion

Weinan Gao, W. Martin Snelgrove, and Stephen J. Kovacic

Abstract-This paper presents a monolithic comparator implemented in a 0.5-μm SiGe heterojunction bipolar transistor (HBT) process. The SiGe HBT process provides HBT npn transistors with maximum f_T over 40 GHz and f_{max} over 55 GHz. The comparator circuit employs a resettable slave stage, which was designed to produce return-to-zero output data. Operation with sampling rates up to 5 GHz has been demonstrated by both simulation and experiments. The comparator chip attains an input range of 1.5 V, dissipates 89 mW from a 3-V supply, and occupies a die area of 407 x 143 μm^2. The comparator is intended for analog-to-digital (A/D) conversion of 900 MHz RF signals.

I. INTRODUCTION

THERE has been a significant research effort on developing bandpass delta-sigma analog-to-digital (A/D) converters in recent years since there is a demand for digitizing IF signals in wireless radio receivers [1]-[3]. It is desired to move the A/D conversion close to the front end of a radio to simplify the overall system design and alleviate the problems associated with IF mixers. The ultimate goal is to directly digitize the RF signal and hence eliminate any analog mixers. To approach such a high A/D conversion rate, crucial components including RF narrowband filters and gigahertz comparators need to be explored.

The bandpass delta-sigma modulator (BP$\Delta\Sigma$M) can be implemented by designing the loop resonator either in the discrete-time domain such as with switched-capacitor filters [2] or in the continuous-time domain such as with LC [1] or transconductor-C filters [3]. Switched-capacitor technology has to subsample RF signals heavily [4] and transconductor-C has poor dynamic range at RF. However, with recently demonstrated integrated inductors on silicon [5], bandpass conversion at gigahertz RF with LC resonators is now feasible. This would allow digital radios to be implemented with fully monolithic digital RF and baseband stages, which requires comparators that can be sampled at 3.6 GHz for a 900 MHz carrier. III-V compound technology has traditionally been the only contender for applications at such high frequencies [6], [7]. The emergence of production-ready SiGe heterojunction bipolar transistors (HBT's) offers an alternative technology which meets such high speed challenges [8], [9].

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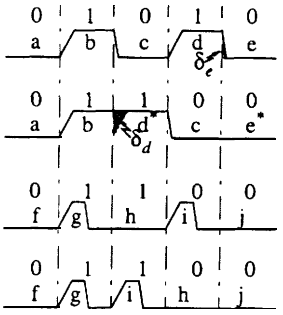


Fig. 1. Illustration of NRZ nonlinearity. (a) NRZ (0 1 0 1 0) pattern. (b)NRZ (0 1 1 0 0) pattern.(c) RZ(0_1_0_1_0) (d)RZ(0_1_1_0_0) pattern.

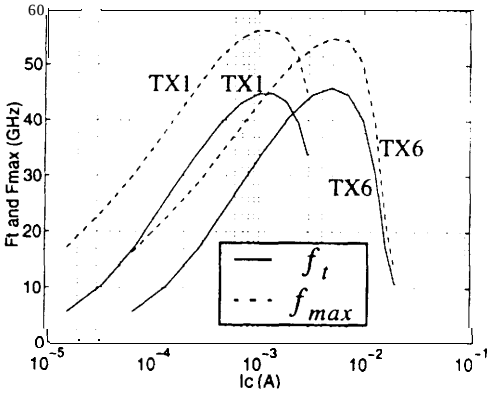


Fig. 2. Measured f_t and f_{max} versus I_C for both TX1 and TX6 transistors at V_{CE} = 1 V.

Employing a 0.5-μm SiGe HBT technology with a peak cutoff frequency around 43 GHz [9], we have implemented a high-speed comparator that exploits the attributes of SiGe HBT technology and achieves a sampling rate up to 5 GHz. The paper reports on the design and experimental results of the comparator. In a single-bit delta-sigma modulator the comparator acts as a signal sampler and one-bit quantizer Intersymbol interference (ISI) effects on the feedback pulse shape can induce nonlinearity in continuous-time modulators due to the difference of the integrated area between two data sequences as shown in Fig. 1. This can be mitigated by matching rise and fall times, such as by using differential circuits [7], or by using return-to-zero (RZ) pulses [1 1]. we use both approaches for increasing linearity. Whether RZ is necessary or not is an open question in this field; nonreturn-to-zero (NRZ) loops rely on matching and so make heavier demands on layout and manufacturing variability, while RZ demands speed. This work establishes that RZ is feasible The comparator has therefore been designed as a return-to

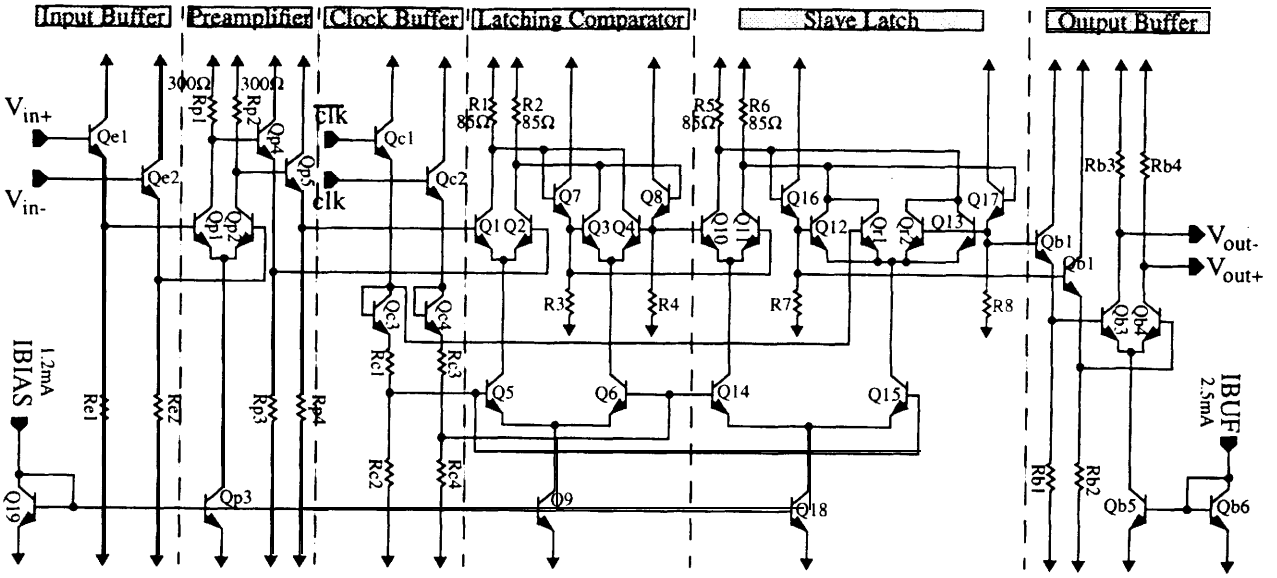


Fig 3. A complete schematic of the SiGe HBT return-to-zero comparator

zero comparator intended for RF delta-sigma A/D converter applications. RF conversion has traditionally been thought to consume a lot of power; the comparator is a critical part of a project that aims to bring power under 1 W.

II. SiGe HBT Technology

compared to conventional bipolar junction transistors (BJT's), SiGe HBT's have improved high frequency behavior, a low base resistance, and large βV_A product. To date, SiGe HBT transistors have reached 1 17 GHz f_T [9] and 160 GHz $f_{\max}$ [10]. Moreover, in some versions [8], SiGe HBT technology is compatible with submicron CMOS and hence we can complete the delta-sigma analog-to-digital converter and monolithic radio receiver design by implementing decimation filters and digital signal processors (DSP's) in submicron CMOS technology, which in general cannot be done by present III-V compound technology.

The SiGe HBT technology we used for the work is a high-performance production-ready HBT process, in which an SiGe HBT is fabricated by growing one or more thin epitaxial layers of SiGe alloy to form the base of the transistor [8]. The SiGe HBT technology features HBT NPN transistors, polysilicon resistors, polysilicon-to-polysilicon capacitors, three levels of metal interconnect, and substrate contacts. It is an 8-inch wafer process with a 0.5-μm minimum design rule and is compatible with 0.25-μm CMOS. Nominal SPICE Gummel-Poon (SGP) model device parameters for 0.5 x 2.5 μm^2 (TX I) and 0.5 * 10 μm^2 (TX6) emitter-area devices were extracted from test wafers and are summarized in Table I. These models have since been adjusted to reflect improvements in processing and extraction procedures [9]. The measured cutoff frequencies for current gain versus collector current for both transistors are shown in Fig. 2.

III. Circuit Design

SiGe HBT transistors are very similar to the conventional silicon homojunction bipolar transistors. The basic design principles gained in silicon BJT circuits can therefore be applied to SiGe HBT circuit design in a straightforward manner. Fig. 3 shows the complete comparator circuit configuration. It consists of an input buffer. a clock buffer, a preamplifier stage, a core latching comparator. a slave latch, and an output buffer. The design objective was to achieve the fastest possible operating speed without requiring excessive amounts of power and chip area. The use of differential signals in both the data and clock. paths leads to a fully symmetric topology. The power supply for the overall circuit was selected as 3 V to minimize power and be consistent with BV_{ceo} of the SiGe HBT transistors.

TABLE 1
TYPICAL SIGE HBT DEVICE PARAMETERS

Parameters	TX1	TX6
β (V_{CE} = 1 V)	100	130
Peak f_T (V_{CE} = 1 V)	43 GHz	45 GHz
Peak f_{MAX} (V_{CE} = 1 V)	56 GHz	55 GHz
BV_{ceo}	3.3 V	3.3 V
R_B	195 Ω	70 Ω
C_{JE}	9.65 fF	32.30 fF
C_{JC}	6.10 fF	17.42 fF
C_{JS}	5.27 fF	8.80 fF
τ_F	2.64ps	2.67 ps

A. Latching Comparator and Preamplifier

As illustrated in Fig. 3, the latching comparator is formed by two cross-coupled differential pairs activated by current switching clocks in a conventional series gated configuration [12]. The latching comparator circuit alternates between the sampling mode and the latching mode by switching on clk and clk signals, respectively.

To optimize the circuit design. we need to choose the proper voltage swing, load resistance, and tail current. The speed of the latching comparator is mainly determined by the recovery

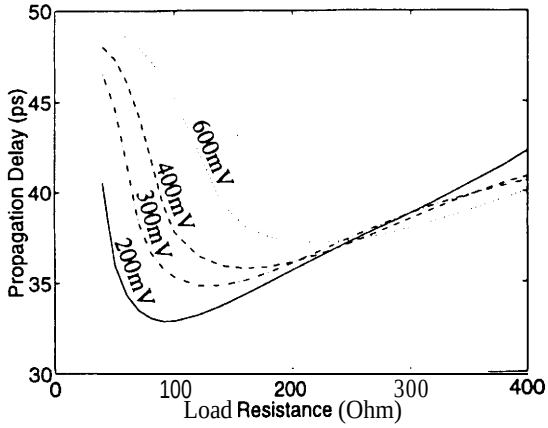


Fig. 4. Propagation delay versus load resistance for the latching comparator with different differential voltage swings.

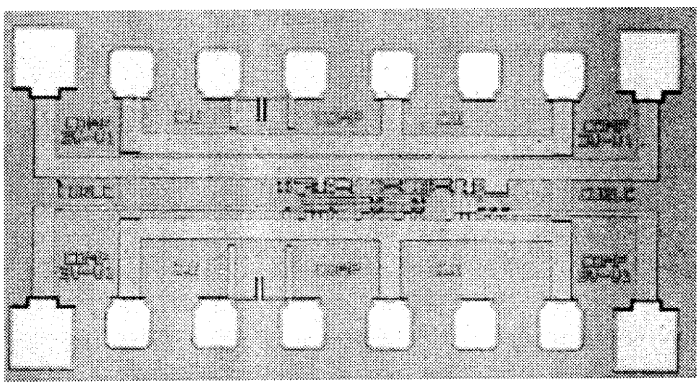
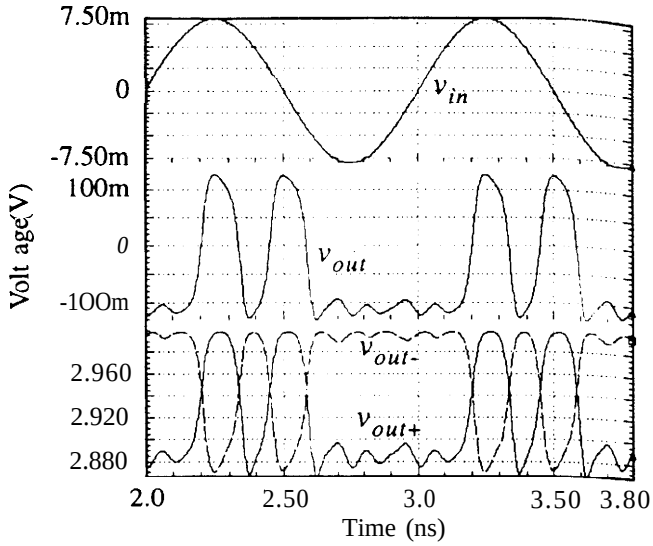


Fig. 5 Chip microphotograph of the SiGc HBT comparator

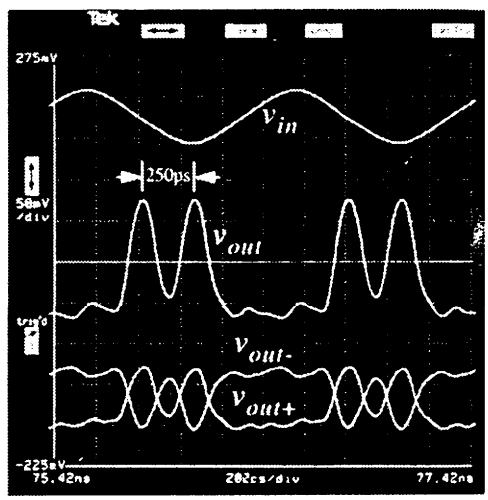
time t_r, which is defined by the time required in the sampling mode to change the output of the latching comparator from one logic state to the midpoint of the logic state. From a simplified model of the comparator representing the effective capacitance associated with the collector of the differential pair as C_L [12]. we have

$$t_r \propto R_L C_L \rightarrow t_r \propto \frac{\Delta V_o}{I_L} C_L \qquad (1)$$

where R_L is the equivalent collector load resistance, C_L is the total load capacitance, I_L is the tail current for the input differential pair of the latching comparator, and ΔV_o is the differential output voltage swing. It is therefore desirable to reduce output voltage swing in order to reduce the recovery time. A small output voltage swing is also favored for a 3 V supply. Further. in the LC BP$\Delta\Sigma$M design, the linear input range of active Q-enhanced LC filters is limited by the nonlinearity of the BJT or HBT transistor to a level on the order of the thermal voltage V_T ($V_T = kT/q \approx 26$ mV at room temperature) with present techniques [13]. However, the logic output voltage swing must be sufficient to switch the tail current of the differential pair including a margin for noise, interference, and the emitter degeneration effect, which set the lower limit. The minimum voltage required to fully switch on/off a differential pair is about four times the thermal voltage V_T. The additional voltage drop caused by the extrinsic emitter resistance of 15 Ω when transistors operate near the



(a)



(b)

Fig. 6. Simulated and measured waveforms for the SiGe HBT comparator with sinusoidal inputs: (a) simulation and (b) measurement.

1.2 mA current corresponding to peak f_T is: $I_L R_E = 1.2$ mA $\times 15\Omega = 18$ mV. Adding a 10% noise margin, the minimum voltage swing is: $\Delta V_o = 1.1(4 \times 26 + 18)$ mV $\approx$ 134 mV. The nominal voltage swing should be larger than this value to account for process variation. It has been shown in the literature that there is an optimum load resistance to achieve the minimum propagation delay for ECL circuits [14]. A series of HSPICE simulations was conducted to investigate this. Fig. 4 plots several simulated curves of propagation delay versus load resistance, where each curve corresponds to a voltage swing. Based on the simulation and the criteria on the selection of the output voltage swing and the tail current. it was concluded that: $\Delta V_o = 200$ mV. $R_1 = R_2 = 85\ \Omega$. and $I_L = 1.2$ mA. The simulated rise and fall times are 60 ps while the propagation delay for both rising and falling edges is 33 ps.

The broad-band differential preamplifier stage amplifies the input signal by a gain and feeds this signal into the latching comparator. This helps the output of the latching comparator

TABLE II
SIMULATED AND MEASURED PARAMETERS

Parameters	Simulation	Experimental
Power Supply	3 V	3 V
Power Consumption	85.93 mW	89.04 mW
Offset Voltage	—	<1 mV
Input Voltage Range	1.5 V	1.5 V
Rise Time (10%-90%)	62 ps	avg. 76 ps
Fall Time (90%-10%)	70 ps	avg. 84 ps
Clock Frequency	max. 5 GHz	max. 5 GHz
Output Voltage Swing	200 mV	147 mV
Sensitivity	<2 mV	<4 mV

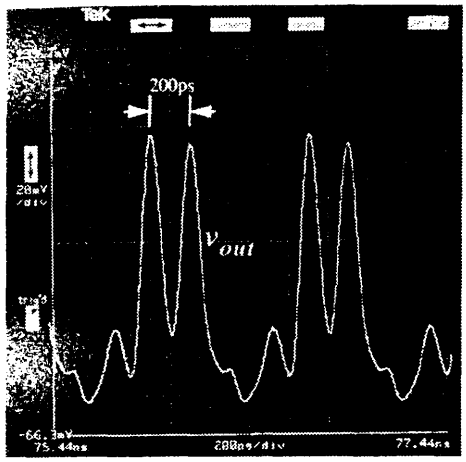


Fig. 7. A measured output waveform in response to a 1.25 GHz input signal and a 5 GHz clock.

change state quickly in the sampling mode. To optimize the input signal response. the preamplifier was designed to have the same time constant as that of the latching comparator [12]. To realize this the resistor values of R_{p1} and R_{p2} were chosen as 300 Ω, which set the gain of the preamplifier to 6.4. The emitter followers Q_{p4} and Q_{p5} are implemented using two TX1 transistors for each emitter follower. They reduce the clock flashback to the input and make a voltage level shift. It is cxpectcd that the small base resistance of SiGe HBT's should minimize the ringing caused by fast clock steering operation. The reason is that the output inductance of the emitter follower is directly proportional to the base resistance of the emitter follower circuit This. in turn, makes the resonance between the follower load capacitance and the output inductance shift to a higher frequency, which is about 1 1.7 GHz based on the theoretical calculation and HSPICE simulation. At this frequency, the resonance Q is low.

B. Return-to-Zero Latch

The differential output of the core latching comparator is fed to the slave latch stage shown in Fig. 3, which is similar to the core latching comparator To produce RZ data at its output, the latching comparator used for implementing the slave stage was modified by adding a transistor Q_{r1} controlled by clk to reset the latch output to the logical "0" state. Q_{r2} was added to keep symmetric differential operation. For proper RZ operation, the dc voltage level of Q_{r1} has to be compatible with the output of the slave stage. However, the dc bias voltage level for the clock steering differential pairs (Q_5–Q_6 and Q_{14}–Q_{15}) needs to be carefully set up to avoid differential pair transistors operating in saturation, especially for a 3 V power supply. Thus, voltage dividers (formed by R_{c1} and R_{c2}, and R_{c3} and R_{c4}) were used to provide a proper dc bias voltage level. The simulated rise and fall times for the RZ latch are 62 and 70 ps, respectively; while the rising edge and falling edge propagation delays are 39 and 45 ps, respectively.

The stave stage also helps to reduce metastable states by providing additional amplification of the input differential signal, and it extends conversion speed by holding a stable comparison result for a complete clock cycle.

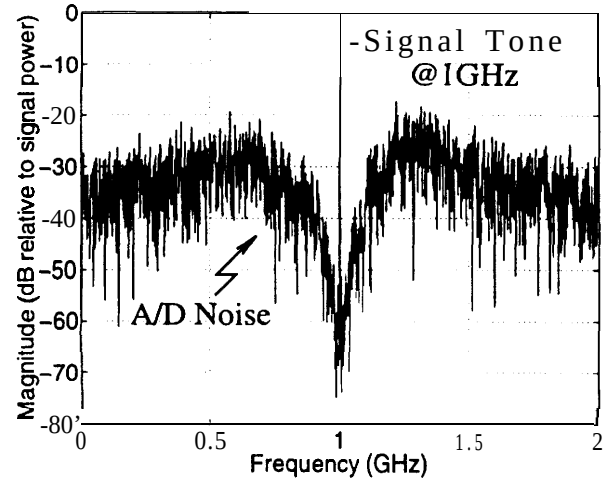


Fig. 8. Simulated output spectrum of a fourth-order LC bandpass modulator.

C. The Output Buffer

The output differential buffer amplifier was designed for unity gain into differential 50 Ω loads, with minimum loading of the internal comparator output. and sufficient bandwidth to minimize waveform distortion. The output voltage swing is proportional to the bias current I_{buf} of the output pair.

IV. Experimental and Simulation Results

Standard transistors were used throughout the comparator design. The TX1 transistor was used in the comparator design excluding the output buffer stage to minimize the power dissipation and layout area. The transistors used in the output buffer circuit were TX6. The comparator chip contains 43 npn transistors and 24 resistors. The comparator was fabricated as a part of a test chip in the IBM SiGe HBT technology. Fig. 5 shows a photomicrograph of the circuit. The total test chip area is 1162 x 606 μm^2, while the core circuit occupies an area of 407 x 143 μm^2.

The chip was tested through a gigahertz probe card. Table II lists the simulated and experimental results for the circuit. The lower measured output voltage swing is due to manufacturing variation in nominal resistor values, which are smaller than nominal. The RZ operation of the comparator results in the difference between the rise time and the fall time in both measurement and simulation. The measured rise and fall times

are longer than the simulated ones because the parasitic device parameters were not available for simulation. It should be pointed out here that a 5 GHz RZ comparator is equivalent to a 10 GHz normal (NRZ) comparator in terms of the edge speeds required. "Sensitivity*' estimates the width of the metastability region on the input when clocked at 4 GHz as the window of input levels for which the output pulse is significantly distorted. In BP$\Delta\Sigma$M's. the comparator output signal will be latched twice in another master-slave flip flop (M/S DFF) before it is used [3]. This should reduce metastability to a negligible level. The effect of metastability on the overall $\Delta\Sigma$ loop is included in our loop simulation below and does not appear to be severe. The lower measured voltage swing and longer measured rise and fall times contribute to a larger experimental minimum input voltage sensitivity. The 1 mV offset voltage is good, but unimportant in the BP$\Delta\Sigma$M application.

The HSPICE simulated and measured waveforms are shown in Fig. 6. Both cases were run at a 4 GHz sinusoidal clock with the input frequency set at 1 GHz, Fig. 7 is a measured output waveform with a 5 GHz sinusoidal clock that is the maximum speed achieved. where we can see that the output signal has a larger ringing and a smaller voltage swing. To demonstrate the application for BP$\Delta\Sigma$ A/D converters, Fig. 8 gives a simulated output spectrum of the comparator embedded in a fourth-order LC bandpass $\Delta\Sigma$ modulator that is modeled at the transistor level with a center frequency of 1 GHz and a sampling frequency of 4 GHz. The resultant signal-to-noise ratio (SNR) for a 10 MHz bandwidth is 49.5 dB.

Y. Conclusion

A high-speed SiGe HBT comparator has been implemented which provides good performance with a sampling frequency up to 5 GHz. The gigahertz RZ data output of the comparator would make LC bandpass delta-sigma A/D conversion on silicon possible. The successful demonstration of the 5 GHz comparator and the noise shaping spectrum simulation of a high-speed integrated LC bandpass delta-sigma modulator centered at an 1 GHz carrier frequency show the potential of SiGe HBT technology for high-speed analog, mixed signal, and RF wireless applications.

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