FLOATING GATE MOS DEVICE AS AN ANALOG TRIMMING ELEMENT

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ABSTRACT-This **paper investigates the use of floating gate MOS devices for analog trimming. A floating gate MOSFET structure, in which tunneling occurs at the corners of a polysilicon slab, has been fabricated using a standard 1.2μm n-well CMOS process. A three-dimensional device simulator, DAVINCI, is used to characterize the field enhancement due to geometry. The analog storage performance of the floating gate is evaluated. The charge-transfer behavior of floating gate MOS devices is analyzed and modeled. This model describes the charging and discharging of the floating gate and provides insights to the design of analog floating gate devices. A feedback-based programming strategy is also discussed.**

I. INTRODUCTION

Floating gate MOS transistors currently have widespread applications as the storage elements in EPROM and EEPROM circuits. These devices are optimized for small area, high write/erase speed and low failure rate when used for digital memory [1] [2]. Due to their long-term charge retention, the floating gate devices would have potential applications in analog circuits [3-5] but they are not trivial to implement and need much fundamental work.

The research is directed toward the use of floating gate devices as compact and non-volatile elements for analog trimming. Among the desired features of such a device are bi-directional fine trimming, low programming voltages, good charge stability, and large trim range. It is also desirable to avoid the need for special processing to achieve ultrathin oxide film [6] or textured-surface polysilicon [7] since these processing features are expensive and often not available.

Based on a previous attempt to build a tunneling injector in a 2μm standard p-well CMOS process by L. R. Carley [3], we have designed and fabricated tunneling injectors which rely on the corners of a polysilicon slab and a floating gate MOS device to test the feasibility of floating gate analog trimming circuits. The implementation technology is a 1.2μm n-well standard CMOS process (CMOS4S) [8].

To analyze these tunneling injectors, a three-dimensional field simulation is required. This study uses a three-dimensional device simulator, DAVINCI [9], to analyze field enhancement effects induced by geometric features.

To understand and control the transfer of charge onto and off the floating gate, it is necessary to develop a model which analytically describes charging and discharging of the floating gate via Fowler-Nordheim tunneling. Our model ties together most important parameters necessary for the analog floating gate MOS device design such as tunneling oxide thickness, tunneling area, critical coupling capacitances, programming time, programming voltages and initial floating gate voltage.

II. TUNNELING INJECTOR STRUCTURES AND CHARACTERIZATION

The floating gate MOS device in our study consists of a tunneling injector, a sense transistor and a polysilicon bootstrap capacitor (Figure 1). The tunneling injector enables the flow of electrons onto or off the floating gate by means of Fowler-Nordheim tunneling, and thereby sets the analog voltage on the floating gate which controls the operation of the sense transistor.

Normally, special processing requirements such as ultrathin tunneling oxide or textured-surface polysilicon are required to induce Fowler-Nordheim tunneling at a reasonable voltage (<20V) [6]. It has been suggested that corners introduced by lithographic features in the polysilicon layer can enhance the electric field in the oxide film[3]. To examine the influence of corners on the tunneling characteristic, a test chip which consisted of several tunneling injectors with different numbers of corners was designed and fabricated in CMOS4S. This process has a 250A gate oxide thickness and a poly-poly oxide thickness of 400A. The layouts of these tunneling injectors are shown in Figure 2, in which the polysilicon slab in each injector ends in the

middle of a diffusion region. According to electromagnetic field theory, the electric field is enhanced at the corners of this polysilicon slab [10].

The tunneling current is theoretically characterized by the Fowler-Nordheim equation [11]

$$J_{tun} = \alpha E_{tun}^2 \exp(-\frac{\beta}{E_{tun}}) \quad (1)$$

where J_{tun} is the current density, and α and β are constants determined from experimental data.

Figure 3 shows a typical measured tunneling current characteristics for electrons being injected onto (forward) or removed (reverse) from the floating gate as a function of the voltage difference between the floating gate and the diffusion region. It can be seen that the voltages required to induce the tunneling current in the forward and reverse directions are about 12V and 15V, respectively. They are much lower than the voltages for inducing tunneling in a structure without comers[1]. The tunneling current curve is asymmetric with slightly higher reverse tunneling voltage. To better characterize the tunneling performance of tunneling injectors, these measured data are replotted on Fowler-Nordheim axes ($\log(Z/V^2)$ *vs.* (V^{-1})) in Figure 4. The curves fit the Fowler-Nordheim equation well since the experimental data lie close to a straight line

We suspect that the asymmetry of tunneling is due to reverse behavior being defined by the comers of the polysilicon slab itself, while forward tunneling is defined by corners in the underlying diffusion.

From the forward Fowler-Nordheim plot, α and β can be extracted as 1.25×10^{-6} A/V^2 and 2.67×10^8 V/cm, respectively. In the reverse direction, a and β are 1.88×10^{-6} A/V^2 and 3.15×10^8 V/cm, respectively.

Without field enhancement, the tunneling-oxide electric field is given by

$$E_{tun} = \frac{|V_{tun}|}{X_{tun}} \quad (2a)$$

where V_{tun} is the voltage drop across the oxide and X is its thickness. Field enhancement increases electric fields near comers by a constant factor, so

[1] For the comerless structure in our test chip, no tunneling current was observed up to 25 volts.

$$E_{tun} = \kappa \frac{|V_{tun}|}{X_{tun}} \quad (2b)$$

where κ expresses the degree of field enhancement. For the experimental tunneling injectors, the reduction in tunneling from the "comerless" case indicates that κ in the forward and the backward tunneling direction is at least 2.0 and 1.6, respectively.

Our experimental data showed a great deal of variability in I-V characteristics between structures. Structure (d) and (e) have better uniformity over measurements of five different dice. This may be due to having more comers in Structure (d) and better control of comer radius in fabricating structure (e). Another important phenomenon is that measured tunneling current is not proportional to the number of comers. Both of these results indicate either the exact shape of the three-dimensional comers or the extent of interface trap states being very important in determining the degree of field enhancement. Therefore one of disadvantages of this tunneling injector is that it is sensitive to process variations because the process features strongly affect the exact shape of these 3-D comers. We don't know how consistent parameters are from run to run, but have the advantage over MOSIS users of using a single foundry.

It has been recently reported that tunneling can also occur through the oxide between the two polysilicon layers normally used for capacitors and that tunneling voltage is more reliable and controllable if there is a large tunneling area [12]. The polyl-poly2 tunneling injector may be useful as a substitute for the poly-diffusion tunneling injector in our floating gate analog MOS device structure.

Because it is the comers of the polysilicon that create enough field enhancement to dramatically lower the tunneling voltage, a three-dimensional field analysis is required to predict the degree of field enhancement and other three-dimensional effects. Figure5 shows electric field distributions simulated with DAVINCI in the oxide around the rectangular comers on applying 14 volts to the polysilicon electrode. It can be seen that the electric fields around the comer are stronger than the electric fields far away from the corner, and stronger than those without comers. The degree of field enhancement predicated by this simulation is about 1.5, lower than the data

given in [3]. The reason may be the description of the exact shape of three-dimensional comers, which is hard to know due to variability in fabrication. Further, DAVINCI cannot analyze arbitrary-shaped comers. To better predict tunneling performance and the impact of the shape of **the** three-dimensional comers on tunneling, an advanced three-dimensional device simulator which supports arbitrary grid structure and tunneling characteristics is required.

III. FLOATING GATE ANALOG STORAGE

The objective of floating gate analog trimming is to establish precise trim-voltage levels on the gate of the sense transistor, which is dependent on the amount of stored charge on the floating gate.

One of the significant characteristics of floating gate devices is their nonvolatile performance since the floating gate is completely isolated by surrounding layers of oxide. Therefore, the analog information stored on the floating gate can be retained for a sufficiently long time, and the floating gate can henceforth act as a capacitor with long-term charge retention capability. On the other hand, the stored analog information can be electrically programmed. This is achieved by applying a sufficiently high voltage across the tunneling injector, which causes a tunneling current to flow through the tunnel oxide, into or out of the floating gate, and thus changes the amount of charge stored on the floating gate positively or negatively. Therefore, both setting and updating of the stored voltage on the floating gate can be accomplished. The stored analog voltage on the floating gate can be accessed through the drain current of the sense transistor without destruction of the charge on the floating gate.

Essentially, the two variables that may be used to vary the amount of charge and hence the voltage stored on the floating gate are: (1) programming voltage, (2) programming time. The programming voltage controls the target values on the floating gate and programming time controls how close to this target value the programming comes.

Floating gate analog storage is designed to handle trim voltages that require high precision and good stability. The variability of their behavior is therefore a major concern. It is well known

that most floating gate digital memories have data charge retention exceeding 10 years at room temperature [1]. Since the floating gate MOS device here employs a standard gate oxide as the tunnel oxide, its retention should be very good. It has been experimentally demonstrated that the charge loss of these floating gate memories using a standard gate oxide for tunneling is less than 0.1 percent in ten years at operating and storage temperatures up to $100\,^{\circ}C$ [3].

V. MODELLING OF CHARGE-TRANSFER CHARACTERISTICS

In order to gain insight into the basic charge-transfer characteristic of floating gate MOS devices, a capacitive equivalent circuit shown in Figure 6, is developed. From this equivalent circuit, the floating gate voltage, V_{FG}, *can be* formulated using superposition as

$$V_{FG} = P_{CG}V_{CG} + P_{INJ}V_{INJ} + P_B V_B + P_S V_S + P_D V_D \pm \frac{Q_{FG}}{C_{FG}} \tag{3}$$

with

$$C_{FG} = C_{CG} + C_{FI} + C_B + C_S + C_D \tag{4a}$$

$$P_{CG} = \frac{C_{CG}}{C_{FG}}, \quad P_{INJ} = \frac{C_{FI}}{C_{FG}}, \quad P_B = \frac{C_B}{C_{FG}}, \quad P_D = \frac{C_S}{C_{FG}}, \quad P_S = \frac{C_D}{C_{FG}} \tag{4b}$$

where P_{CG}, P_{INJ}, P_B, P_S and P_D *are the* coupling ratios from the control gate, the current injector drain, the source of the n-channel transistor, the drain of the n-channel transistor and the substrate to the floating gate, respectively. Q_{FG} is the total charge on the floating gate, with "+" used for positive charge and "-" for negative.

Based upon the above equivalent circuit and the Fowler-Nordheim tunneling equation, analytical expressions can be derived to show the change in floating gate voltage as a function of programming voltage and time in each charging (injecting electrons onto the floating gate) or discharging (removing electrons from the floating gate) operation [13].

The change in floating gate voltage during charging is

$$\Delta V_{FG}(t) = -V_{FG}(0) + V_{INJ}(t) + \frac{M}{\ln[\exp(\frac{M}{V_{FG}(0) - V_{INJ}(0)}) + \beta NPt]} \tag{5a}$$

and the change in floating gate voltage during discharging is

$$\Delta V_{FG}(t) = -V_{FG}(0) + V_{INJ}(t) - \frac{M}{\ln[\exp(-\frac{M}{V_{FG}(0) - V_{INJ}(0)}) + \beta NPt]} \tag{5b}$$

where

$$V_{FG}(0) = P_{CG}V_{CG} + P_{INJ}V_{INJ}(0) + P_B V_B + P_S V_S + P_D V_D \pm \frac{Q_{FG}(0)}{C_{FG}} \tag{6}$$

$$\beta X_{tun} = M, \quad \frac{\alpha A_{tun}}{C_{FG} X_{tun}} = N, \quad P = \frac{C_{FG} + C_{INJ}}{C_{FG} + C_{FI}} \tag{7}$$

in which, C_{INJ} is the total capacitance associated with the diffusion node of the tunneling injector.

Eqs. (5a) and (5b) characterize the net electron accumulation and the net electron loss, respectively. If the voltage at the injection electrode, V_{INJ}, is a constant, the above equations reduce to

$$\Delta V_{FG}(t) = -V_{FG}(0) + V_{INJ} + \frac{M}{\ln[\exp(\frac{M}{V_{FG}(0) - V_{INJ}}) + \beta Nt]} \tag{8a}$$

for the charging process, and

$$\Delta V_{FG}(t) = -V_{FG}(0) + V_{INJ} - \frac{M}{\ln[\exp(-\frac{M}{V_{FG}(0) - V_{INJ}}) + \beta Nt]} \tag{8b}$$

for the discharging process.

Furthermore in the field enhancement situation, the equations (15a) and (15b) are simply modified as

$$\Delta V_{FG}(t) = -V_{FG}(0) + V_{INJ}(t) + \frac{M}{\kappa_1 \ln\{\exp(\frac{M}{\kappa_1[V_{FG}(0) - V_{INJ}(0)]}) + \beta NPt\}} \tag{9a}$$

for net electron accumulation, and

$$\Delta V_{FG}(t) = -V_{FG}(0) + V_{INJ}(t) - \frac{M}{\kappa_2 \ln\{\exp(-\frac{M}{\kappa_2[V_{FG}(0) - V_{INJ}(0)]}) + \beta NPt\}} \quad (9b)$$

for net electron loss. κ_1 and κ_2 characterize the degree of field enhancement in forward and reverse directions, respectively.

The above equations, giving $V_{FG}(t)$ versus time, are related to all of the most important parameters. Therefore, they are useful for the design and analysis of floating gate analog MOS devices. They can also be used to evaluate the charge-transfer characteristics and the controllability of analog floating gate devices. As an example of the application of this model, the programming rate of the floating gate in charging is simulated, with results shown in Figure 7. Data are shown with programming voltages of lSV, 16.5V and 17V applied to the control gate. The parameters we chose were based on the layout parasitics of our fabricated floating gate analog MOS devices and the measured characteristics of our tunneling injectors; they are: $\alpha = 1.25 \times 10^{-6}\,A/V^2$, $\beta = 2.57 \times 10^{8}\,V/cm$, $\kappa = 2$, $X_{tun} = 250\,Å$, $A_{tun} = 1\mu m^2$, $C_{FG} = 1pF$, $C_{INJ} = 5fF$, $V_{FE} = 12V$, $P_{CG} = 0.8$. As seen from this figure, the charging process is very fast; the changes in floating gate voltage achieved in $1\mu s$ are $-0.054V$, $-0.361V$ and $-0.834V$ with the three control voltages. We note that the change in floating gate voltage increases monotonically with increasing charging time. Also, from this simulation, we can see a basic trade-off higher programming levels result in a larger trim range (the extent of target values that may be achieved), but make it harder to control trim step size.

V. FEEDBACK-BASED PROGRAMMING

The operation of the floating gate device needs control circuitry to provide both positive and negative programming voltages to inject charge onto or remove it from the floating gate. An efficient programming strategy is to embed the floating gate MOS device into a feedback loop [14]. The local feedback circuitry measures the extent of the uncompensated offset in the system and then decides whether the trimming is needed, as well as which type of programming pulses is required.

A conceptual diagram of our feedback-based programming strategy is shown in Figure 8. Programming pulses are generated by high voltage driving circuitry, and the UP/DOWN counter decides programming direction. Accordingly, the amount of charge on the floating gate is increased or decreased to achieve a target value which is used to cancel the offset of the uncompensated circuit.

VI. CONCLUSION

The work presented here indicates that floating gate devices are very usable as analog trimming elements. The successful implementation of tunneling injectors with a number of comers demonstrates that floating gate trimming methods can be implemented in a standard CMOS VLSI process, although more work is still needed to provide a mom reliable and controllable floating gate device. The charge-transfer model provides a powerful tool for the design and analysis of analog floating gate devices.

ACKNOWLEDGMENTS

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FIGURE CAPTIONS

Figure 1. Analog floating gate MOS device structure: (a) cross section; (b) circuit symbol: (c) layout diagram.

Figure 2. Layout diagrams of the fabricated tunneling injectors: (a) without corners; (b) two corners; (c) four corners; (d) twenty six comers; (e) two comers over a p^+ diffusion area.

Figure 3. The measured I-V characteristic of a tunneling injector.

Figure 4. Fowler-Nordheim plot of the Figure 3: (a) forward direction; (b) reverse direction.

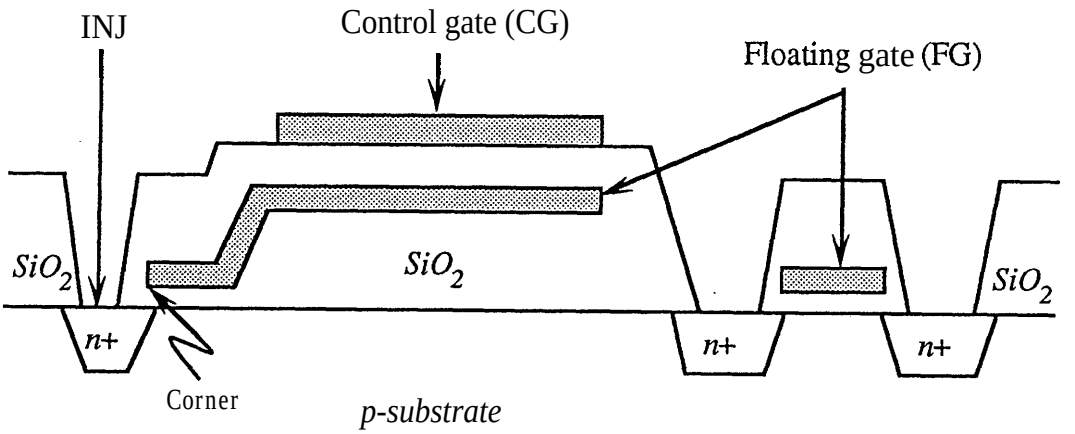
Figure 5. The 3-D simulation for the field distribution in oxide in case of a rectangular comer for the characterization of field enhancement: (a) at the comer; (b) $0.05\mu m$ away from the comer along the diagonal direction on the poly rectangle; (c) $0.1\mu m$ away from the comer along the diagonal direction on the poly rectangle; (d) $0.2\mu m$, $0.3\mu m$ and $0.4\mu m$ away from the comer along the diagonal direction on the poly rectangle, and the field distribution in oxide for the poly slab without comers.

Figure 6. A simplified capacitive equivalent circuit of the floating gate MOS device. C_{CG} is the floating gate to the control gate capacitance (bootstrap capacitance), C_{FI} is the overlap capacitance from the floating gate to the diffusion region of the tunneling injector, C_{FB} is the floating gate to substrate capacitance, C_S is the floating gate to source capacitance, C_D is the floating gate to drain capacitance.

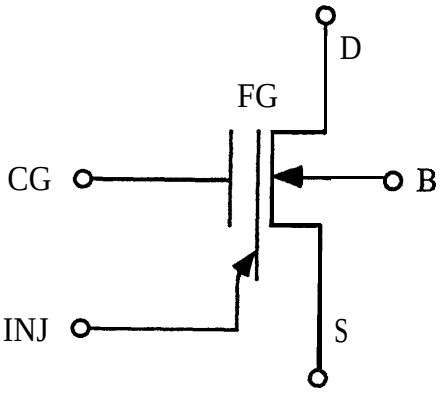
Figure 7. Simulation for the programming rate of charging operation with control voltages of 15V, 16.5V and 17V.

Figure 8. A conceptual diagrarn of a feedback-based programming strategy.

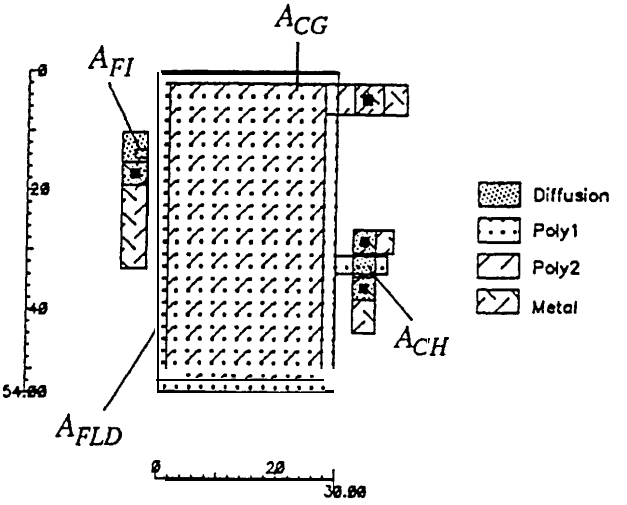
Figure 1


INJ
Control gate (CG)
Floating gate (FG)
SiO_2
SiO_2
SiO_2
n+
n+
n+
Corner
p-substrate

(a)


D
FG
CG
B
INJ
S

(b)


A_{CG}
A_{FI}
A_{CH}
A_{FLD}
Diffusion
Poly1
Poly2
Metal

(c)

Figure 2

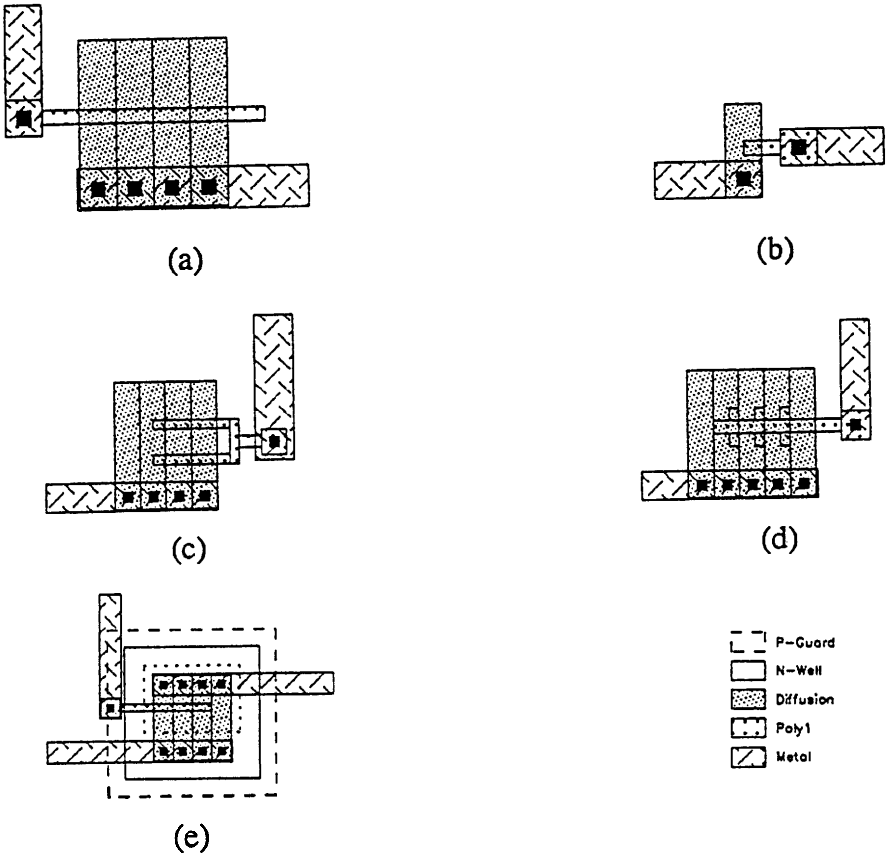


Figure 3

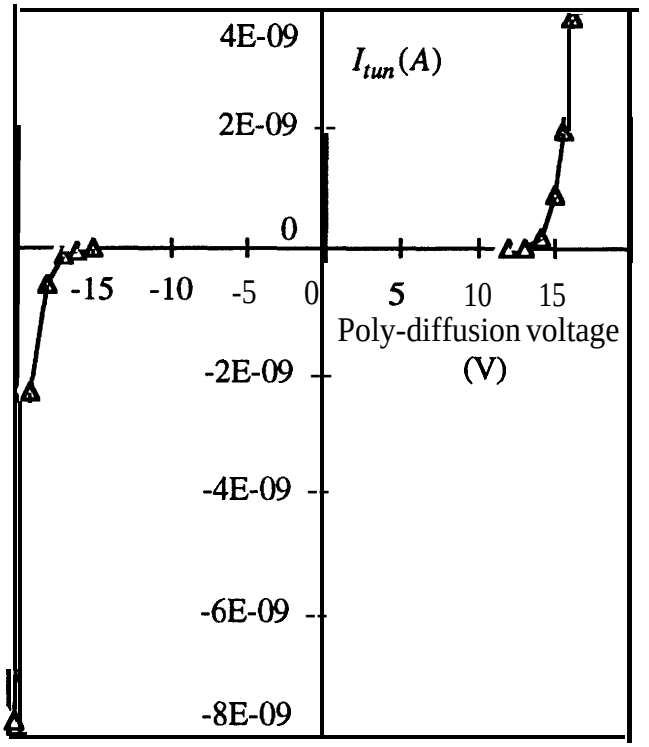

4E-09
2E-09
0
-2E-09
-4E-09
-6E-09
-8E-09
$I_{tun}(A)$
-15
-10
-5
0
5
10
15
Poly-diffusion voltage
(V)

Figure 4

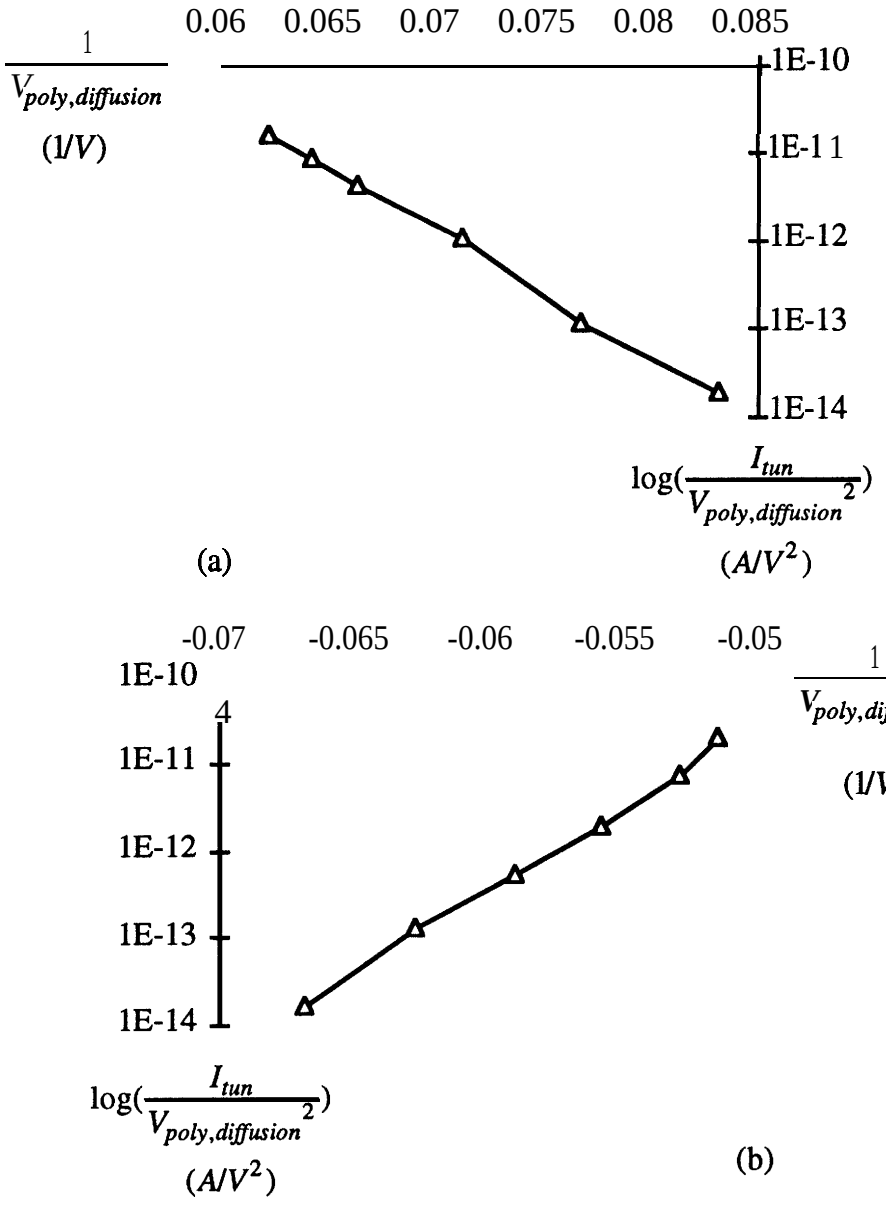

0.06
0.065
0.07
0.075
0.08
0.085
1
$V_{poly,diffusion}$
(1/V)
1E-10
1E-11
1E-12
1E-13
1E-14
$\log(\frac{I_{tun}}{V_{poly,diffusion}^2})$
(A/V^2)
(a)
-0.07
-0.065
-0.06
-0.055
-0.05
1E-10
1E-11
1E-12
1E-13
1E-14
$\log(\frac{I_{tun}}{V_{poly,diffusion}^2})$
(A/V^2)
1
$V_{poly,diffusion}$
(1/V)
(b)

Figure 5

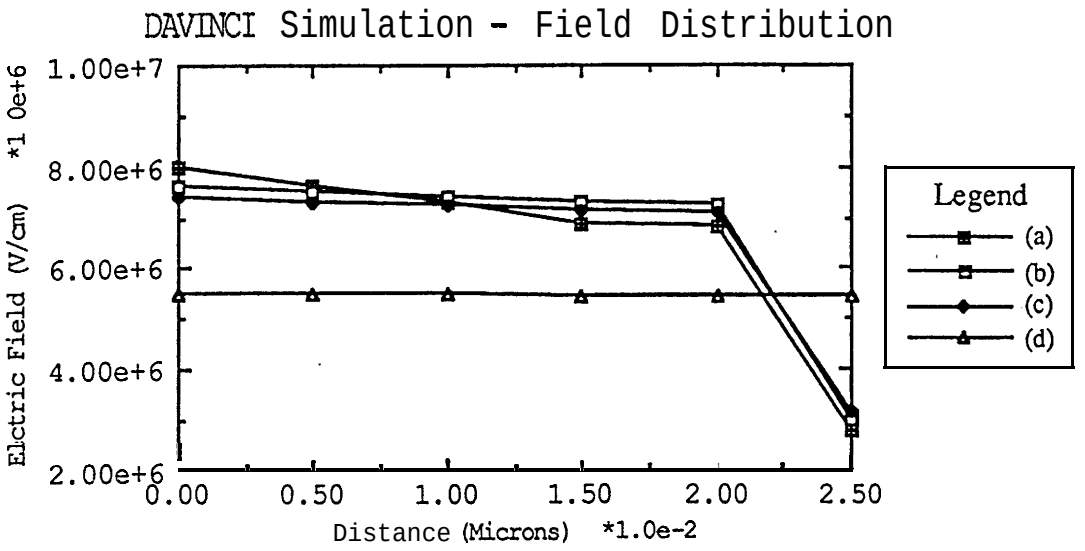


Figure 6

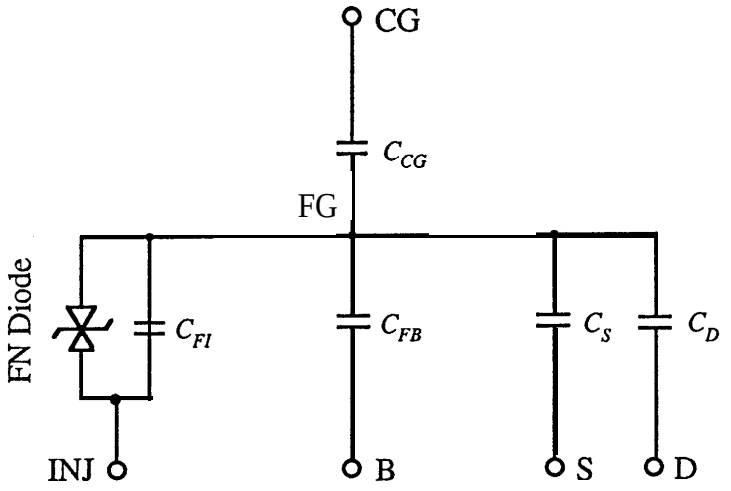


Figure 7

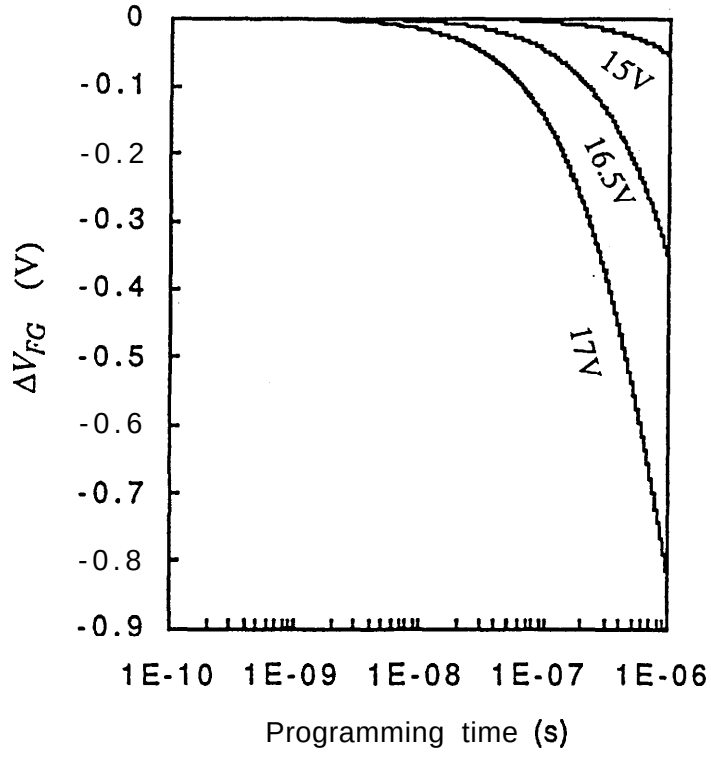


Figure 8