Simple backgated MOSFET structure for dynamic threshold control in fully depleted SOI CMOS

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A simple junction-isolated backgate electrode, formed by boron implantation through the buried oxide, is shown to provide effective dynamic control of device thresholds in fully depleted **SOI CMOS** for $\simeq$ 1 **V** power supply operation.

Introduction: Recently, Yang *et al*. have reported a fully depleted silicon-on-insulator (SOI) MOSFET structure in which an oxide-isolated polysilicon backgate electrode is formed beneath the MOSFET channel [1]. By applying bias to this backgate electrode, it is possible to modulate the device threshold voltage. In this way

the benefits of dynamic threshold adjustment in response to process variations, changes in ambient temperature and operating requirements demonstrated for bulk CMOS ICs operating at power supply voltages near or below 1V [2], can be extended to fully depleted SOI technology: which offers inherent advantages of reduced junction capacitance and near-ideal subthreshold swing. The structure described in [1] was formed by a complex wafer bonding and polishing technique. It is shown here that backgate control of V_T can be achieved using a much simpler structure.

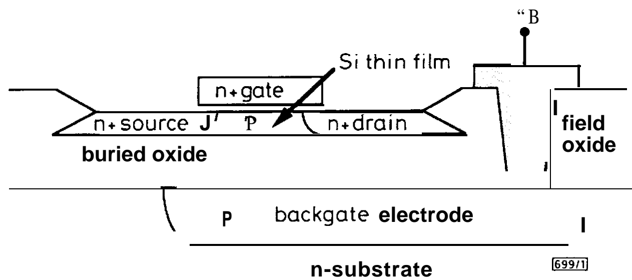

Fig. 1 *Cross-section of SOI MOSFET with implanted backgate electrode*

Device structure and simulation: Fig. 1 shows a new SOI MOSFET structure in which a backgate electrode is formed by boron implantation through the silicon film and buried oxide into a lightly doped n-type substrate. If the substrate is connected to the most positive potential generated on the integrated circuit, then the backgate electrodes will be junction isolated, allowing different backgate biases V_B to be applied to *n*- and p-channel devices, or to different groups of devices; e.g. V_{Tn} and $|V_{Tp}|$ could be raised in selected parts of an integrated circuit to lower power dissipation at the expense of reduced speed. Although Fig. 1 shows an extension of the backgate electrode underneath the MOSFET drain, to illustrate that contact to this electrode is made through a window etched in the field oxide, in a practical transistor the backgate electrode would only overlap the active channel, and would be contacted from the side to minimise parasitic capacitance to source and drain regions.

A structure similar to Fig. 1, in which an implanted n-well was placed beneath p-channel transistors in thin buried oxide SOI in order to enhance their current drive and reduce source/drain-to-substrate capacitance, was reported very recently by Yoshino *et al.* [3]. However, the possibility of dynamic threshold control was not considered.

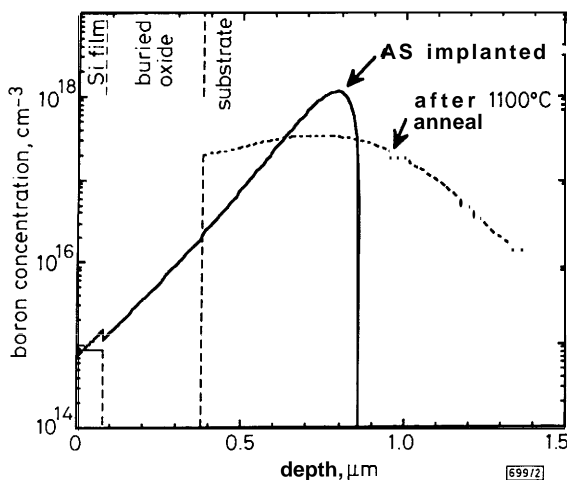

Fig. 2 *Doping profile predicted by SUPREM3 for backgate electrode implant*

Fig. 2 shows the doping profile predicted by SUPREM3 simulation for implantation of $^{11}B^{++}$ at a dose of $2\times10^{13}cm^{-2}$ and an accelerating voltage of 150kV (giving an ion energy of 300keV) into a silicon film 80nm thick overlying a buried oxide layer 300 nm thick: appropriate values for a 1 µm gate length technology generation [4]. The as-implanted profile was confirmed by spreading resistance profiling of an implant into a bulk n-type test wafer. Fig. 2 shows that implantation is capable of creating a backgate electrode with a doping concentration $>10^{17}$ cm^{-3} at the buried oxide interface while leaving a residual boron concentration $<10^{16}cm^{-3}$ in the silicon thin film. The latter value is low enough to avoid significant interference with subsequent well doping implants.

The Poisson equation solver in SUPREM3 was used to study the dependence of the subthreshold chardcteristics and V_T on V_B for *n*- and p-channel MOSFETs with the backgate electrode structure described above. A gate oxide thickness of 25nm was assumed, with n^+ and p^+ poly gates for the *n*- and *p*-channel MOSFETs, respectively [4]. Doping levels of $4\times10^{16}cm^{-3}$ and $5\times10^{16}cm^{-3}$ in the *n*- and p-wells provided $|V_T| \simeq$ 200mV at $V_B = 0V$, appropriate for 1V supply operation. The subthreshold swing S was 63mV/decade. $\Delta V_T/\Delta V_B$ was found to be 80mV/ V for $-3V < V_B <$ 3V. The $\Delta V_T/\Delta V_B$ ratio could be increased by using a thinner buried oxide, but only at the expense of degraded subthreshold swing and increased source/drain-to-substi-dte parasitic capacitance. For $V_B > 5V$, the bottom of the silicon thin film begins to invert, degrading S as the front gate loses control of the channel current. For $V_B <$ -5V a hole accumulation layer begins to form at the bottom surface of the silicon film, screening the channel from further increases in $|V_B|$. In this operating regime the MOSFET effectively becomes a partially-depleted device, and S is once again degraded.

Circuit application In a practical integrated circuit application, bias for the backgate electrode shown in Fig. 1 would be supplied through an on-chip charge pump circuit. It is therefore necessary to determine whether a useful range of *VT* adjustment can be provided with values of *VB* attainable with a charge pump. To this end, various CMOS ring-oscillator-driven charge pump circuits operating from 1 V supplies were simulated using SOISPICE [5]. To simulate the backgate electrode, a p-type 'substrate' was invoked in the LEVEL = 2 MOSFET model, with doping equal to that at the interface between the buried oxide and backgate electrode. Dickson's charge pump design [6] was used to maximise pump output for 1V operation. It was found that charge pump circuits could generate V_B values sufficient to restore $|V_T|$ = 200mV for initial $|V_T|$ values differing from the nominal 200mV target by as much as ±250mV.

Experiment: Prototype backgated n-channel MOSFETs were fabricated on SIMOX [4] substrates with the gate oxide, silicon film and buried oxide thickness specified above. The starting substrates were n-type wafers of 4Ωcm resistivity. The wafers received the backgate implant specified above in selected areas, following LOCOS isolation of device wells. The leakage between the backgate electrode and the substrate was just $30nAcm^{-2}$ at 5V reverse bias, low enough for charge pump generation of V_B. *No* separate well doping implant was used, so a relatively large negative V_B value of -1OV was required to obtain the design threshold of 200mV. A sensitivity $\Delta V_T/\Delta V_B$ of 8OmV/V was found for variations in V_B about this point, in agreement with the predictions of SUPREM3. Fig. 3 illustrates the ability of the backgate electrode to control the MOSFET drain characteristics

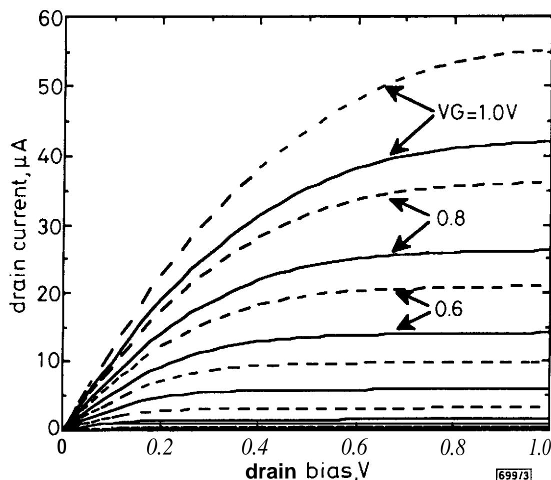

Fig. 3 *Drain characteristics for experimental backgated SOI MOSFET*

- - - $V_B = -9V$, —— $V_B = -10V$
V_G ranges from 0 to 1.OV in 0.2V steps

Conclusion: SUPREM3 simulation confirmed by fabrication of prototype experimental devices has shown that a simple junction-isolated backgate electrode, formed by boron implantation through the silicon film and buried oxide, can provide effective dynamic control of V_T for fully depleted SO1 CMOS operating from $\simeq$ 1 V power supplies.

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