Switched-Capacitor Bandpass Delta-Sigma A/D Modulation at 10.7MHz

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ABSTRACT

Two second-order bandpass delta-sigma A/D modulators have been implemented in a 0.8μ BiCMOS process [1] to demonstrate the feasibility of converting a 10.7 MHz radio IF signal to digital form. The circuits, based on switched-capacitor biquads, demonstrated 57dB SNR in a 200 kHz bandwidth when clocked at 42.8MHz, dissipating 60mW from a 5V supply.

I. INTRODUCTION

There is broad industrial interest in A/D conversion at the intermediate-frequency (IF) stage of a radio, because that allows digital channel-select filtering, gain control and demodulation. The robustness of the digital circuitry gives manufacturing advantages and allows the use of sophisticated algorithms, which are especially useful with digitally coded transmissions and where multiple transmission standards are in use. Because this is a new application area for A/D conversion the system-level trade-offs needed to specify the converters are still a matter of debate. This work contributes by demonstrating experimentally that it is feasible to make a fully monolithic converter with the bandwidth required for a per-channel GSM radio or several channels of IS-54 [2] and enough dynamic range to simplify gain-control and adjacent-channel rejection. It also suggests a preferred clocking scheme for high speeds.

We extrapolate from the experimental part to suggest that it is practical to build a converter able to cover an entire 1MHz band for narrowband personal communications basestations or the 1.25MHz that covers all of the North American cellular standards from IS-95 to AMPS, and with enough dynamic range to do all channel selection and gain control functions on the digital side.

For telephony there are two distinct variants of the radio design problem — one for base stations and the other for the terminals. For example, the base station is expected to handle several channels, while the terminal generally operates only on a single channel; on the other hand power constraints are tighter in the terminal. The converter we demonstrate is aimed at a single channel of GSM telephony and has low enough power for a terminal, and the wider-band converters we extrapolate to are intended for base stations.

The A/D conversion required can be done at baseband on quadrature channels (using a “zero-IF” receiver), but (for the multi-channel problem) that requires precision matching and (for both base

stations and terminals) is susceptible to a variety of DC instabilities and electromagnetic compatibility problems. Alternately a bandpass signal can be directly converted either with a conventional or noise-shaped converter. Noise-shaped (or $\Delta\Sigma$) converters, which we demonstrate here, consist of a filter and comparator in a feedback loop as in Fig. 1, and are oversampled. (that is, sampled well above the Nyquist rate for the *bandwidth* required). The type of filter used in the loop is a key determinant of the performance possible.

II. PRIOR ART

Monolithic bandpass delta-sigma modulators have been reported [3][4][5] with centre frequencies of 455kHz, 2MHz, and 50MHz, and with bandwidths of 10kHz, 30kHz and 200kHz respectively and resolutions of nine to fourteen bits. These bandwidths are suitable for broadcast and voice AM, IS-54 cellular telephony and GSM telephony respectively. Another device obtained a 55dB SNR performance with a 6.5MHz centre frequency [6] and 200kHz bandwidth using off-chip inductors as resonators.

Using oversampling with wideband signals necessarily implies fast clocking, so there is a question as to how wideband a monolithic realization can be. Brandt and Wooley showed that a 1MHz bandwidth is possible in the lowpass case with a MASH architecture [7], and Song demonstrated switched-capacitor (switched-C) bandpass filtering at 10.7MHz [8]. This work demonstrates in a second-order modulator prototype that a 10.7MHz bandcentre is possible, with 57dB SNR performance in a 200kHz band.

When channel-select filtering is to be performed after A/D conversion in a radio system it is of prime importance to have high linearity, or else strong interferers may intermodulate in the converter and mask the desired signal. This study focuses on switched-C technology because it is proven for high resolution and linearity at baseband and because it is a monolithic technology capable of delivering precision analog performance. Inductor- [6][9][10] or transconductor-based [5] technologies can be expected to dominate at very high speeds, but are more difficult in that they involve off-chip components or tuning; their linearity is also compromised by “intersymbol interference” effects in the pulse feedback used as well as in the loop filter. Switched-C should be expected to dominate up to some upper bandwidth limit, and this work helps estimate that limit.

This paper presents and compares (experimentally) two different types of second-order switched-C bandpass $\Delta\Sigma$ modulators. The two structures both use fully differential BiCMOS op-amps with continuous-time common-mode feedback, but employ different clock phasings to experiment

with trade-offs between active and passive sensitivities.

This paper is concerned with A/D modulation. To make a complete A/D converter decimation is also required. Brandt and Wooley have recently shown that this can be done at low power for a similar set of specifications: with 11.3MHz data and a 3V power supply they consumed only 6.5mW. [11] Extrapolating to our higher data rate suggests that 30mW should be sufficient.

II. MODULATOR DESIGN

The basic one-bit modulator consists of a quantizer and a loop filter as shown in Fig. 1 [12]. Traditionally the filter block would just be an integrator resulting in a first-order lowpass ΔΣ modulator. By choosing the loop filter [3][10][13] we can shape the noise away from any frequency band desired. Modelling the quantizer by a linear white noise source, (shaded area in Fig. 1) we can derive a noise transfer function $H_n(z)$ and a signal transfer function $H_u(z)$. In terms of the loop-filter gain $A(z)$[1] they are

$$H_n(z) = \frac{1}{1 + A(z)} \qquad \text{...(eq.1)}$$

and

$$H_u(z) = \frac{A(z)}{1 + A(z)} \qquad \text{...(eq.2)}$$

and the overall output is a superposition of shaped noise and signal

$$Y = H_n(z)N + H_u(z)U \qquad \text{...(eq.3)}$$

For high-order filters or spectrally rich inputs the quantization noise is approximately white, [14] so a deep notch in H_n makes for a good signal-to-noise ratio in a narrow band.

For a simple second-order BPΔΣ modulator with a centre frequency at one-quarter of the sampling frequency

$$f_o = \frac{f_s}{4} \qquad \text{...(eq.4)}$$

the filter response is given by $A(z) = -1/(z^2 + 1)$ giving noise gain $H_n(z) = (z^2 + 1)/z^2$ and signal gain $H_u(z) = -1/z^2$. The output spectrum of the resulting ideal modulator with an

1. A quantizer also has a signal-dependent equivalent gain, which we have included in $A(z)$.

input sine wave at midband is shown in Fig. 2. For the simulation a small random dither was added to the input (in practical designs thermal noise is sometimes exploited to do this) to whiten the quantizer noise and remove tones.

This particular loop filter, which is the one we implemented, has a precise mathematical relationship to the well-understood first-order lowpass $\Delta\Sigma$ modulator: a change of variable [15]

$$\hat{z} = -z^2 \qquad \text{...(eq.5)}$$

gives

$$\hat{A}(\hat{z}) = 1/(\hat{z} - 1) \qquad \text{...(eq.6)}$$

The mathematical properties of the first-order lowpass prototype delta-sigma converter using $\hat{A}(z)$ are fairly well understood, including a simple stability guarantee and properties of the limit cycles. These properties carry over to a bandpass version designed according to (eq. 5), with the square term in the substitution giving the bandpass modulator the behaviour of two interleaved first-order converters, each of them "highpass" because of the negative sign in (eq. 5).

This transformation gives our circuit the noise-shaping behaviour of a first-order lowpass converter, with 9dB improvement in SNR for each octave of oversampling. It is also the one that guarantees the stability of Longo's fourth-order circuit [4] and gives it 15dB/octave shaping.

FILTER STRUCTURE

There are many filter structures implementing a given $A(z)$, and with an ideal realization of the filter all of them would give modulators with identical behaviour. In the presence of errors in capacitor ratios and of finite gain and bandwidth in op-amps, though, they behave differently. The most important effect is that the positions of the filter poles are affected in different ways by these errors: if filter poles are at the wrong frequency (wrong angle, in the z-plane) then the noise notch (see Fig. 2) will not be properly centered, and if they move off the unit circle (wrong magnitude of the complex pole, in the z-plane) then the notch will be shallower. Fig. 3 plots effects of pole position on overall SNR. It is also known that the effects of poles moving inside the unit circle are subtly worse than those of moving slightly outside [16][17][18] because an "over-stable" filter allows "deadbands" where limit cycles persist, and this can cause intermodulation distortion.

The "lossless discrete integrator" (LDI) loop of Fig. 4 has its poles at the zeros of $1 - L(z)$, where $L(z)$ is the loop gain. The numerator of $1 - L(z)$ is $z^2 - (2 + R)z + 1$, and the equal coefficients

on the squared and constant terms force the roots to be exactly on the unit circle. This seems very desirable, since the noise notch of the modulator will then be very deep. We use a nominal value $R = -2$, for which the centre frequency should be $f_s/4$, but gain errors can affect this. Jantzi's modulator, and one of ours, use this structure. On the other hand, gain errors in either of the integrators contribute to frequency errors, which can be even worse for SNR (Fig. 3).

Our second version of the modulator uses a "Forward Euler" (FE) loop as shown in Fig. 5. It consists of two "delaying" integrators $1/(z-1)$ rather than the mix of delaying and non-delaying ($z/(z-1)$) integrators in the LDI structure. The second integrator has to be heavily "damped" with a feedback D because the basic FE loop is highly unstable, and the poles of the loop are at the roots of $z^2-(2+D)z+(1-R+D)$. We choose $R = D = -2$ to get a pole at $f_s/4$. The disadvantage of this circuit is that errors in R and D can now move poles above or below the unit circle; there is some compensation from the fact that gain errors in the first integrator and R have no first-order effect on notch frequency. More significantly, we show in the next section another offsetting advantage in that one of the op-amps used to implement the circuit can settle more quickly. The FE and LDI loops trade off active and passive sensitivities differently.

Longo [4] used a switched-C implementation of a pure delay to make the loop shown in Fig. 6, which has characteristic equation $z^2 - \alpha$. This is exactly the inverse of the LDI loop in the sense that the angle (frequency) of the poles is fixed, but the magnitude (notch depth) is sensitive to loop gains. This structure can only be used for the particular case of bandpass modulators centered at $f_s/4$.

SC FILTER DESIGN

The loops of Fig. 4 to Fig. 6 can be implemented in switched-C technology in a number of ways, resulting in different demands on the op-amps. We compare them first using an optimistic simple model of an op-amp as a pure transconductor, modelling the effects of finite op-amp gain and slew-rate in a second pass.

The LDI loop, in particular, can be implemented either with the timing used in [3], where both op-amps are connected together during settling or so that they are decoupled [19]. We decoupled the op-amps for settling, obtaining the modulator design shown in Fig. 7. (ignore clock phasings in parentheses "()" and connections shown as dashed lines at this point) Component values are as given in Table 1.

The settling behaviour of this circuit is analyzed using the simplified version in Fig. 8, where a single-ended representation of the second op-amp A2 is shown as connected in each phase. (A1 sees the same connections on the opposite phases) Notice that the amplifier has to simultaneously handle an input transient and drive a load on phase 1, and then does nothing on phase 2. This is inefficient, unless more complex circuitry is used either to multiplex a single amplifier [19] or to turn off power in the idle phases. Modelling the amplifier as a pure transconductor with conductance G_m the settling time-constant on phase 1 would be

$$\tau = \left(C_r + C_{lp} + \frac{(C_x + C_p)C_{i2}}{C_x + C_{i2} + C_p}\right) \Big/ \left(\frac{C_{i2}}{C_x + C_{i2} + C_p} G_m\right) \qquad \text{...(eq.7)}$$

where input and load parasitics C_p and C_{lp} play important parts. For our amplifier representative values are: $G_m = 2\text{mA/V}$, $C_p = 0.6\text{pF}$, $C_{lp} = 0.3\text{pF}$ and other values are as in Table 1, giving $\tau \approx 2.65\text{ns}$ so that 7τ settling will take about 18.5ns.

The second-order settling of the coupled structure of [3] makes a formula more cumbersome, but using the same component values a linear model settles to the same 0.1% in 22.4ns.

Longo's implementation uses the delay circuit of Fig. 10. The op-amps here also settle input and load transients simultaneously, so that broadly similar performance can be expected, though the loop gains are lower and hence settling should be slightly better. Both op-amps are active on both phases. Using the same op-amp with all load and integrator capacitors equal at 0.6pF (making them significantly smaller would compromise phase margin) gives $\tau = 1.95\text{ns}$. Some care has to be taken because the op-amp is open-circuit between clock phases.

The second filter topology that we chose to implement, using Forward Euler phasing, is very similar to the LDI: Fig. 7 shows both, with clock phasings for FE shown in parentheses where they differ from the LDI, and with the extra "damping" capacitor C_d shown connected with dashed lines. There is also a sign change in the overall feedback, shown with the comparator output signs in parentheses. The main advantage of this structure is that the op-amps settle their input transients on one phase, then drive a load on the next. The time-constant for A2 driving its load, which is large because of C_d, is

$$\tau = \left(C_r + C_d + C_{lp} + \frac{C_p C_{i2}}{C_{i2} + C_p}\right) \Big/ \left(\frac{C_{i2}}{C_{i2} + C_p} G_m\right) \qquad \text{...(eq.8)}$$

which, for our sample values, comes to $\tau = 2.5\text{ns}$. This is the worst-case time-constant for this circuit. and A1 is significantly faster because of its lower load. When only one op-amp contributes settling errors, the net effect is better by a factor of roughly two.

The advantage that LDI phasing has, of having the magnitude of the filter poles independent of capacitors, comes at the expense of connecting input and output on the same phase giving the op-amps only half a clock cycle to settle. With a 42.8 MHz non-overlapping clock each op-amp will have to settle in less than 11.7 ns, and amplifier transconductance will have to be higher than in the example. We designed with a nominal small-signal $G_m = 4\text{mA/V}$.

OP-AMP SLEWING AND GAIN

The effects of finite opamp gain, bandwidth and slew rate were considered when determining the equations that would predict the phase and magnitude errors in the two different biquads. The effects of finite gain and bandwidth on switched-C biquads for op-amps with zero output impedance were first investigated by Martin and Sedra [20] and the results were generalized to transconductance opamps by Ribner and Copeland [21]. Neither of these methods considered slew rate limited opamps or input and output parasitic capacitances.

Delta-sigma modulators differ in settling behaviour from linear filters in that the internal states are driven by a great deal of high-frequency energy from shaped quantization noise, and so slew on every cycle even with small input signals. For this reason we model the effect of slew-rate limiting as a loss of a few nanoseconds at the beginning of every cycle during slew, followed by linear settling. The transition from slew to linear settling is of course gradual, so we model the op-amp as having an “effective” transconductance $G_{m,\,\text{eff}}$ during settling, which is lower than the small-signal G_m.

The effects of op-amp bandwidth on overall performance are dominated by the worst-case settling studied in the previous section, but are affected by both amplifiers. Table 2 below summarizes, for the LDI case, the net effects on pole positions (both magnitude and angle) of DC gain A_0, finite slew rate SR and finite linear bandwidth ω_t. Slew rate and bandwidth both depend on load capacitance, so they are subscripted in the form $\text{SR}_{n,\,m}$ where n specifies the integrator (1 or 2) and m the clock phase. Op-amp non-idealities contribute to pole-magnitude errors M and integrator gain errors P, defined by

$$\frac{V_o(z)}{V_i(z)} = \frac{(C_{in}/C_i)P}{z - M} \qquad \text{...(eq.9)}$$

In the ideal integrator $M = P = 1$. Errors in the individual integrators then produce magnitude and angle errors in the overall poles according to the formula in the first row of the table. Notice that the gain R does not affect $|z|$, as we know for LDI. The second row of the table shows how finite gain affects M_n and P_n, while the third row shows the effects of slew rate and bandwidth (via $G_{m,\,\mathrm{eff}}$).

Auxiliary terms used in modelling bandwidth effects are

$$\omega_t = G_{m,\,\mathrm{eff}}/C_L \qquad \text{...(eq.10)}$$

$$\tau = (C_{in} + C_p + C_i)/(C_i\omega_t) \qquad \text{...(eq.11)}$$

$$\zeta = (\tau \mathrm{SR})/V_{\mathrm{step}} \qquad \text{...(eq.12)}$$

$$K = (1/\tau)\left(\frac{1}{2f_s} - \frac{V_{\mathrm{step}}}{\mathrm{SR}} + \tau - t_{ol}\right) \qquad \text{...(eq.13)}$$

ζ is a scaling factor for the slew rate errors; V_{step} is the expected step size for slewing, which we take to be the reference voltage for the A/D; K is the number of time-constants of linear settling available after penalizing for slew and the "non-overlap" time t_{ol}; τ is the linear settling time constant; C_{in} represents all the capacitors connected to the input of the opamp, not including the input parasitic; C_i is the integrating capacitor; C_p is the parasitic capacitance at the input of the opamp; C_{lp} is the parasitic capacitance at the output of the op-amp and C_L is the total capacitive load on the op-amp output, including parasitics and the feedback network. In the tables C_o refers to all the capacitors which are connected from the output of the opamp to ground, not including the output parasitic.

The errors for the FE biquad are given in Table 3 in a similar fashion.

OP-AMP AND COMPARATOR CIRCUITS

A fully differential folded cascode opamp with continuous time common mode feedback was designed in the $0.8\mu\mathrm{m}$ BiCMOS process (Fig. 12). An infinite input impedance was required for the switched-C filters to avoid charge leakage, so we used MOS inputs. PMOS devices were used so that the much faster NPN bipolar devices could be used as the cascoding devices that set the

second pole to roughly its f_t. The simulated parameters for the folded cascode opamp are given in Table 4.

An NMOS-NPN (non-folded) cascode has the potential for even faster operation, or for better power efficiency, but is more sensitive to bias errors. We chose to leave it for a later revision, and are fabricating a prototype.

The comparator (Fig. 13) was a version of an existing part [22] modified by replacing bipolar inputs with NMOS devices so as not to load amplifier A2 at DC. (which would reduce its gain and settling accuracy) It has approximately eight-bit accuracy at 200 MHz, which is sufficient for our modulators, since $\Delta\Sigma$ circuits are known to be tolerant of comparator offsets and hysteresis. It consumes 10mW.

The overall circuit consumes 60mW (experimentally). In a time-division multiple-access receiver application where it need only be active $1/8$ of the time the average power would be under 10mW.

EXPERIMENTAL RESULTS

Fig. 14 is a photomicrograph showing both the FE (labelled “SigDel2ph” on the layout in reference to the two-phase delay around the loop) and LDI (SigDelLDI) BP$\Delta\Sigma$ modulators. Test structures were also fabricated for an individual op-amp and a switched-C settling test circuit. The op-amp tested alone showed a DC gain of 55dB, and the settling tester responded to a 1.6V differential step with a 10% to 90% rise-time of 3.3ns; that included approximately 1.2ns of slewing.

A typical output spectrum, one for the LDI BP$\Delta\Sigma$ modulator when clocked at 45 MHz, is shown in Fig. 15a. It broadly matches the simulated spectrum in shape (with a fatter noise band attributable to the larger variance expected from using a larger number of bins), but has significant tone power well out of band at about $1/8$ and $3/8$ of the clock frequency. The FE modulator produces a very similar spectrum, as shown in Fig. 16a.

Fig. 15b and Fig. 16b are expanded in-band plots measuring in-band SNR and intermodulation distortion for the two modulators. Two input tones, each 6dB below the saturation level, were applied in-band. (this was also the case for Fig. 15a and Fig. 16a, but the two tones are too close to distinguish on that scale) Clock and input frequency generators were asynchronous, so the input tones are not confined to a single FFT bin, and there is also sideband power from both frequency sources. Note that the spectra in these experiments are obtained digitally, rather than (as is

commonly done) simply by running the digital stream into an analog spectrum analyzer. The latter technique can be misleading because it hides the effects of clock jitter.

In-band noise is evaluated by averaging noise power over the band of interest. The noise components are averaged over FFT bins of bandwidth $22.5\text{MHz}/32768 \approx 686\text{Hz}$. Intermodulation products are below the noise for the LDI case but peaks are clearly visible in the FE case (Fig. 16b) at about -60dB. The third-order intercept point is thus $+28\text{dB}$ relative to the saturation level for the FE case, and somewhat higher for the LDI.

The in-band spectra slope to the left, which shows that the notch is slightly low, and we attribute this partly to capacitor ratio errors and partly to finite DC gain and incomplete settling. The problem is much more evident for the LDI case, which we would expect from our settling analysis.

In order to separate the effects of DC errors and incomplete settling, bit streams were obtained for both modulators at several different clock frequencies. A Hanning-windowed 65536 point. FFT was performed on the bit streams and the notch frequency was determined to give the points plotted in Fig. 17. Assuming that the 55dB gain from the test op-amp applied to the modulators, a +0.3% error in the capacitor ratio Cd/Ci2 and +0.2% error in the capacitor ratio Cr/Ci1 were estimated to be the capacitor ratio mismatches, resulting in a small frequency error even at low clock rates. These mismatches are quite plausible given the small unit capacitor value we are using. The plot shows that settling is essentially complete below about 30MHz and that the FE structure is still good to 1% at the 42.8MHz clock needed for a 10.7MHz IF.

Signal levels were varied at a constant clock frequency of 20MHz, where settling is complete, producing the plot of SNR against signal level shown as Fig. 18. There is a large deviation from the straight-line behaviour predicted by the linear model and by simulations: this is similar to the characteristic already known for first-order lowpass $\Delta\Sigma$ modulators in the presence of a small offset, and which should be expected for second-order bandpass. It suggests that tones tend to be out-of-band at low input levels, making for anomalously good SNR.

Fig. 19 summarizes the effect of changing clock rate on SNR in a given bandwidth. At low clock rates there is insufficient oversampling to get good SNR, and when the clock rate exceeds about 40MHz the notch frequency drifts off-centre and reduces SNR again. The measurements were made with the signal 10dB below saturation (where Fig. 18 shows that we only have about 45dB of SNR) The best SNR is obtained for the FE structure near the nominal 42.8MHz, and is about 47dB relative to the -10dB input signal, giving a peak SNR of 57dB relative to the modulator's

saturation level. The curve shows experimental SNR together with the mathematical model of Table 2 and Table 3. The mathematical fit is not nearly as good as for Fig. 17 because SNR measurements are affected by non-ideal tone behaviour whereas notch frequencies are set accurately by the behaviour of the linear filter.

OBTAINING A 1MHZ BANDWIDTH

As mentioned in the Introduction, some base-station applications need bandwidths of about 1.2MHz. Pushing the technology of this paper to 80MHz clocking (as simulation suggests may be possible) would give an oversampling ratio of $40\text{MHz} / 1.2\text{MHz} = 33.3$, which is quite low. The high linearity requirements of digital radio may be a problem for the multi-bit or MASH approaches that tend to be used at low oversampling rates, but digital correction to the 20-bit level has recently been demonstrated for a three-state feedback A/D [23]. On the assumption that this is possible for bandpass conversion, and designing a noise transfer function according to the method of [3] with split notches and a conservative 5dB of out-of-band gain, Fig. 20 shows the SNR performance that can be expected for modulators of order four, six and eight. Although an eighth-order modulator sounds very aggressive, recall that it has the dynamics of a fourth-order lowpass converter, of which examples are in commercial use.

CONCLUSIONS

Switched-capacitor bandpass $\Delta\Sigma$ technology appears to be practical for A/D conversion of radio IF signals at 10.7MHz, although a production version of the chip would need an improved op-amp (particularly to improve slew rate, and also to reduce power consumption) to get the performance margin needed to cover process and temperature variation. We have initial simulations showing that an op-amp almost twice as fast should be possible in the same process, using a simple rather than folded cascode, and a test version is in fabrication.

A second-order modulator gives a 57dB SNR in a 200kHz bandwidth when clocked at the nominal 42.8MHz, but shows pronounced non-ideal noise behaviour. Using a fourth-order structure (shown to work at lower clock rates in [3] and [4]) with the high-speed technology demonstrated here should give improved bandwidth and SNR, which in turn should give more margin and flexibility to the system designer. A bandwidth of about 1MHz seems attainable with present technology, and at high order would benefit from the use of a three-level quantizer.

Forward-Euler switch phasing gives a significant speed advantage over LDI, and its sensitivity to ratio errors does not appear to seriously degrade SNR. High-order quantizers with high relative

bandwidths tend to be less sensitive to magnitude errors in the poles, so the FE structure should work even better there. A structure like that of [4][24] may have even better speed, but was not compared on the same process as the LDI and FE circuits. At high clock rates it is more important to design switched-C circuits for rapid amplifier settling than for low passive sensitivities.

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Figure Captions

Figure 1: Block diagram of delta-sigma modulator.

Figure 2: Output spectrum of ideal second order modulator. The abscissa contains 2048 bins.

Figure 3: Linear model prediction of SNR for a 2nd-order modulator which has errors in the magnitude and angle of its filter pole. (input at -6dB)

Figure 4: The LDI loop, where pole magnitude is capacitor-insensitive

Figure 5: The Forward-Euler loop.

Figure 6: The two-delay loop.

Figure 7: 2^{nd}-order BPΔΣ modulators in their differential form a) LDI modulator b) FE modulator use clock phasing in () and dashed lines.

Figure 8: Op-amp loading in our LDI structure which has op-amps settling in parallel rather than series

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Figure 12: Folded cascode op-amp with continuous time CMFB.

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Figure 15: Output spectrum of the LDI modulator when clocked at 45MHz. Two tone inputs each at -6dB a) output spectrum, abscissa contains 32768bins b) expanded view of in-band spectrum

Figure 16: Output spectrum of the FE modulator when clocked at 45MHz.Two tone input each at -6dB. a) output spectrum, abscissa contains 32768bins b) expanded view of in-band spectrum

Figure 17: Percentage error in notch frequency resulting from non-ideal OTAs. Points are experimentally measured and lines are mathematically predicted by equations in Table 2 and Table 3

Figure 18: SNR in a 200 kHz bandwidth centered at 5MHz while being clocked at 20MHz.

Figure 19: SNR in a 200kHz band centered at 1/4 the sampling frequency. (input at -10dB) Points are experimentally measured and line are mathematically predicted.

Figure 20: Simulated SNR versus input amplitude for 4^{th}-, 6^{th}- and 8^{th}-order 3-level modulators with an oversampling ratio of 33.

Figures

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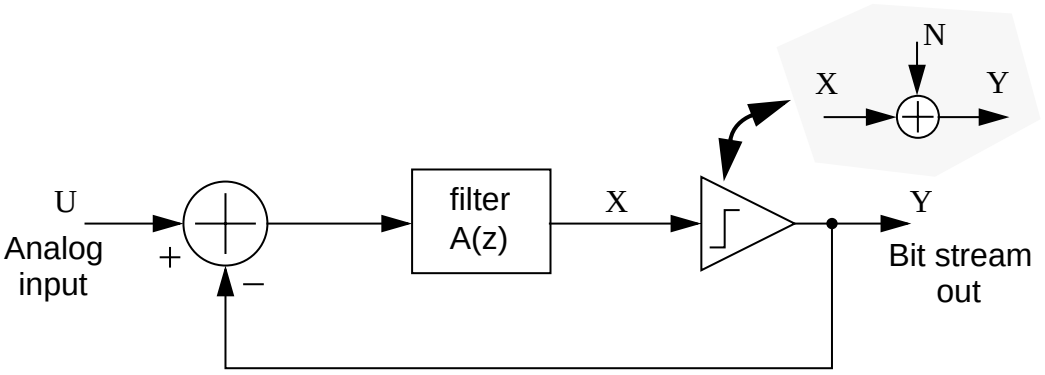

Figure 1 Block diagram of delta-sigma modulator.

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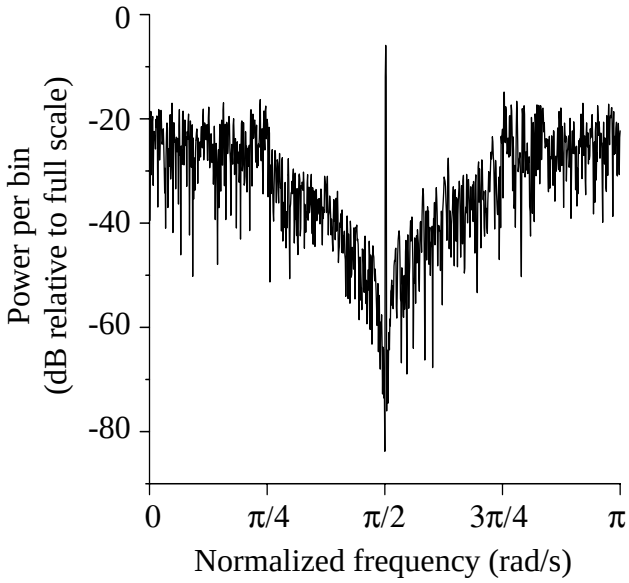

Figure 2 Output spectrum of ideal second order modulator. The abscissa contains 2048 bins.

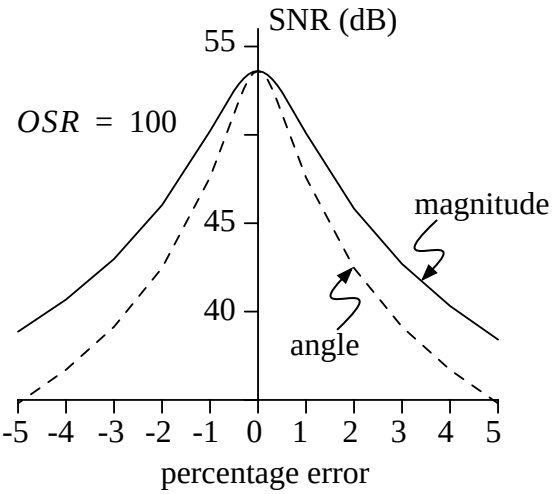

Figure 3 Linear model prediction of SNR for a 2nd-order modulator which has errors in the magnitude and angle of its filter pole. (input at -6dB)

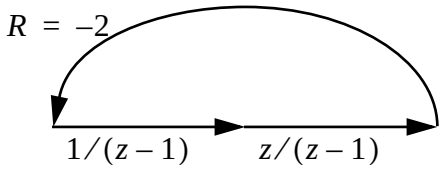

Figure 4 The LDI loop, where pole magnitude is capacitor-insensitive

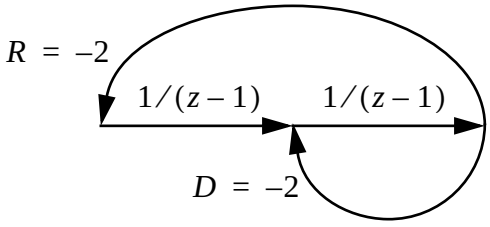

Figure 5 The Forward-Euler loop.

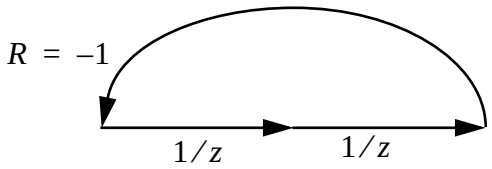

Figure 6 The two-delay loop.

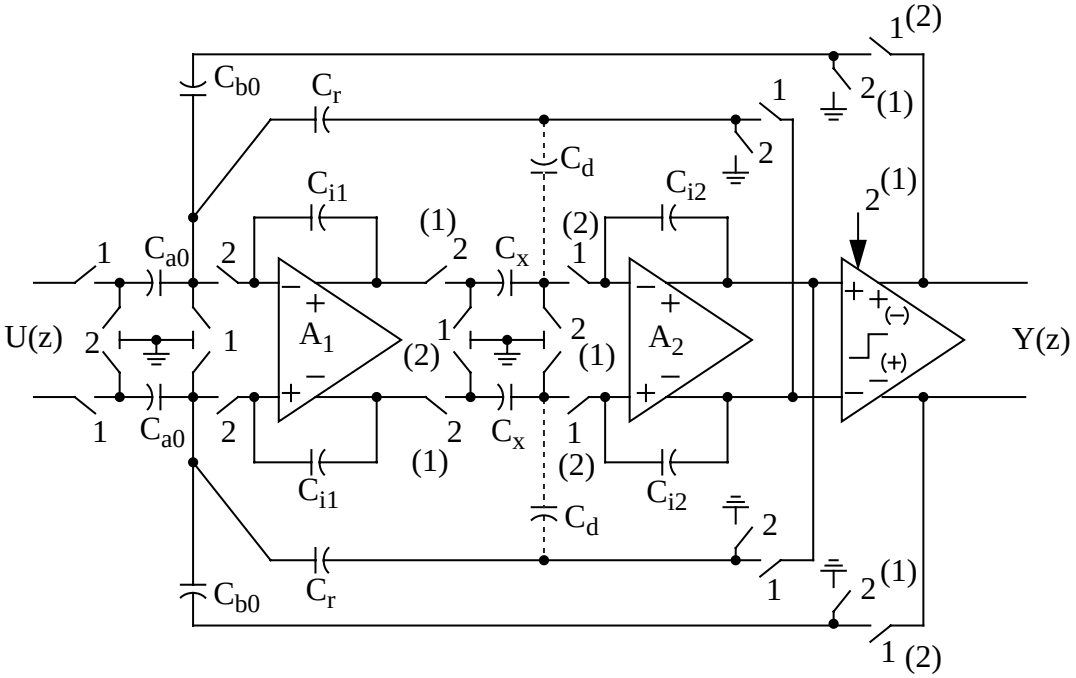

Figure 7 2nd-order BPΔΣ modulators in their differential form
a) LDI modulator
b) FE modulator use clock phasing in () and dashed lines.

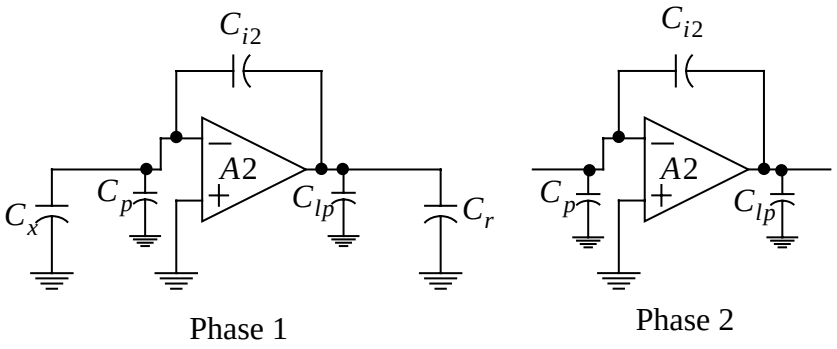

Figure 8 Op-amp loading in our LDI structure which has op-amps settling in parallel rather than series

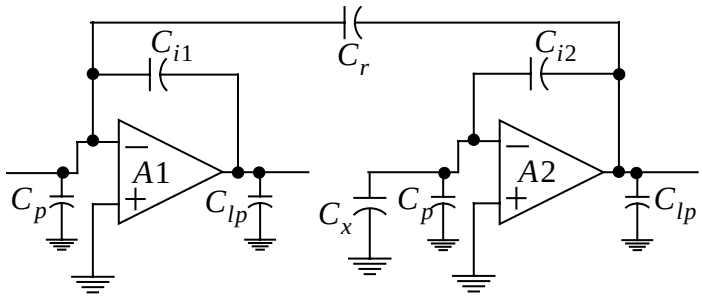

Figure 9 Op-amp loading in Jantzi structure.

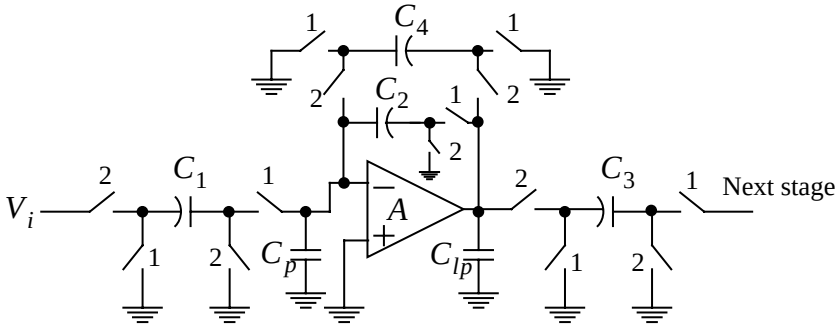

Figure 10 Unit delay circuit used in Longo's structure.

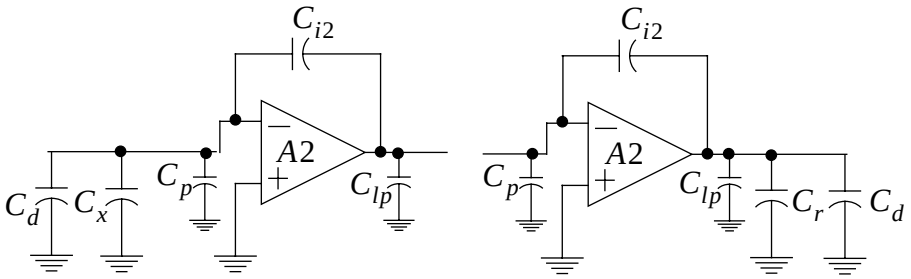

Figure 11 Worst case op-amp loading in FE structure.

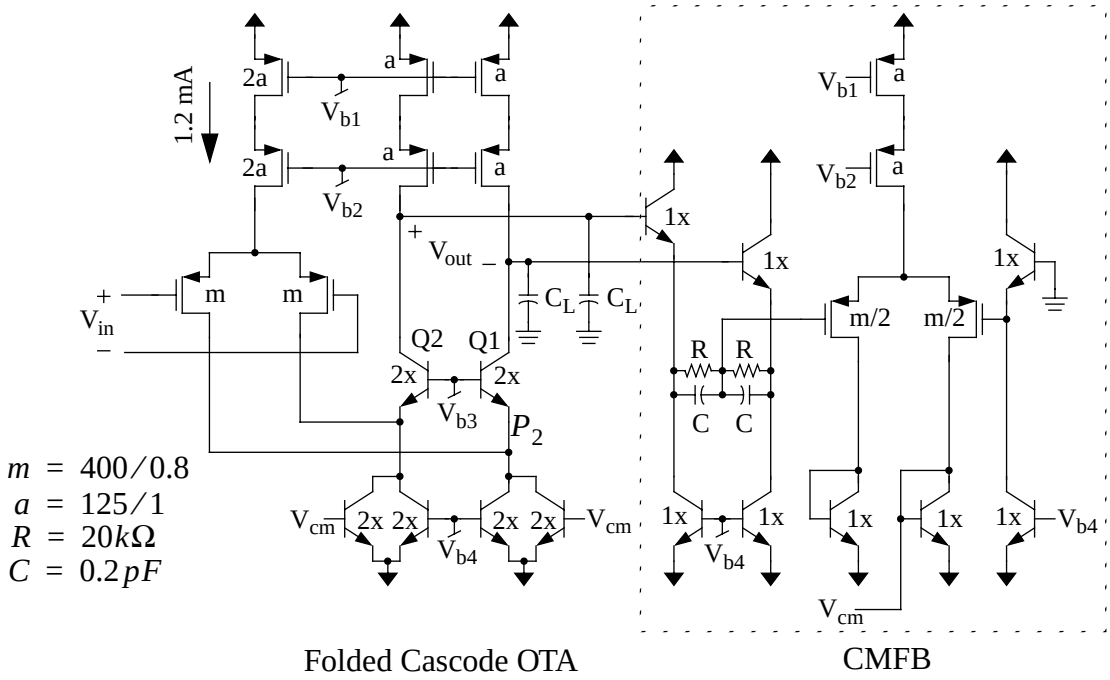

Figure 12 Folded cascode op-amp with continuous time CMFB.

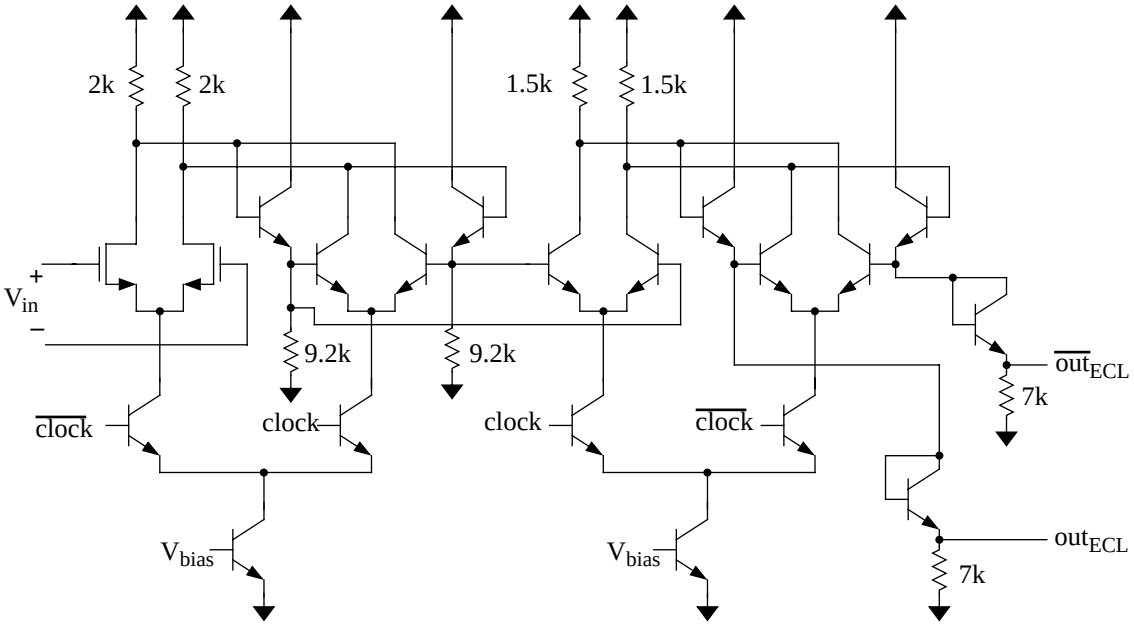

Figure 13 Pseudo-ECL latched comparator.

Figure 14 Photomicrograph of test chip
a) Folded cascode opamp
b) Switched-C unity gain configuration
c) Forward Euler BPDS modulator
d) LDI BPDS modulator

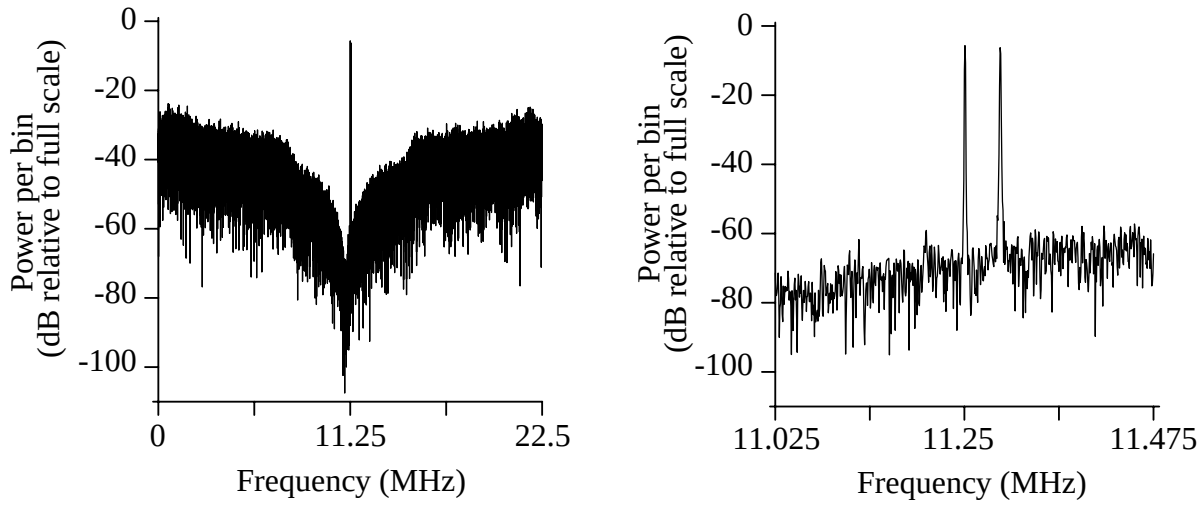

Figure 15 Output spectrum of the LDI modulator when clocked at 45MHz.
Two tone inputs each at -6dB
a) output spectrum, abscissa contains 32768bins
b) expanded view of in-band spectrum

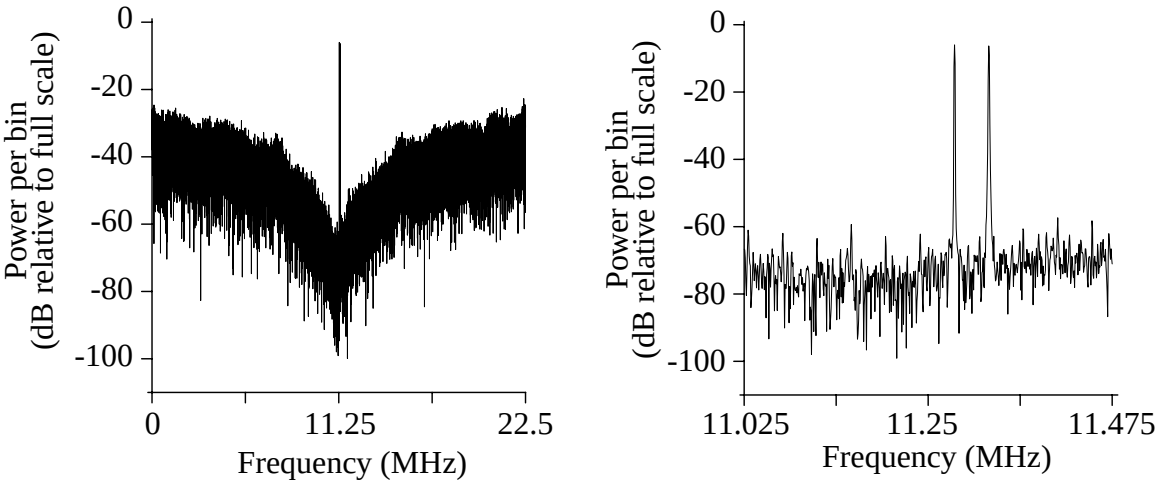

Figure 16 Output spectrum of the FE modulator when clocked at 45MHz.Two tone input each at -6dB.
a) output spectrum, abscissa contains 32768bins
b) expanded view of in-band spectrum

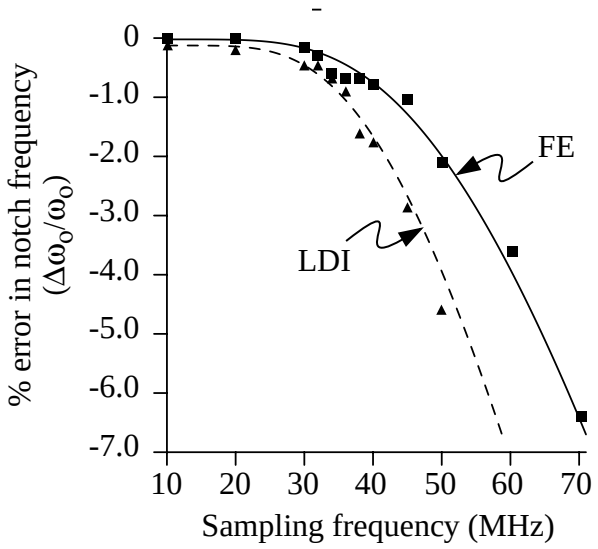

Figure 17 Percentage error in notch frequency resulting from non-ideal OTAs. Points are experimentally measured and lines are mathematically predicted by equations in Table 2 and Table 3

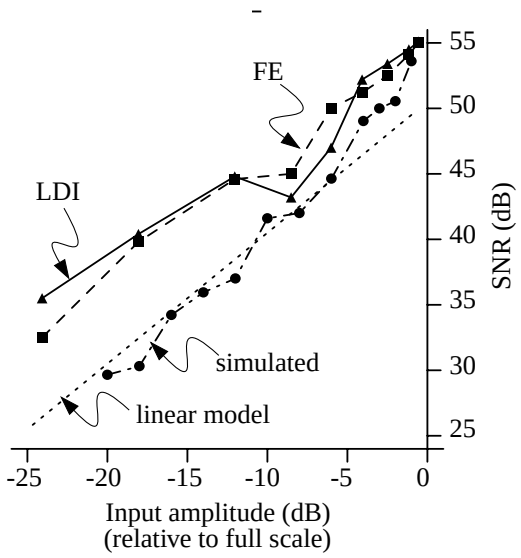

Figure 18 SNR in a 200 kHz bandwidth centered at 5MHz while being clocked at 20MHz.

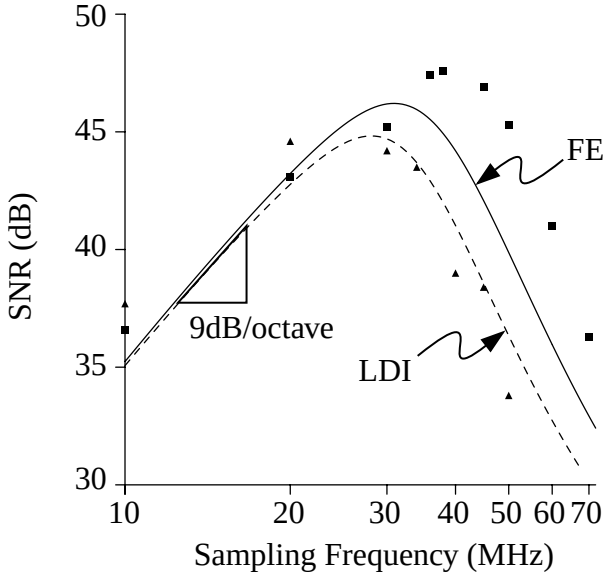

Figure 19 SNR in a 200kHz band centered at 1/4 the sampling frequency. (input at -10dB) Points are experimentally measured and line are mathematically predicted.

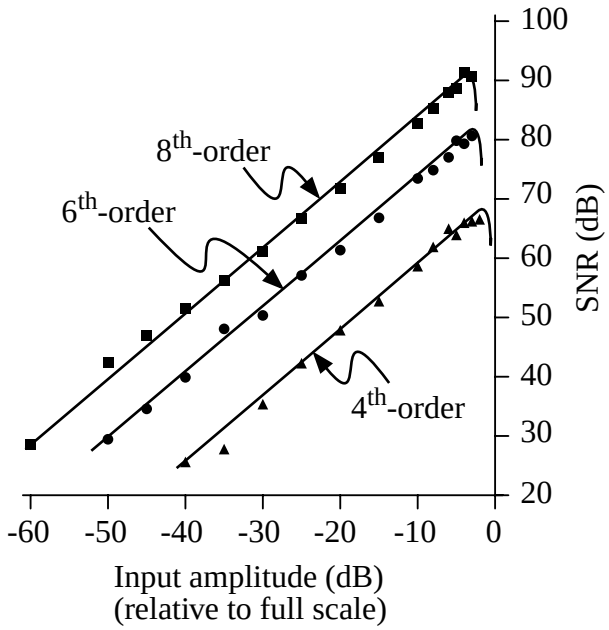

Figure 20 Simulated SNR versus input amplitude for 4^{th}-, 6^{th}- and 8^{th}-order 3-level modulators with an oversampling ratio of 33.

Tables

Tables

Table 1: Nominal capacitor values for both modulators

Component	C_{a0}	C_{b0}	C_{i1}	C_{i2}	C_x	C_r	$C_d^{\wedge}$
Value (pf)	0.2	0.2	0.5	0.3	0.5	0.6	0.6

Table 2: Effects of non-ideal OTAs on the LDI Biquad

$$\lvert z\rvert \approx \sqrt{M_1 M_2}$$ $$\Delta\theta \approx \left(\frac{(M_1 + M_2 - RP_1P_2)/2}{\sqrt{M_1M_2 - (M_1 + M_2 - RP_1P_2)^2/4}} \right)$$ $$R = \frac{C_r}{C_{i1}}\frac{C_x}{C_{i2}}$$	
errors due to finite DC gain	$$M_n \approx 1 - \frac{C_{in,n}}{C_{i,n}A_o},\ P_n \approx M_n - \frac{C_{i,n} + C_p}{C_{i,n}A_o}$$
errors due to finite BW and SR.	$$M_n \approx 1 - \lambda_n\zeta_n e^{-K_n},\ P_n \approx 1 - \alpha_n\zeta_n e^{-K_n}$$ $$\lambda_n = \frac{C_{o,n}(C_{in,n} + C_p + C_{i,n})}{(C_{in,n} + C_p)(C_{i,n} + C_{o,n} + C_{lp}) + C_{i,n}(C_{o,n} + C_{lp})}$$ $$\alpha_n = \frac{(C_{in,n} + C_p + C_{i,n})(C_{i,n} + C_{o,n} + C_{lp})}{(C_{in,n} + C_p)(C_{i,n} + C_{o,n} + C_{lp}) + C_{i,n}(C_{o,n} + C_{lp})}$$

Table 3: Effects of non-ideal op-amps on the FE biquad

$$z\| \approx \sqrt{M_1 M_2 + R P_1 P_2 - D P_2 M_1}$$ $$\Delta\theta \approx \left(\frac{(M_1 + M_2 - D P_2)/2}{\sqrt{\|z\|^2 - (M_1 + M_2 - R P_2)^2/4}} \right)$$ $$R = \frac{C_r}{C_{i1}} \frac{C_x}{C_{i2}},\ D = \frac{C_d}{C_{i2}}$$	
errors due to finite DC gain	$$M_n \approx 1 - \frac{C_{in,n}}{C_{i,n} A_o},\ P_n \approx M_n - \frac{C_{i,n} + C_p}{C_{i,n} A_o}$$
errors due to finite BW and SR.	$$M_n \approx 1 - \lambda_n \zeta_{n,2} e^{-K_{n,2}}$$ $$P_n \approx (1 - \alpha_n \zeta_{n,1} e^{-K_{n,1}})(1 - \lambda_n \zeta_{n,2} e^{-K_{n,2}})$$ $$\lambda_n = \frac{C_{o,n}}{C_{o,n} + C_{lp} + C_{i,n} C_p/(C_{i,n} + C_p)}$$ $$\alpha_n = \frac{C_{in,n} + C_p + C_{i,n}}{C_{in,n} + C_p + C_{i,n} C_{lp}/(C_{i,n} + C_{lp})}$$

Table 4: Simulated Performance of the Folded Cascode Amplifier

Parameter	Value
DC gain	57dB
Unity-gain frequency	500MHz
Phase-margin	75^o
Settling time to 0.1%	9.0ns
Slew-rate	1000V/μs
Differential output range	5.2V
Power consumption	26mW
measurements for a 1pF load capacitor	