A 100 Mb/s BiCMOS Adaptive Pulse-Shaping Filter

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***Abstract*— With the growing demand for high-speed transmission of digital data, there is a challenge for utilizing the existing copper plant as the transmission medium, especially for short-hop links. This medium offers a lower cost to a fiber medium, but requires more sophisticated electronics to account for electromagnetic emissions, cross-talk, and cable loss. These include pulse shaping filters, cross-talk cancelers, and equalizers. To maintain system cost at a minimum, analog solutions are preferred. In this paper a continuous-time tunable biquad implemented in a 0.8 μm BiCMOS process and configured as an adaptive pulse-shaping filter is described. The biquad is tunable over the range 10-230 MHz with variable Q factors. It is composed of five transconductance-C integrators each dissipating a static power of 10 mW at 5 V. A method for adapting the filter's pole-frequency and Q-factor while servicing 100 Mb/s NRZ data is presented together with experimental results.**

I. Introduction

APPLICATIONS such as high-speed data communications over a copper channel or small area, low power wireless communications require analog circuits such as pulse-shaping filters, equalizers, cross-talk cancelers, and others. To accommodate the desired application, these circuits usually resort to leading edge technologies and thus suffer from large variations such as temperature, bias errors, parasitics, and process tolerances. Consequently, a tuning mechanism is required to compensate for these variations. While element-matching dependent tuning schemes such as master-slave phase-locked loops might be possible, analog adaptive filters are more attractive as they are less sensitive to matching and parasitic effects and can also track load and signal variation.

Unlike digital adaptive filter technology, which is now commercially mature, analog adaptive filter technology is still mostly experimental. However, an analog approach offers higher signal processing speeds, lower power dissipation, and smaller integrated circuit area. Preliminary demonstrations of analog adaptive filters have been presented in [1]–[4]; yet these achievements focused on architecture and were mostly low speed. Progress in practical, efficient yet simple algorithms for adapting high-frequency filters is required and must be demonstrated in an application for the technology to be commercially viable. This paper presents experimental results to verify a new adaptation technique and illustrates circuit practicality of a 100 Mb/s pulse-shaping biquad where the output signal is used to automatically tune the filter pole-frequency and the Q-factor.

An adaptive filter consists of a programmable filter whose coefficients are automatically tuned using an update algorithm such as the least mean square (LMS) algorithm. The LMS algorithm computes the correlation between the response error signal and the filter gradient signals. This paper explores the implementation of very simple coefficient update techniques. Specifically, comparators are used to make sample measurements on the filter output(s), based on known signal characteristics, to obtain an error signal for coefficient computation. In other words, given a set of unknown filter parameters, we obtain a set of sample measurements to provide sufficient information to solve for these parametersIn addition, gradient signal computation is avoided to simplify the hardware. While the common adaptation techniques employ training sequence, the approach presented here allows a simplified on-line blind adaptation. However, it should be noted that it is based on a restricted range of possible inputs and is most applicable for tracking reasonable process and channel variations. Inputs in this category are found in data communication applications.

In Section II, background material on pulse-shaping and the adaptive tuning schemes are presented. Specifically, two sample measurements are used to tune two filter parameters. Also, the effect of DC offsets on the performance of the techniques is discussed. In Section III, the transconductor, which is the basic building block of the prototype filter, is described. In Section IV, the biquad filter and additional on-chip circuitry required for testing the adaptive pulse-shaping system are discussed. Experimental results are provided in Section V.

II. Adaptive Pulse-Shaping

In high-speed data communications over a copper channel, a pulse-shaping filter or pulse conditioning mechanism is required to ensure transmitted power complies with electromagnetic interference (EMI) regulations (for example, [5]). Typically for a given data-rate and signal-line code, a time-domain mask for the transmitted pulse and/or a frequency-domain mask for the output power must be adhered to. In Fig. 1, a 100 Mb/s NRZ pulse, together with some experimentally measured pulse-shaping filter outputs, is shown.[1] The signal template is also shown shaded in the figure. This application lends itself to our tuning strategy.

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[1] Due to output buffer attenuation, the levels depicted are 35 dB below filter internal levels.

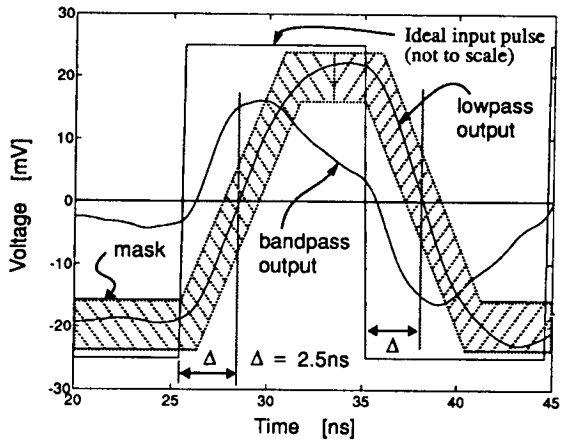


Fig. 1. Lowpass and bandpass biquad outputs for 100 Mb/s NRZ data including the time-domain pulse shaping mask.

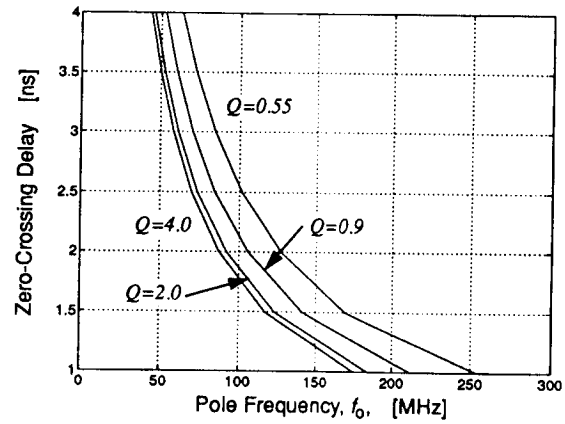
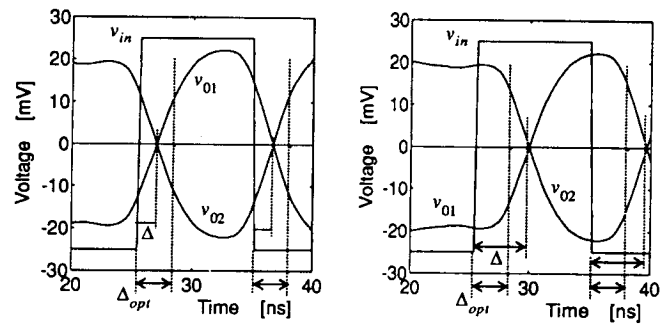


Fig. 2. Zero-crossing delay as function of f_o and Q.



(a) (b)

Fig. 3. Illustrating the details when the filter is mistuned: (a) too fast—zero-crossing comes early; (b) too slow—zero-crossing comes late.

For data communication signaling, the filtered output is strongly related to the step response of the filter. Consider a second-order filter or biquad whose lowpass and bandpass transfer-functions are

$$T_{LP}(s) = \frac{K\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \tag{1}$$

$$T_{BP}(s) = \frac{K\omega_o s}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}. \tag{2}$$

The step response for this biquad is characterized by the parameters ω_o, Q, and K. For a given gain term, K, the tuning algorithm must extract and process ω_o and Q from the filter output.

A. Adaptation of Filter f_o

Observe from Fig. 1 the lowpass output zero-crossing (also the midpoint transition for differential signaling) is delayed from the input zero-crossing. This delay, Δ, is inversely related to both ω_o and Q as shown in Fig. 2. Notice that for constant Q, the relationship between ω_o and Δ is monotonic, thus simply monitoring delay time is sufficient to determine whether the pole frequency is in error. As shown in Fig. 3, a filter mistuned too fast ($f_o > f_{o,\text{opt}}$) will exhibit an output zero-crossing that is early ($\Delta < \Delta_{\text{opt}}$), while a filter mistuned too slow ($f_o < f_{o,\text{opt}}$) will exhibit a zero-crossing that is late ($\Delta > \Delta_{\text{opt}}$) where $f_{o,\text{opt}}$ and Δ_{opt} are the optimal filter pole frequency and delay, respectively. The monotonic relationship in Fig. 2 also guarantees that only a single solution for a given ω_o, Δ pair exists at a particular filter Q. Thus, the adaptive algorithm error signal can be simply obtained by computing the time difference between Δ_{opt} and Δ. It should be mentioned, however, that for the special case where f_o is mistuned extremely fast and Q mistuned extremely high, a condition where more than one zero-crossing in the output pulse may occur resulting in a nonmonotonic relation and hence a local minimum in the adaptation performance. For example, if the overshoot in the step response is larger than 50%, then at high f_o values, multiple zero-crossings can occur which could result in adaptation error.

Since the relationship between pole frequency and delay time is monotonic, the sign of the error signal is sufficient to determine in which direction to tune the pole frequency. Therefore the gradient signal is not required allowing a simplified algorithm as follows: Consider the low-to-high (LH) transition of the data pulse in Fig. 3(a). Comparing v_{o1} to v_{o2} (i.e., $\text{sgn}\,[e_{f_o}(k)] = \text{sgn}\,[v_{o1}(t) - v_{o2}(t)]$) at the nominal delay time results in digital "1". This result indicates the filter is mistuned too fast and f_o should be decreased. Using a binary set of ± 1 and defining $F_o(k)$ to be a digital word applied to a DAC which controls the filter pole-frequency, the algorithm can be accomplished by evaluating the following expression for each data transition:

$$F_o(k+1) = F_o(k) + data(k) \oplus \text{sgn}\,[e_{f_o}(k)]\,. \tag{3}$$

Here the symbol $\oplus$ denotes an exclusive "or" gate, the summation is implemented using an up/down (U/D) binary counter, and the time index k does not represent successive system clock periods but instead represents successive comparator clock sample instants which take place only after the occurrence of data transitions. In other words, the above expression is evaluated for both a LH and high-to-low (HL) transition of the data stream and provides equivalent actions for both transitions under ideal conditions. The length of the counter controls the integration time constant or convergence time. The DAC provides analog DC updates for the coefficient; the resolution of which governs the size of the steady-state limit

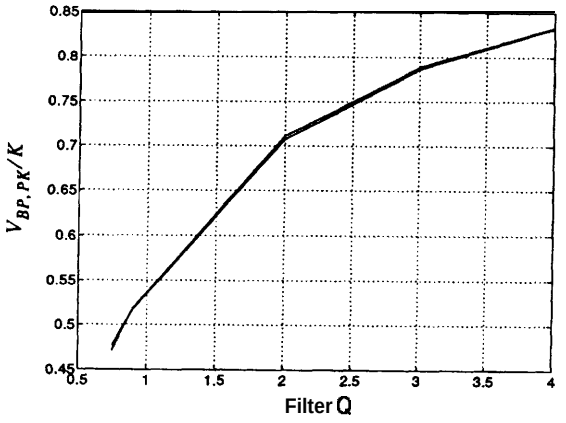


Fig. 4. Normalized bandpass peak level versus Q for $f_o = 10$, 85, 100, and 200 MHz.

cycle about the optimal coefficient value once convergence is attained.

B. Adaptation of Filter Q

Observe from Fig. 2 that delay time is a function of both pole frequency and filter Q-factor. Hence if the filter Q is in error, the algorithm may be optimized at an incorrect value for f_o. Moreover, a mistuned Q value will result in signal shape variations (for example ringing when Q is high) which could violate the EM1 template. For both these reasons, the Q-factor must also be tuned.

The rate of change (slope) of the biquad step response rises as the lowpass output increases and falls as this output reaches steady-state. In between, the slope will attain a peak level that will occur approximately when the filter output pulse crosses zero as can be noted from Fig. 1. The slope output represents the biquad impulse response and can be easily obtained from the bandpass output. As can be seen from Fig. 4, the bandpass peak level, $V_{BP,PK}$, dominantly depends on Q and a monotonic relation occurs between $V_{BP,PK}$ and Q.[2] Hence, simply comparing bandpass output, $v_{o,bp}$, to a reference level, V_{REF}, at the optimal delay time is sufficient to determine the Q error signal, $e_Q(k)$, and the tuning direction without the need for a gradient filter. As before, depending on the compared outcome, a DAC controlled by an U/D counter is used to automatically adapt the filter Q coefficient. Quantitatively, for differential signaling with $Q(k)$ the digital word applied to the DAC controlling filter Q, we have:

$$e_Q(k) = \begin{cases} \left(\frac{V_{\mathrm{REF}}}{2} - \frac{v_{o,bp}}{2}\right) - \left(\frac{-V_{\mathrm{REF}}}{2} - \frac{-v_{o,bp}}{2}\right) \\ \quad = V_{\mathrm{REF}} - v_{o,bp} \Leftrightarrow v_{o,bp} > 0 \\ \left(\frac{-V_{\mathrm{REF}}}{2} - \frac{v_{o,bp}}{2}\right) - \left(\frac{-V_{\mathrm{REF}}}{2} - \frac{-v_{o,bp}}{2}\right) \\ \quad = -V_{\mathrm{REF}} - v_{o,bp} \Leftrightarrow v_{o,bp} < 0 \end{cases} \quad (4)$$

$$Q(k+1) = Q(k) + data(k) \oplus \mathrm{sgn}\,[e_Q(k)]. \quad (5)$$

[2] In the special case of very high Q, a local minimum can occur as mentioned in the previous section.

C. DC-Offset Effects

It is known that DC offsets in an adaptation algorithm lead to residual mean-squared error [1]–[4]. That is, the coefficients converge to a biased estimate of the optimal location. However, since most of the adaptation algorithm is digital, a single offset source can be lumped at the input of the comparators which models comparator input-offset and signal differential offset.

Consider the f_o tuning scheme. In a fully differential implementation, the comparator output depends on the difference between the two filter half-circuit outputs and therefore any common-mode offset will not cause error. However, a differential offset alters the symmetry in the location of the output zero-crossing between a LH and a HL transition of the input data. Consequently, inconsistency will occur in the action defined by (3) between consecutive data transitions. As a result, the U/D counter will not advance in either direction and the coefficient controlling f_o will stabilize above or below $f_{o,\mathrm{opt}}$ depending whether the filter was mistuned initially fast or slow. Thus a nonreachable offset-dependent dead-band about the optimal coefficient value will exist. The effect of DC offset will be manifested when the filter f_o is near the nominal location such that the term $\Delta_{\mathrm{opt}} - \mathrm{A}$ is small and the offset term dominates. When the term $\Delta_{\mathrm{opt}} - \mathrm{A}$ is large, the algorithm will yield a correct response.[3]

It is possible to let the algorithm locate the dead-band as follows. Once invalid data is detected between a LH and HL transitions, the algorithm is modified to force the coefficient update in the same direction the update exhibited when valid comparator output was obtained. This process will lead to a limit cycle about the optimal coefficient value whose size will depend on the dead-band and not the resolution of a single DAC LSB as would occur in the ideal case. The effect of this limit cycle on performance is further discussed in Section V.F.

For the Q tuning mechanism, ideally a fully balanced comparator is required to realize the comparison in (4). Just as in the f_o tuning mechanism, it can be inferred that unlike a common-mode offset between the signal and reference level, a differential offset will lead to inconsistency between resultant actions for the data transitions and lead to the same dead-band convergence behavior discussed above.

III. The Transconductor

The preferred integrator or filter building block for high frequency filters is a transconductance-capacitor ($G_m - C$) element and is the technology style adopted in the biquad. Tuning of the biquad is achieved by varying the element's transconductance, G_m, and hence the integration time-constant, C/G_m, which defines the frequencies of the filter poles or zeros. However, common transconductors suffer from a low tuning range that is just larger than the process spread [6]–[14], namely on the order of 1-2 in a CMOS process, 2–4 in a BiCMOS process and 2-5 in a Bipolar process.

[3] It can be shown that if the offset term is larger than twice the product of $\Delta_{\mathrm{opt}} - \Delta$ and the rate of change of the lowpass output signal at the zero crossing, the dead-band will occur.

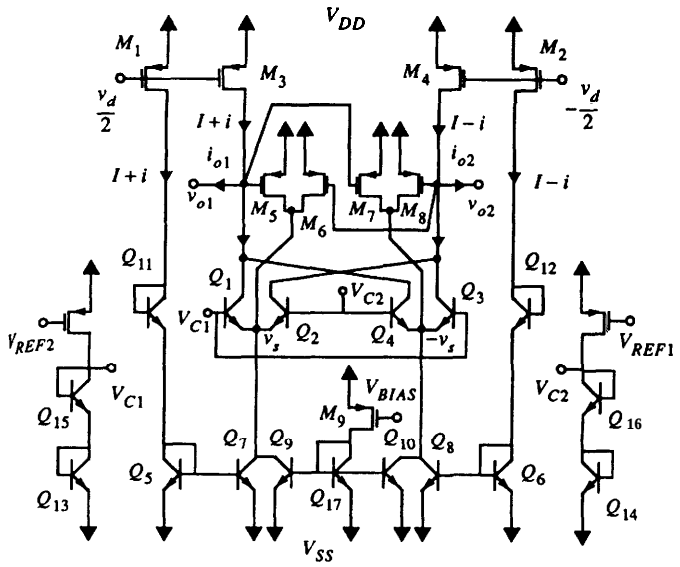


fig. 5. The BiCMOS transconductor.

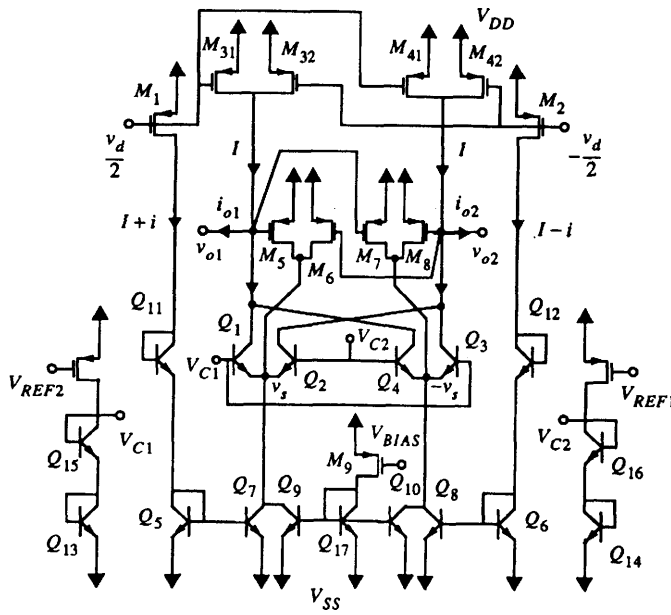


Fig. 6. The **second** BiCMOS transconductor.

To achieve a wide tuning range, a Gilbert multiplier was used for current steering $(Q_1$–$Q_4)$ as shown in Fig. 5 [15]. The transconductor consists of two input stages: the first formed by M_1 and M_2 and the second formed by M_3 and M_4. The differential signal current appearing at the emitter terminals of Q_1, Q_2, and Q_3, Q_4 is shunted by the multiplier and appears at the transconductor output scaled by the multiplier bias voltage difference, V_{C2}–V_{C1}, while the common-mode current components are unaltered. Letting g_m represent the small-signal transconductance of the input devices M_1–M_4, the overall transconductance can be shown to be given by [16], [17]

$$G_m = \frac{1}{2}\left[1 + \tanh\left(\frac{V_{C2} - V_{C1}}{2V_T}\right)\right] g_m. \qquad (6)$$

The transconductor in Fig. 5 provides only "2-quadrant" operation for transconductance tuning as evident from (6). To provide a transconductor that can be tuned for "4-quadrant" operation, consider Fig. 6, which is similar to Fig. 5 in all respects with the exception that the second differential input stage is replaced by the input stage consisting of the PMOS transistors M_{31}, M_{32}, M_{41}, and M_{42}. These transistors have their aspect ratios *half* the aspect ratios of the transistors M_1 and M_2. In the IC layout, each of the transistors M_1 and M_2 consist of two parallel transistors each matched to the transistors comprising the second input stage. For the circuit in Fig. 6, the transconductance is given by

$$G_m = \frac{1}{2}\tanh\left(\frac{V_{C2} - V_{c1}}{2V_T}\right) g_m. \qquad (7)$$

Notice that while this transconductor can be tuned for both Positive and negative values for G_m, it provides half the maximum G_m value of that in Fig. 5 at similar quiescent power dissipation. Hence when optimizing for speed for a specified power dissipation, transconductors or integrators realized using the topology of Fig. 6 should only be used where "4-quadrant" Operation is required, such as for cancelling transconductor finite output conductance as discussed in Section IV.

Observe from (6) and (7) that the entire tuning range spans a tuning control voltage range of $\pm 4V_T$. For this reason the transconductors in Figs. 5 and 6 each include the two buffer circuits shown on either side of the transconductors. These circuits expand the tuning control voltage span to ± 1.75 V between terminals V_{REF1} and V_{REF2}. In addition, the buffers provide isolation between the control DC sources and any components of the AC signal that appear at V_{C1} and V_{C2}, as well as a low impedance load to AC ground.

A. Linearity

Transconductors feature low input-stage linearity since they lack local feedback. To obtain reasonable linearity, we made use of the approach in [14]. Specifically, the input-pair tail bias current sources were removed as evident from Figs. 5 and 6. For matched input MOS devices obeying the ideal square law expression, it can be shown that the transconductor output current is linear with respect to the input signal voltage. When the input devices depart from a square law expression, linearity degrades. However, for the devices implemented, the short-channel effects enhance linearity especially at high overdrive voltage, $V_{GS} - V_t$, [14], [18]. The net result is satisfactory linearity as will be noted in from Section V-C.

Finally, note that the tuning mechanism relies on current steering rather than on the commonly used input-stage bias adjustment. With this approach, tuning does not affect the bias conditions of the input stages and hence *input-stage* linearity is preserved throughout the tuning range.

B. Noise

In this design, noise was not a major concern as a signal to noise ratio (SNR) in the range 30-40 dB is sufficient for the pulse-shaping application. However, in other applications noise can be an issue. It should be apparent that for similar input levels, the "2-quadrant" transconductor will display

better noise performance than the "4-quadrant" transconductor due to its higher signal gain. For the transconductors described here, the major source of noise comes from the base resistors of the BJT's Q_1–Q_{10} as they exhibit high gains to the output. It can be shown that the differential output noise is concave with a maximum at the extremes of the tuning range (dominated by Q_5–Q_{10}) and a minimum at mid-range (dominated by Q_1–Q_4) [16]. The ratio between maximum to minimum noise is about 8 dB. Thus relative to transconductors that are tunable by adjusting bias current for which noise drops as G_m is tuned for lower values, for our transconductor output noise does not reduce, implying SNR degrades as G_m is tuned below mid-range.

C. Common-Mode Feedback

Choosing to eliminate the current source in the input stages to enhance linearity implies the common-mode gain increases. In fact, it can be easily shown that the common-mode gain of the transconductors in Figs. 5 and 6 would be comparable to the differential gain when the transconductors' second input stages are connected as current-source load devices rather than input devices. This undesirable common-mode gain was the major reason for the second input stages. For matched input devices, the transconductor common-mode signals cancel at the output for ideally zero common-mode gain. In a practical realization, the transconductor common-mode gain would only appear as a mismatch error. Thus, a common-mode feedback (CMFB) circuit was still required to stabilize the output common-mode level.

The CMFB circuit chosen for the prototype transconductor is shown in Figs. 5 and 6 and consists of the PMOS transistors M_5–M_9. Each pair of MOS devices M_5, M_6 and M_7, M_8 sense the transconductor output voltage to produce a common-mode current component that is referenced to that produced by M_9. Since transconductors run at equal input and output signal swings, and since the devices M_5–M_8 are biased similar to the transconductor input transistors M_1–M_4, the devices M_5–M_8 should accommodate the entire transconductor output swing.

Unfortunately, the half-circuit outputs v_{o1} and v_{o2} suffer from nonlinearity due to the CMFB circuit which has nonzero differential to common-mode conversion. This signal conversion results in a common-mode current that depends on the differential signal. When fed-back to the transconductor (at node v_s), this error current will force some asymmetry between the two half outputs [16]. This asymmetry results in distortion on each of the outputs that is more severe when the devices obey the ideal square law relation and less severe when the devices are modeled using the short channel expression [14]. Fortunately the overall differential output v_o, will be distortion free as the distortion is common to both outputs.

D. Output Resistance

To determine the output resistance of the transconductor in Figs. 5 or 6, consider the BJT transistors Q_1 to Q_4 with output resistance $r_{oi} = V_A/i_{Ci}$, where V_A is the BJT early voltage. Assuming that the output resistance of the current sources Q_7–Q_{10} is infinite, using Kirchoff's current law at nodes v_s and v_{o1} for $v_{o1} = -v_{o2}$, the differential output resistance looking down into the Gilbert cell can be shown to be given by

$$R'_{od} = \frac{V_A}{I}\left[1 + \cosh\frac{(V_{C1} - V_{C2})}{V_T}\right]. \tag{8}$$

If the output resistances of the current sources Q_7–Q_{10} are taken into consideration, these have little effect on the result in (8) since they are in parallel with the multiplier BJT's emitter resistances.

The variation in R'_{od} as function of the tuning voltages is quite severe and might result in a local minimum when the element is used in an adaptive system. However, the transconductor differential output resistance, R_{od}, is the parallel combination of R'_{od} and the MOS differential output resistance which is much lower than R'_{od}. Thus at low settings for filter Q (low transconductor DC gain suffices) the effect is acceptable, however, this effect will become more severe as one connects a self-connected transconductor in parallel and tunes for negative transconductance to enhance filter Q (higher transconductor DC gain).

IV. Biquadratic Filter and Peripheral Circuitry

To determine the feasibility of adaptive analog filters in practical applications, a fully tunable biquad was implemented using the transconductors of Figs. 5 and 6 as shown in Fig. 7. The load capacitance 2C includes: 80 fF poly-poly capacitors, 104.2 fF MOS gate and drain-source capacitance, 56.5 fF wire capacitance and 175.8 fF BJT collector-substrate capacitance for a total of 417 fF. In Fig. 7, the G_ms represent the transconductance parameters of the transconductors. Letting g_os represent the respective transconductor's output conductance, it can be shown that the transfer functions corresponding to the bandpass and lowpass outputs, respectively, are

$$\frac{X_2}{U} = \left\{\frac{G_{mi}}{c}s + \frac{G_{mi}}{C^2}(g_{o12} + g_{ob}) - \frac{1}{C^2}G_{m21}G_{mb}\right\} \Big/ \left\{s^2 + \frac{1}{C}(G_{m22} + g_{o22} + g_{oi} + g_{ob} + g_{o12} + g_{o21})s + [(g_{o22} + g_{oi} + g_{o21} + G_{m22})(g_{o12} + g_{ob}) + G_{m12}G_{m21}]/C^2\right\} \tag{9}$$

$$\frac{X_1}{U} = \left\{\frac{G_{mb}}{c}s + \frac{G_{mi}G_{m12}}{C^2} + \frac{(g_{o22} + g_{oi} + g_{o21} + G_{m22})G_{mb}}{C^2}\right\} \Big/ \left\{s^2 + \frac{1}{C}(G_{m22} + g_{o22} + g_{oi} + g_{ob} + g_{o12} + g_{o21})s + [(g_{o22} + g_{oi} + g_{o21} + G_{m22})(g_{o12} + g_{ob}) + G_{m12}G_{m21}]/C^2\right\}. \tag{10}$$

Notice from (9) and (10) that finite transconductor output conductances lead to both pole and zero frequency shifts as well as limit the attainable filter Q. However, since the filter

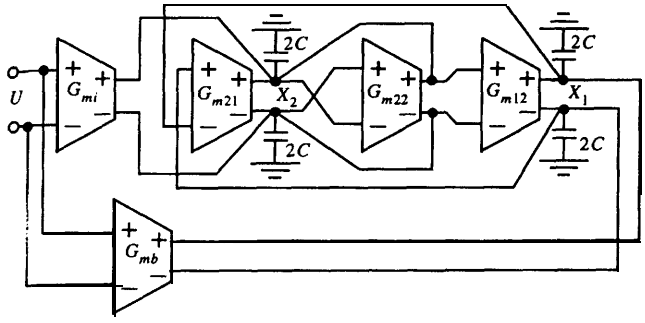


Fig. 7. The adaptive biquad filter.

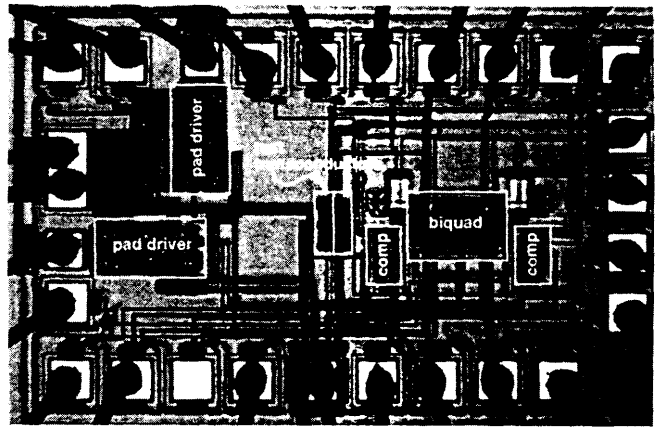


Fig. 8. System chip photomicrograph.

is fully tunable, it is possible to mitigate this problem through tuning. For example, the transconductors G_{mi}, G_{m12}, and G_{m21} were realized using the topology in Fig. 5 and are used to tune the filter gain coefficient via G_{mi} and the filter pole frequency via either G_{m12}, G_{m21}, or both. For these blocks "2-quadrant" operation is sufficient. The transconductor G_{m22} was realized using the "4-quadrant" topology of Fig. 6 so that it can be tuned to enhance filter Q by tuning for negative transconductance to cancel the denominatog_o terms in (9) and (10). The block G_{mb} can be used to shift a mistuned bandpass transfer-function zero, $s_z = -(g_{o12} + g_{ob} - G_{m12}G_{mb})/C$, back to DC. This transconductor is a scaled version of the transconductor in Fig. 5.

A. *Probes*

Observe from Fig. 7 that the filter output signals X_1 and X_2 are both at high impedance nodes. With high frequency signals, it becomes difficult to probe these nodes without affecting the circuit. Thus, 50-Ω analog drivers were implemented. These probe circuits consisted of 8 μm/0.8 μm common-source open-drain NMOS transistors biased at 1 mA to drive external 50-Ω resistors for analog probing. Bipolar emitter followers could have been used, but a Darlington pair would be required to ensure high input impedance. Thus for simplicity, the high impedance FET was preferred for testing purposes.

B. *Comparators*

Since the adaptive system described in Section II requires clocked comparators, these blocks were integrated together with the biquad filter. The comparators were designed for a different system [19] and were incorporated in our test chip. Each comparator consists of a dual-stage BJT differential-pair amplifier with a positive-feedback network to implement a latched comparator [20].

C. *50-Ω Digital Pad Drivers*

To drive the comparator output (ECL levels) off-chip, a large current drive output buffer would be required. To achieve this requirement, a 50-Ω digital pad driver was used. This pad driver consists of a bipolar differential-pair, a bias circuit and a high-current drive bipolar emitter-follower. It has a maximum bandwidth of 500 MHz when driving a 50-Ω load.

TABLE I
BIQUAD EXPERIMENTAL RESULTS SUMMARY

Integrator size	0.14mm x 0.05mm		
Integrator power dissipation	10mW @ 5V		
Biquad size	0.36mm X 0.164mm		
Biquad f_o tuning range	10MHz-230MHz @ 5V, 9MHz-135MHz @ 3V		
Biquad Q tuning range	1-Infinity		
Bq. input-referred noise density	$0.21\mu V_{rms}/\sqrt{Hz}$		
Biquad CMRR	20dB		
Biquad **PSRR+**	28dB		
Biquad **PSRR-**	22dB		
Filter Setting	**Output IP_3**	**Output CP_1**	**SFDR**
106MHz, Q = 2, **Gain = 10.6dB**	23dBm	14.3dBm	35dB
20MHz, Q = 2, Gain = 30dB	20dBm	6.6dBm	26dB
100MHz, Q = 15, **Gain = 29.3dB**	18dBm	6dBm	26dB
227MHz, Q = 35, **Gain = 31.7dB**	10dBm	4dBm	20dB

V. EXPERIMENTAL RESULTS

A photomicrograph of the chip, fabricated in a 0.8-μm BiCMOS process, is given in Fig. 8 distinctly showing the two pad drivers (upper left comer). the biquad filter (bottom right center), two additional test transconductors (center) and the two comparators (below and on either side of the biquad). The entire chip measures 1.7 mm x l .l mm and dissipates 640 mW at 5 V. This large power dissipation is mostly due to the ECL pad drivers which drive high-frequency digital signals off-chip (see Section IV.C). In a fully integrated chip, the digital circuitry would be on chip and the 50-Ω digital pad drivers would not be required. The biquad alone consumes about 50 mW. A summary of the test results is given in Table I.

A. *Transconductance Curves*

The transconductors in Figs. 5 and 6 were tested to compare the obtained tuning curves with theory and simulation. The output transconductance value was calculated by measuring the unity gain frequency of the transconductor for a given capacitive load. The peak transconductance $G_{m,\max}$ for the "2-quadrant" transconductor was about 200 μA/V while the peak transconductance for the "4-quadrant" transconductor was about 88 μA/V. Fig. 9(a) and (b) depict respective transconductor transconductance relative to the maximum attainable

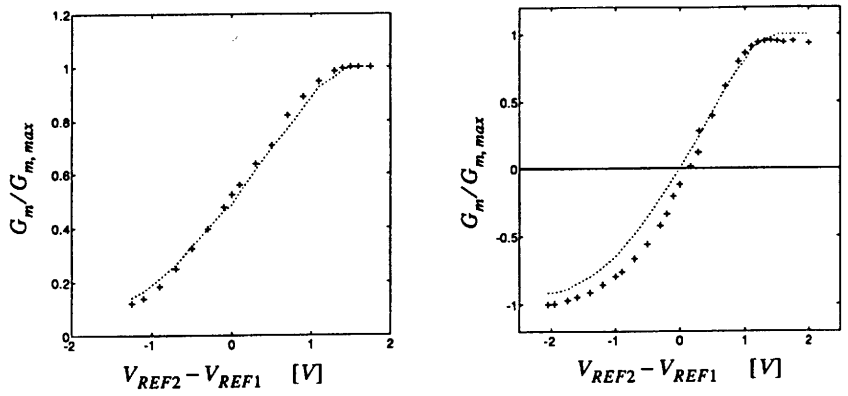


Fig. 9. Experimental (plus symbols) and simulated (dotted curves) transconductance characteristic as function of DC control voltage for the (a) "2-quadrant" transconductor and (b) "4-quadrant transconductor.

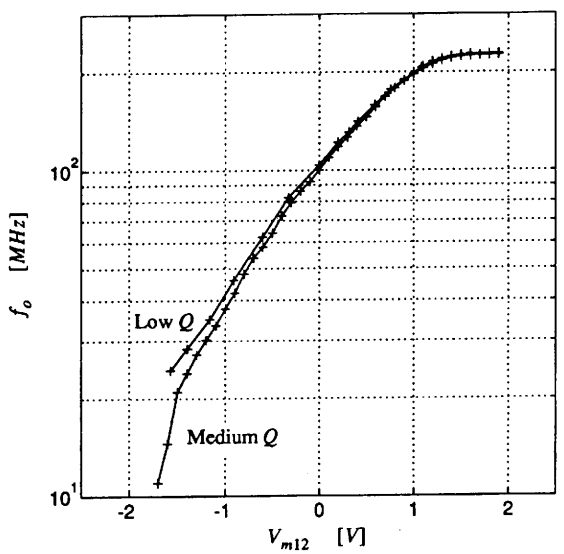


Fig. 10. Illustrating pole frequency tuning range for two different filter Q settings.

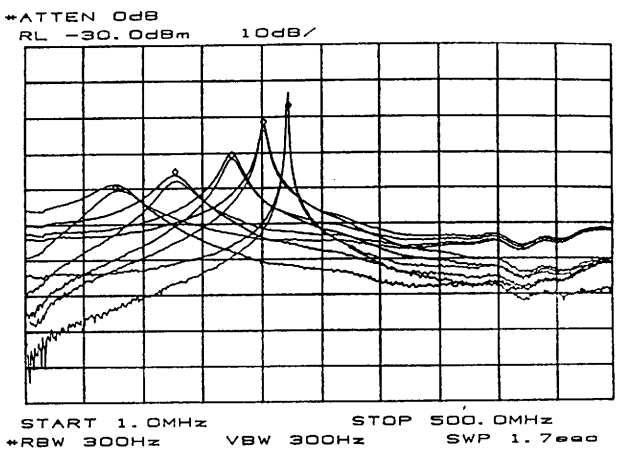


Fig. 11. Illustrating pole frequency tuning for the lowpass and bandpass outputs at fixed G_{m22}. The f_o, Q values are: 222 MHz, 87; 201 MHz, 32; 176 MHz, 13; 128 MHz, 4.6; 78 MHz, 2.1.

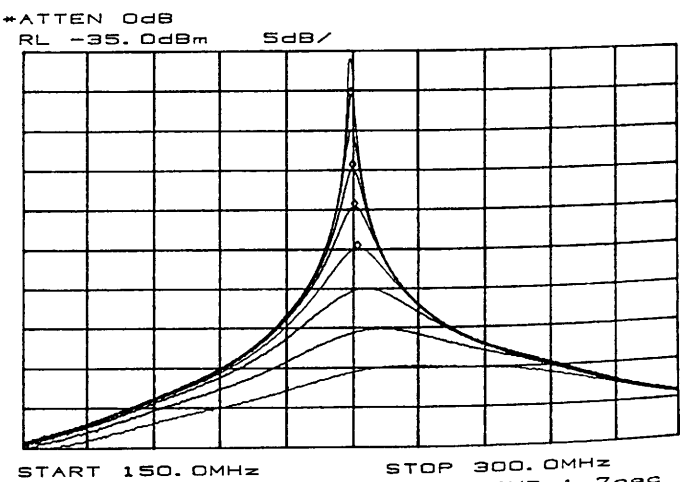


Fig. 12. Bandpass filter response for $f_o = 227$ MHz and Q values of: 160, 126, 88, 54, 26, 19, 10, 5, 3. Input level for each is -50 dBm.

transconductance as function of the control voltage. The experimental results compare with simulations and verify the expressions in (6) and (7).

B. Biquad Tuning Range

To determine the minimum and maximum operating frequencies of the biquad, the control voltage V_{m12} for both G_{m12} and G_{m21} was swept through its entire tuning range while two different control voltages for G_{m22} were selected: $V_{m22} = -1.2$ V (medium Q), $V_{m22} = -0.092$ V (low Q). The other control voltages were fixed as follows: $V_{mi} = 1.74$ V (maximum filter gain), $V_{mb} = -0.575$ V (zero well below 1 MHz). From the plot of the experimental results in Fig. 10 we note the filter can be tuned from 10–230 MHz giving a tuning range of 4.5 octaves for a 5 V supply. For a total power supply level of 3 V, the filter worked satisfactorily and displayed a tuning range of 9–135 MHz. Some of the results depicting the bandpass and lowpass transfer functions are shown in Figs. 11 and 12.

C. Biquad Linearity Tests

One of the mechanisms which limits filter dynamic range is linearity. To determine the linearity of the filter, a two tone intermodulation (IM) distortion test was conducted at

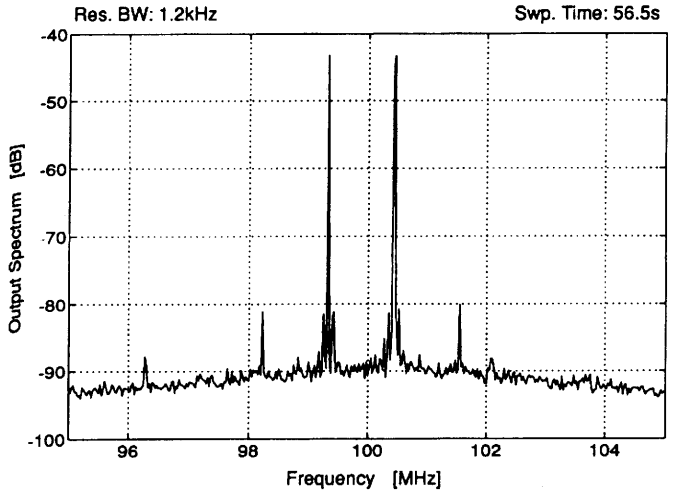


Fig. 13. Experimental IM distortion plot for the 100 MHz $Q = 15$ filter setting.

different filter settings. This test involved placing two tones of equal level within the passband of the bandpass output and measuring the signal to distortion (S/D) ratio between the fundamental tones and the third-order intermodulation tones produced. Since for every 1 dB drop in signal level the IM distortion products drop by 3 dB, from measurements at low levels of distortion it is possible to extrapolate the third-order intercept point (IP_3) [21]. The IP_3 is defined to be the point at which the extrapolated fundamental output tones and the third-order distortion products are at the same level. Based on the IP_3 value it is then possible to compute the output level for any S/D ratio. For example, for the 106 MHz $Q = 2$ filter in Table I (the setting closest to the application response), $IP_3 = 23$ dBm. For 1% IM distortion (S/D = 40 dB) the signal would have to be reduced below IP_3 by 20 dB so that third-order distortion products would be reduced by 60 dB. Hence, a reasonable internal differential filter output level (before the probes) of 3 dBm or 312 mV_{rms} is obtained. As a graphical example, a 37.4 dB (1.35%) IM distortion result for the 100 MHz $Q = 15$ filter is shown in Fig. 13. The overall output level of -40 dBm corresponds to an internal output level of -0.7 dBm.

To obtain the 1 dB compression point (CP_1), the point at which the power level of the filter is reduced by 1 dB from the expected linear gain, the bandpass peak output level was monitored while the input level was varied. From Table I, for the 106 MHz, $Q = 2$ filter the output CP_1 of 14 dBm (1.2 V_{rms}) corresponds to a differential input level of 4.5 dBm or 375 mV_{rms}.

D. Biquad Noise Test

The second mechanism which limits filter dynamic range is noise. A fundamental lower limit on output noise can be obtained by estimating kT/C. For this biquad filter we obtain an output noise voltage of 0.14 mV_{rms}. To measure filter output noise, the filter inputs were grounded and the spectrum at the bandpass output was observed. The total noise was computed based on integrating the noise density over all frequencies.

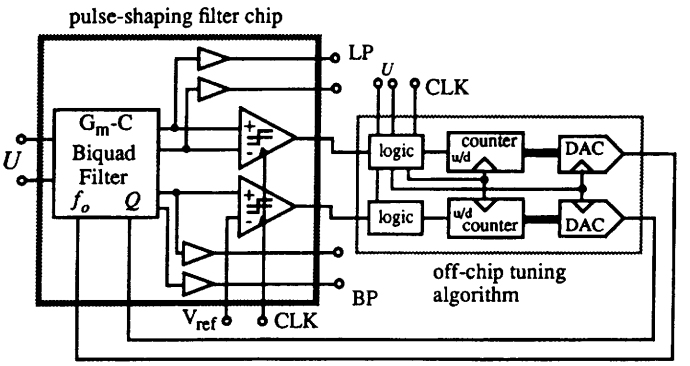


Fig. 14. Block diagram of the adaptive pulse shaping filter system.

Due to the low gain of the probe devices it was not possible to measure output noise for the 106 MHz $Q = 2$ filter, however, for the other three cases in Table I, filter noise was measurable. For the 100 MHz $Q = 15$ filter, the measured peak spectral density is about -91.3 dBm/Hz or 6.1 $\mu V_{rms}/\sqrt{Hz}$ on an internal differential filter bandpass output and the total internal differential output noise voltage is 19.6 mV_{rms}. For this filter setting, the measured differential input-referred noise density is 0.21 $\mu V_{rms}/\sqrt{Hz}$ which compares well the other filter settings and with a simulated figure of 0.223 $\mu V_{rms}/\sqrt{Hz}$.

Considering the 106 MHz $Q = 2$ filter, for the same input noise density above we obtain an internal differential output noise voltage of 7.16 mV_{rms}. At the 1% IM distortion level found above for this filter setting, we obtain a SNR of 33 dB showing that noise dominates the linearity of this prototype. This performance is sufficient for binary signalling, however, this biquad would have to be improved for more demanding signalling.

E. Biquad Spurious Free Dynamic Range (SFDR)

SFDR is a useful figure of merit related to dynamic range. It is usually quoted for radio receiver front end amplifiers and defined as the SNR at the signal level where the distortion equals the noise. For our filter we compute this figure in units of dB using the relation $SFDR = \frac{2}{3}(IP_3 - MDS)$ where MDS is the noise voltage level. The results for different filter settings are given in Table I.

F. Adaptive Pulse-Shaping Filter

A block diagram of the adaptive pulse shaping system is shown in Fig. 14. While all critical high-frequency analog components were integrated, external circuitry consisted of two U/D counters, two low-frequency (not necessarily linear) 12-bit D/A converters and simple digital logic. The digital circuitry implementing the LMS algorithm was placed off-chip to allow flexibility in trying different algorithms. Since it is quite robust, it can easily be placed on chip in a subsequent submission. The amount of digital logic required is not significant as can be inferred from (3) and (5). A pseudo-random 100 Mb/s NRZ ECL bit stream was supplied at the filter inputs and a programmable delay line/duty cycle controller was used to trigger the comparators by a fixed delay

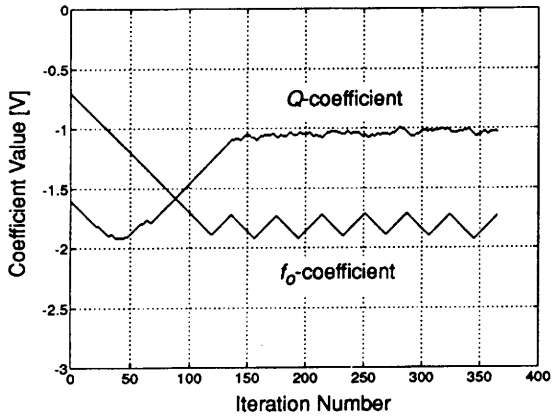


Fig. 15. Experimental coefficient trajectory for the test case presented in the paper.

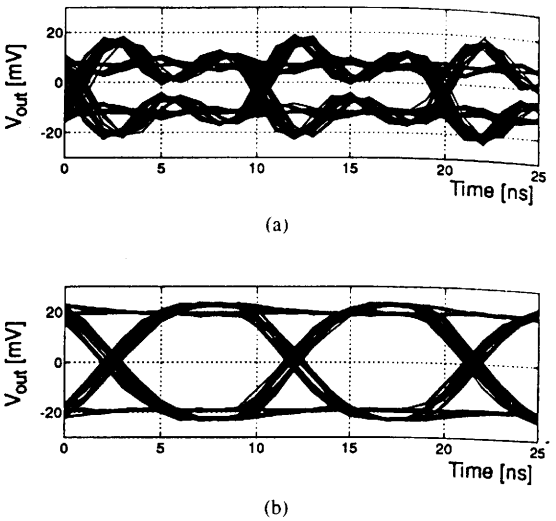


Fig. 16. (a) Filter initial and (b) final output eye diagrams for the test case in Fig. 15.

from data transitions. The measured delay at the chip input was 2.64 ns.

The comparator digital outputs were connected to two channels of a 4-channel, 1 GS/s oscilloscope. The other two channels were connected to the filter input and output ports. The scope was connected to the Ethernet via a general purpose interface bus (GPIB). On a remote SUN workstation, labVIEW [22] was running and hence the scope data was available to this software via the Ethernet. Based on the signals supplied from the scope (namely the 2 comparator outputs and the filter input signal), the LMS algorithms described in Section II were implemented. The outputs of the software were two digital signals to address the two external DAC's that drive the filter f_o coefficient and the filter Q coefficient.

Since there are two degrees of freedom, there are four possibilities for a mistuned filter. These possibilities were each examined and all converged to the same location. Each iteration around the Ethernet-software loop took about 6 s. Clearly many millions of data transitions were ignored between iterations. In Fig. 15, we depict the coefficient trajectory for the case where the filter was mistuned to a pole-frequency and Q above nominal. Observe that the limit cycle for the f_o coefficient is quite large (200 mV). The reason for this large behavior is due to DC offset wherein the algorithm was modified to locate the dead-band introduced due to the offset. The manifestation of this limit cycle leads to f_o jitter or jitter in the filter output zero-crossing and hence distortion. The measured jitter was 422.5 ps, that is, the attained output zero-crossing shifted from a minimum value of 2.8 ns to a maximum value of 3.225 ns. Although this amount of jitter is small and may be tolerable in certain applications, it should be reduced by correcting for the offset problem. In the frequency domain, zero-crossing jitter implies jitter in the filter pole frequency. The filter pole frequency was 111 MHz at the 2.8 ns delay and 95 MHz at the 3.225 ns delay for a total variation of 16 MHz. The initial and final filter output eye diagrams are illustrated in Fig. 16 where the improvement in eye opening due to reduced intersymbol interference is evident.

Compared with the target zero-crossing delay of 2.64 ns, there is an error of at least 0.16 ns, which may be attributed to cable delays, experimental error and circuit performance error. Circuit performance error includes static delay between the main clock and the time the comparators make their decisions. These delays would manifest excess MSE similar to the effect of DC offsets. These effects must be considered relative to the allowable system margin in a given application. The error due to delays would be more severe if the sample point being tested occurs in a region where the signal gradient is large (the zero crossing of the lowpass output) than for a sample point where the signal gradient is small (peak of the bandpass output).

Observe from Fig. 14 that to obtain the error signal for Q adaptation, only a single-ended bandpass output was compared against a single-ended reference level. This single-ended circuitry was due to design time constraints and so a fully differential comparator was not fabricated. Consequently, there is no means of locating any dead-band due to offset on the bandpass output.

Finally, in Fig. 17 we illustrate the filter NRZ input spectrum and the filter output spectra before and after adaptation for the same case mentioned above. The frequency response of the respective filters is shown in Fig. 18. Compared with unfiltered NRZ data, our pulse shaping filter attains about 10 dB and 17 dB harmonic suppression at the third and fifth harmonics of the fundamental frequency (50 MHz), respectively.

VI. Conclusions and Recommendations

A biquad test prototype has been used to demonstrate practical and simple adaptive techniques for tuning high-speed continuous-time filters for data communication applications. The tuning scheme involves the use of comparators to make sample measurements on the filtered output to obtain the required error signal for adaptation. These measurements are used to provide information to solve for the unknown filter parameters. This technique is therefore restricted to a class of line codes for which this approach is feasible. Experimental results demonstrate the first high-frequency integrated analog

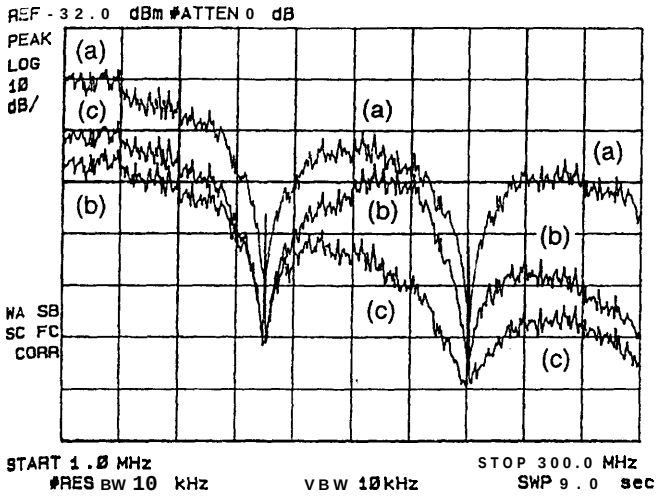


Fig. 17. (a) Filter NRZ input, (b) initial, and (c) final output spectra for the test case in Fig. 15. Reference levels for the input spectrum and output spectra are -10 dBm and -32 dBm, respectively.

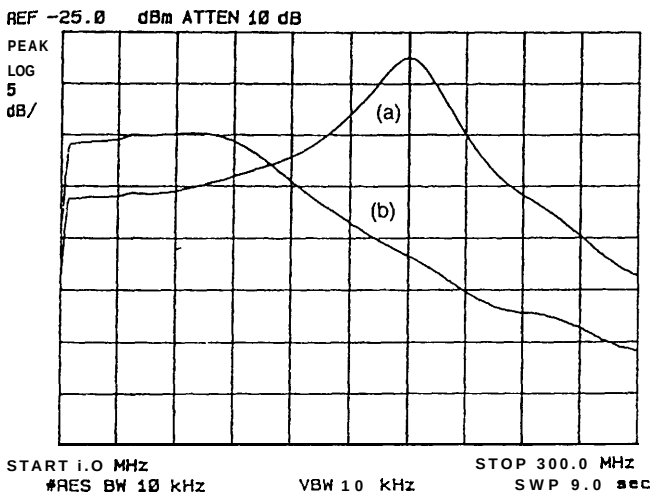


Fig. 18. (a) Filter initial and (b) final frequency responses for the test case in Fig. 15.

adaptive filter and one of the fastest experimental integrated filters reported. Some impairments in this prototype were addressed and the following are possible recommendations.

To eliminate the steady-state jitter in the parameters being adapted, it is possible to freeze the DAC in the middle of the dead-band once the limit cycle is detected. However, rather than locating the dead-band, it is preferable to compensate for the offset directly. For example, given knowledge of the transmit data and the inconsistent comparator outputs, it is possible to detect the offset error and apply a correction adaptively via a bias tap at one of the differential outputs. This solution makes use of the same tuning idea but the unknown parameters are the DC offsets on the lowpass and bandpass outputs.

For this design, the smallest bipolar transistors with a single base contact were used since the design was optimized for speed and power consumption. As a result, noise performance was poor. In fact, relative to the input MOS devices, output noise power is degraded by about 24 dB. Larger BJT's with more base contacts to reduce base resistance and emitter degeneration (500 Ω) could be used to reduce the noise by at least 10 dB. The cost for this alternative would be a lower secondary transconductor pole and possibly more power consumption.

In terms of output resistance, some modification of the basic transconductor might be preferred in a revision circuit to ensure R'_{od} is significantly high, such as by cascoding the Gilbert multiplier.

Finally, we should mention that although a second-order system was described here, for a higher-order filter one can tune the poles using the same f_o adaptation technique. This procedure implies all the poles will be tuned together, either left or right in the frequency domain. Tuning of filter Qs would require more investigation for the particular order, but might be feasible by using the Q information from a biquad section and arranging the other filter Qs to be proportional to the one being adapted.

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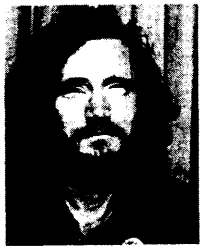

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