Switched-Capacitor Realization of N th-Order Transfer Function Using a Single Multiplexed Op-Amp

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Abstract -This paper presents SC circuits for realizing an arbitrary Nth-order filter function using any number of op-amps, from 1 to N. The reduced op-amp count is obtained at the cost of an increased number of clock phases. Low-noise and low-sensitivity structures are obtained by applying the recently proposed methods of Intermediate-Function Synthesis. An experimental prototype of a 5th-order low-pass filter example is used to verify the proposed multiplexing scheme.

I. INTRODUCTION

SWITCHED-CAPACITOR (SC) circuits are extensively used to implement analog sampled-data filters using integrated circuit technology [1]-[3]. Considerable interest exists in finding new design methods that allow for more economical switched-capacitor filter implementations. One such method is based on a technique for time-sharing or multiplexing individual op-amps, thereby reducing the op-amp count. In general, op-amps represent a considerable amount of circuit die area, consume power, and generate noise. Therefore, fewer op-amps in the filter structure will generally imply a more practical filter realization.

Previous work in this direction [4]-[6] has shown time-sharing methods which reduce the op-amp count by a factor of 2. This paper introduces a method which can reduce the op-amp count by various factors from 1 to N, where N is the order of the transfer function. This large op-amp reduction, however, is at the expense of an increase in the number of clock phases. It should be pointed out however, that the synthesis method presented here is an exact design method, which implies that the circuit can be clocked at relatively low frequencies (limited by the Nyquist rate, but more practically by the prefiltering requirements). This, in turn, reduces the circuit dependence upon the op-amps settling time. Therefore, the extra clock phases can usually be accommodated without the need for higher-speed op-amps.

Unfortunately, however, the additional clock phases complicate the digital clock generation circuitry and layout routing. This in itself may offset any layout area reduction gained from the reduced op-amp count. On the other hand, the structure is very regular so that efficient layouts should be possible. Also, due to the modularity of the proposed structure, this scheme is highly suited for computer-assisted layout thereby automating SC filter design. The authors are presently investigating several possible layout alternatives.

The design method presented begins by generating a state-space description of the transfer function t in terms of the operator A (referred to as the delta operator), which is simply a linear translation of the discrete-time operator z

$$\Delta = z - 1. \tag{1}$$

A direct realization of the state-space description of the filter, in the form of a switched-capacitor structure using a single multiplexed op-amp, is presented in Section II. Also given is a method for reducing the number of required clock phases at the expense of increasing the number of op-amps, resulting in a continuous trade-off between the two numbers. The remaining step in the design, namely the generation of a suitable state-space description from a given filter transfer function, is considered in Section III. Specifically, a systematic procedure is presented for obtaining a low-sensitivity state-space structure from a given set of filter specifications.

Lastly, we will show experimental results using the techniques of this paper for a 5th-order low-pass filter example.

II. MULTIPLEXED SC STRUCTURES

A. Realizations Using a Single Op-Amp

The Nth-order discrete-time linear system can be described by state-space equations of the form

$$(z-1)\boldsymbol{X} = \boldsymbol{A}\boldsymbol{X} + \boldsymbol{b}u \tag{2}$$

$$y = \boldsymbol{c}^T\boldsymbol{X} + du \tag{3}$$

where matrices A, $\boldsymbol{b}, \boldsymbol{c}$, and d have their usual meaning. Substituting (1) into (2) allows us to express the state-variable vector X in the form

$$\boldsymbol{X}(\Delta) = \frac{1}{\Delta}\boldsymbol{A}\boldsymbol{X}(\Delta) + \frac{1}{\Delta}\boldsymbol{b}u(\Delta). \tag{4}$$

In SC technology, the noninverting stray-insensitive integrator [7] has the transfer function $1/(z-1)$ or 1/A.

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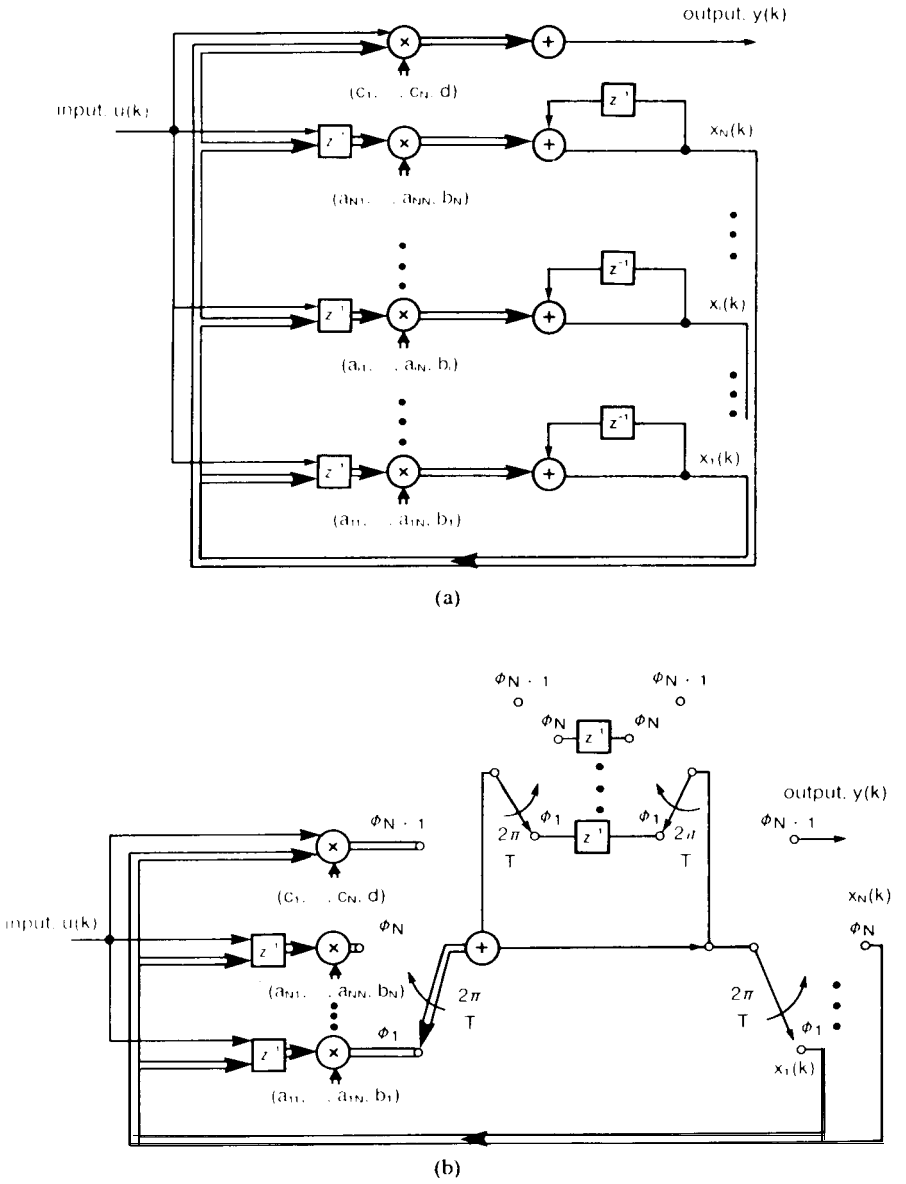


Fig. 1. Functional representation of A domain state-space structure in (a) nonmultiplexed form and (b) multiplexed form.

Therefore, (4) implies that we can synthesize a SC circuit which has as intermediate outputs the state-vector $\boldsymbol{X}$. Then, using a summing circuit which implements (3) enables us to compute the output y. The resulting realization implemented from these state-space equations is said to be synthesized in the delta (A) domain. This A domain representation forms the basis for the multiplexing algorithm proposed here.

In order to implement both positive and negative coefficients of the state-equations with a stray-insensitive noninverting integrator, or what we shall refer to as the A domain integrator, a fully differential circuit is necessary. This will provide for both output signals polarities, thus obviating the need for inverting amplifiers or for the use of the inverting integrator which has a different transfer function [8]. In addition, fully differential circuits offer high common-mode and power-supply rejection. thereby improving the filter dynamic range [1],[9].

The time-domain form of (2) and (3) best illustrates the concept of the A domain multiplexed structures. Taking the inverse z transform of (2) and (3) results in the time-domain expressions

$$x_i(k) = x_i(k-1) \sum_{j=1}^{N} a_{ij} x_j(k-1) + b_i u(k-1), \qquad i = 1, \cdots, N \quad (5)$$

$$y(k) = \sum_{j=1}^{N} c_j x_j(k) + du(k). \quad (6)$$

Fig. l(a) shows a block diagram representation of these state-space equations. We observe that by storing the immediate past states and input, a single multiple-input summing stage can be used to compute the present value of the ith state as a weighted sum of the stored states and the input. The summing stage can be multiplexed to com-

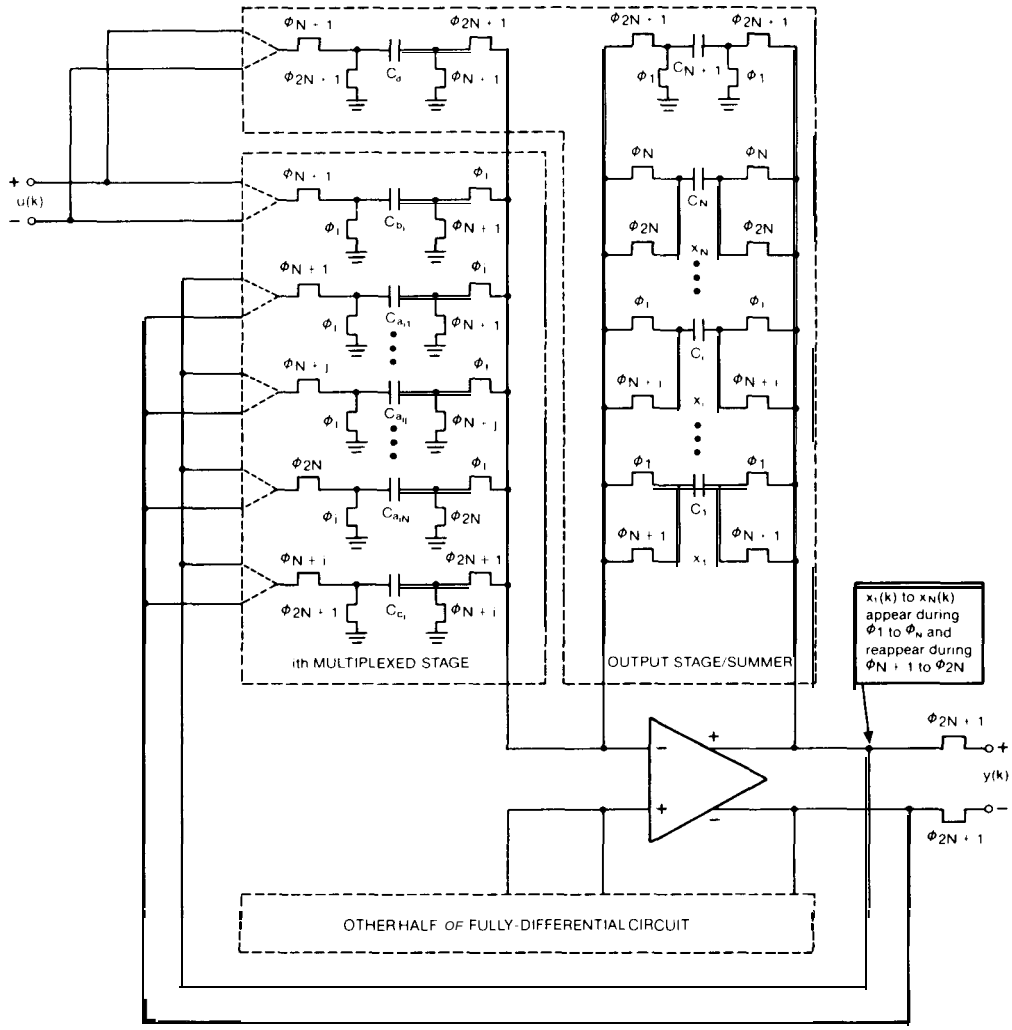


Fig. 2. Generalized multiplexed SC realization for Δ domain state-space structures

pute the present values of all other states. The output y can also be computed with the same summing stage provided the present states and input are made available. A simplified diagram showing the resulting structure is shown in Fig. l(b).

Fig. l(b) would suggest a SC circuit which time-shares a single summing stage, the op-amp, using N + 1 clock phases (N phases to compute the states, one phase to compute the output). Unfortunately, however, realizing this SC structure with only N + 1 clock phases results in a stray-sensitive circuit. This is due to the fact that additional storage capacitors are required to avoid storing presently computed states (or input) in capacitors containing past states (or input). Under specific layout conditions, one can compensate for the stray-sensitive structure and obtain a parasitic-compensated structure [5].

An alternative approach is to delay the storing of presently computed state values in the coefficient capacitors until all the past values of states stored in the coefficient capacitors are utilized. This approach increases the number of clock phases by the number of states N, resulting in 2N + 1 phases, but provides for a stray-insensitive structure. A generalized SC circuit implementing the state-space equations of (2) and (3) with one op-amp is shown in Fig. 2. The circuit operation can be divided into three stages: 1) computation of state values, 2) updating the state values in the coefficient capacitors, and 3) output calculation, which are repeated every clock cycle.

1) Computation Stage: During clock phases ϕ_1 to ϕ_N, the present states $x_i(k)$, for $i = 1$ to N, are computed according to (5) using the weighted past states $x_j(k-1)$, for $j = 1$ to N, and input $u(k-1)$. The i th state is computed during ϕ_i and stored in the feedback capacitor C_i of the op-amp. This calculation uses the past states and input that are stored in the switched capacitors $C_{a_{ij}}$, for $j = 1$ to N, and C_{b_i}.

2) *Updating Stage:* During clock phases ϕ_{N+1} to ϕ_{2N}, the present states are copied into appropriate switched capacitors. These are to be used to compute the output y (the next stage) and delayed for the next computation stage. In particular, the jth state is copied into capacitors $C_{a_{ij}}$ ($i = 1$ to N) and C_{c_j} during clock phase ϕ_{N+j}. The input is obtained during clock phase ϕ_{N+1}, eliminating the need for an additional sample and hold circuit. The input is sampled and stored in capacitors $C_{b_1}, \ldots, C_{b_n}$, and C_d.

3) *Output Calculation Stage:* During clock phase ϕ_{2N+1}, the output $y(k)$ is computed by summing the weighted present states and input, according to (6).

The component values are related to the state-space parameters A, b, c, and d as follows:

$$\frac{C_{a_{ij}}}{C_i} = a_{ij} \qquad \frac{C_{b_i}}{C_i} = b_i$$

$$\frac{C_{c_i}}{C_{N+1}} = c_i \qquad \frac{C_d}{C_{N+1}} = d.$$

B. Reducing the Number of Clock Phases

Time-sharing a single op-amp in a SC circuit requires the op-amp output to change and settle quickly. Instead of using expensive op-amps with faster capabilities, additional op-amps can be introduced into the SC circuit. The objective of adding additional op-amps to the SC multiplexed circuit is to provide for simultaneous computation and updating of several state values. In essence, this will reduce the number of clock phases which will provide more time for the output to reach its true value. Table I illustrates the arrangement of states and phases for a 5th-order SC multiplexed circuit using 2 and 3 op-amps. As is evident from this table, the ordering concept is straightforward and can be easily extended to an Nth-order multiplexed structure using any number of op-amps from 1 to N. Note that the ordering has caused some of the op-amps to be idle during particular clock phases. This arises, in general, because stages of the algorithm cannot be overlapped (i.e., it is not possible to update while computing state values).

The following expression gives the required number of clock phases for an Nth-order filtered using m multiplexed op-amps:

No. of clock phases

$$= \begin{cases} 2(N/m)+1, & \text{when } N/m \text{ is an integer} \\ 2\mathrm{INT}(N/m)+3, & \text{otherwise} \end{cases} \quad (7)$$

where $\mathrm{INT}(\alpha)$ refers to the integer part of a. Fig. 3 shows a plot of the above expression for different filter orders using various numbers of op-amps. In addition, the curves have been expanded to include the points corresponding to two-phase nonmultiplexed structures. One can directly relate the settling time requirement of the op-amp to the number of phases used in the SC circuit; hence, the curves in Fig. 3 can be used to determine the required op-amp bandwidth for a given multiplexed SC filter design. Fig. 3 reveals that, for state-space structures implementing the multiplexing algorithm with 2 op-amps as opposed to 1 op-amp, there is approximately 50-percent reduction in the required number of clock phases. Therefore, in most cases, it may be preferred to implement this multiplexing algorithm with two op-amps.

A SC multiplexed state-space circuit implemented with two op-amps is shown in Fig. 4, assuming N is odd. In this circuit, each op-amp is responsible for computing approximately one-half the number of states, and only one of the two op-amps is used to compute the output y During the phase in which one of the op-amps is idle, that op-amp is connected in a closed-loop configuration, thereby avoiding potentially dangerous open-loop circuit conditions. This two op-amp arrangement reduces the required number of clock phases from 2N + 1 to N + 2. Note that for N even, the required number of clock phases is N + 1.

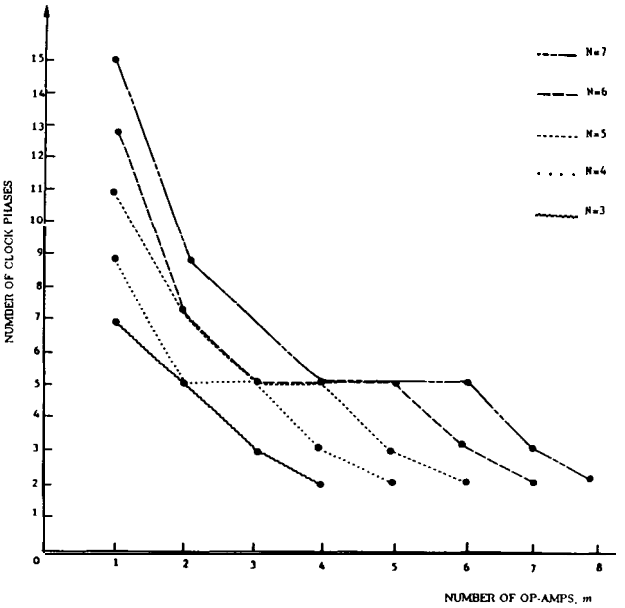


Fig. 3. Multiplexed Nth-order filter with m op-amps.

TABLE I
ARRANGEMENT OF STATES AND PHASES FOR A FIFTH-ORDER SC MULTIPLEXED CIRCUIT USING TWO OR THREE Op-Amps

2 op-amps:

STAGE	PHASE	STATES ASSOCIATED WITH OP-AMP	
		OA-1	OA-2
computation	ϕ_1	x_1	x_4
	ϕ_2	x_2	x_5
	ϕ_3	x_3	idle
updating	ϕ_4	x_1	x_4
	ϕ_5	x_2	x_5
	ϕ_6	x_3	idle
output	ϕ_7	y	idle

3 op-amps:

STAGE	PHASE	STATES ASSOCIATED WITH OP-AMP		
		OA-1	OA-2	OA-3
computation	ϕ_1	x_1	x_3	x_5
	ϕ_2	x_2	x_4	idle
updating	ϕ_3	x_1	x_3	x_5
	ϕ_4	x_2	x_4	idle
output	ϕ_5	y	idle	idle

C. *Finite Transmission Zeros*

SC structures incorporating unswitched capacitors such as those used to form the transmission zeros of elliptic type leap-frog filters can also be multiplexed, but in a limited way. Unswitched capacitors are used to continuously couple an op-amp output with another's input, which

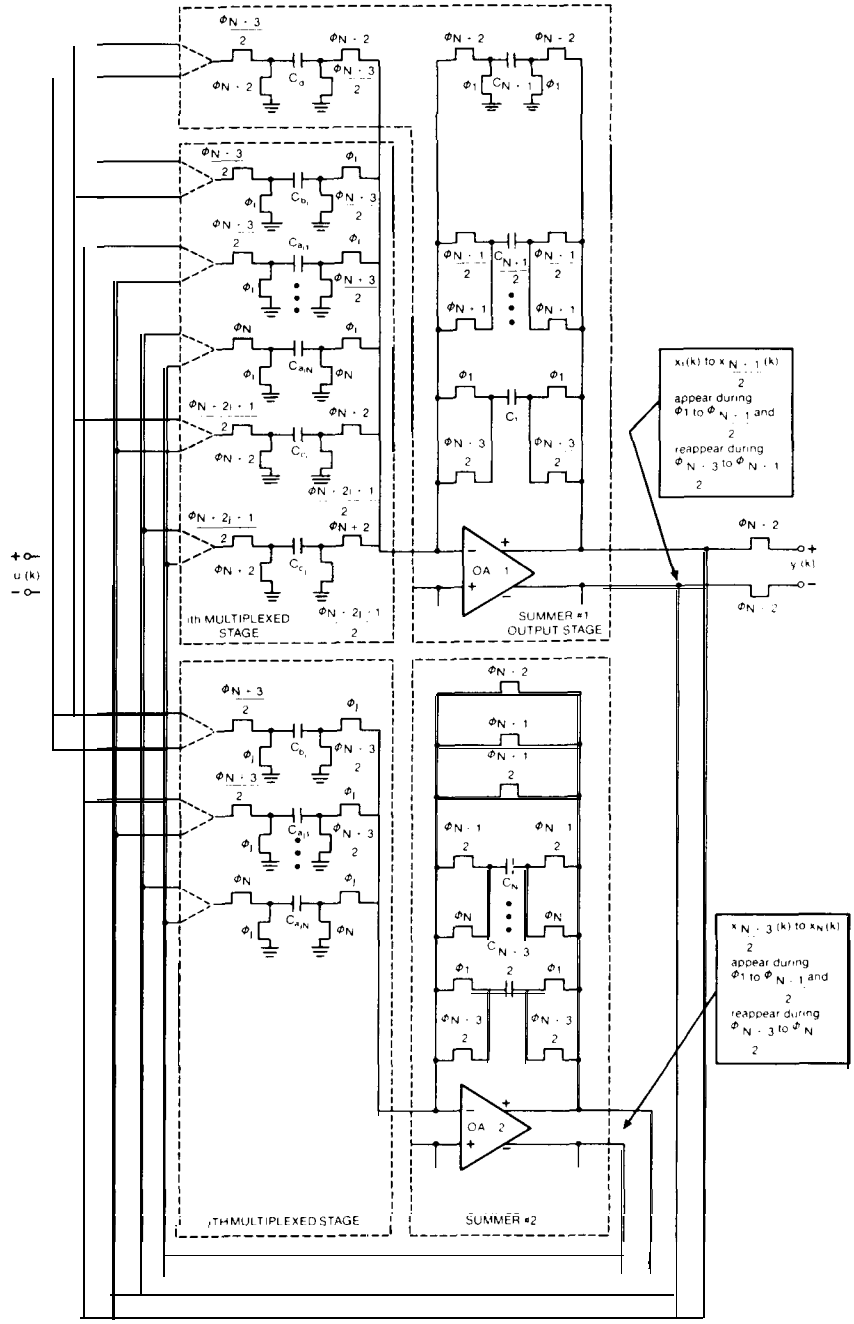


Fig. 4. Multiplexed SC circuit with two op-amps, N odd (only one-half the fully differential circuit is shown).

in turn implies that, at least two or more op-amps must exist in the structure. Fortunately, however, a state-space representation of an arbitrary transfer function containing transmission zeros does not require any continuous feed-in signals. Therefore, the SC multiplexed circuits presented here are complete and do not require additional unswitched capacitors.

D. Open-Loop Condition of the Time-Shared Op-Amp

A common problem in multiplexing is the open-loop condition experienced by the op-amp during the time in which all phases of the multiphase clock are off. This is referred to as the nonoverlap period. During this time, the output of the op-amp can drift to the supply rails, thereby delaying its recovery in the next clock phase. This could seriously degrade circuit performance. One possible solution to this problem is based on the method outlined in [5]. It involves the use of a multiphase controlled switch and two additional capacitors in a circuit that maintains closed-loop conditions during the nonoverlap period. This technique, although effective, results in an increased parts count.

A simpler solution which we have successfully implemented in our experimental prototypes is to design the clock phases such that the nonoverlap period is less than the time required for the op-amp's output to slew a small

amount (e.g., a fraction of a volt). This in turn, virtually eliminates the possibility of op-amp saturation during the nonoverlap period, at no extra cost to the SC multiplexed circuit.

E. Reducing Cross-Talk Effects

Cross-talk effects have been shown to seriously hinder integrated multiplexed SC circuits [3], [14]. They arise mainly because of the parasitic capacitances associated with time-shared op-amps. An applicable solution, presented in [4], which compensates for the dominant cross-talk mechanism is obtained by controlling the design of the differential op-amp and the circuit layout routing.

III. Obtaining Low-Sensitivity State-Space Representation

This section will demonstrate a method for obtaining a A domain state-space description (i.e., A, $\boldsymbol{b}, \boldsymbol{c}$, and d) having an attenuation function that meets required filter specification. From the infinite number of state-space descriptions possible from a single transfer function, we will, in particular, obtain "good" A, $\boldsymbol{b}, \boldsymbol{c}$, and d realizations. Good realizations are those having low-sensitivity and wide dynamic range properties, and are, in general, associated with simulations of doubly terminated LC ladder filters.

Unfortunately, however, an LC ladder cannot be synthesized in the delta domain. This is due to the fact that physical frequencies ω do not map onto points along the imaginary axis of the A plane. This is evident from (1) when z is replaced with $e^{j\omega t}$

$$\Delta = \cos(\omega T) - 1 + j\sin(\omega T). \tag{8}$$

An alternative approach is to synthesize an LC ladder in terms of the bilinear transform variable λ, defined as

$$\lambda = \frac{z - 1}{z + 1}. \tag{9}$$

This transformation maps the unit circle in the z plane onto the entire imaginary axis of the λ plane. The relationship between the frequency ω and the corresponding point Ω on the imaginary axis of the λ plane is given by

$$\lambda = j\Omega = j\tan(\omega T/2). \tag{10}$$

An appropriate set of λ plane ladder states, that is, capacitor voltages and inductor currents, is selected as state-variables to be simulated by the active circuit [10] These state variables determine a set of intermediate functions following the notation of [10] the transfer functions from the ladder input to the capacitor voltages and inductor currents selected as state-variables are denoted intermediate functions $\boldsymbol{f}(\lambda)$. In [10] a method called the Intermediate Function Synthesis is given for obtaining A, $\boldsymbol{b}, \boldsymbol{c}$, and d from the intended transfer function and a set of $\boldsymbol{f}$ functions.

The intermediate functions $\boldsymbol{f}(\lambda)$ and the transfer function $t(\lambda)$ obtained from the LC ladder are then mapped into the A domain via the transformation

$$\lambda = \frac{A}{\Delta + 2}. \tag{11}$$

This results in intermediate functions which are "improper," that is, the order of the intermediate function numerator is the same as its denominator, which is equal to the order of the transfer function. This violates a condition given in [10] which states that the intermediate functions must have numerator orders less than the transfer function order. Fortunately, however, apart from this constraint, the numerators can be arbitrary The following approach has been found to yield a "good" set of proper $\boldsymbol{f}$ functions: those $\boldsymbol{f}$ functions which represent the current of shunt tank circuit inductors or voltage of series tank circuit capacitors and which have numerator roots at $A, = -2 + j0$ (the mapping of $\lambda = \infty$) are made proper by discarding one of these roots. All other $\boldsymbol{f}$ functions are made proper by simply discarding the residue at infinity. Although this approach approximates the internal operation of a doubly-terminated LC ladder network, the intended transfer function is exactly realized. Intermediate functions obtained in this manner have been found to produce structures with relatively sparse matrices and low sensitivity.

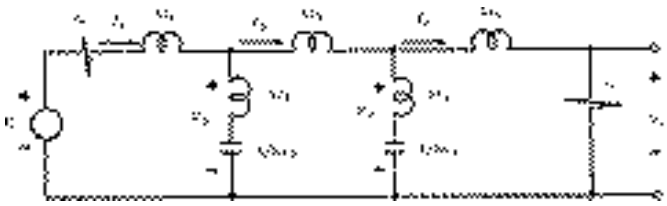
TABLE II
Transfer Function in the Lambda Domain for Low-Pass Example

Polynomial	pole polynomial	zero polynomial
leading coefficient	33 00	0982
list of roots	- 2294 -1685±j 4730 - 0553±j 7216	±j1 4372 ±j2 2219

IV. Design Example and Experimental Results

We shall consider the design of a fifth-order elliptic low-pass SC filter having a passband edge at 1 kHz with 1-dB passband ripple and passband gain of unity. The stopband edge will be at 1.5 kHz with stopband attenuation ≥ 60 dB. The sampling frequency will be 5 kHz.

The delta domain design procedure begins by prewarping the SC filter specifications according to (10). Filter design tables or computer programs can be used to obtain a transfer function $t(\lambda)$ and an LC ladder network whose attenuation function meets the prewarped specifications. Table II lists the poles and zeros of a transfer function meeting the prewarped specifications. An LC ladder realization of this transfer function is given in Fig. 5. The resulting intermediate functions selected for the state-space realization are listed in Table III. These intermediate functions as well as the transfer function $t(\lambda)$ are transformed into the A domain via (11). We then alter the intermediate functions according to the procedure outlined in Section III. This will provide us with a set of "proper" inter-



r_s	l_1	l_2	l_3	l_4	l_5
1.0	2.604	.3840	3.7189	.1434	2.8152
r_l		c_2		c_4	
1.0		1.2607		1.4125	

Fig. 5. λ domain *LC* ladder.

TABLE III
ZEROS OF THE INTERMEDIATE TRANSFER FUNCTION FOR LC LADDER IN THE LAMBDA AND DELTA DOMAINS

f_4	V_c/V_i	−.35521 ij1.4372	-2.000 + j0 −.5242 + j0 −1347±j 9380
f_5	I_{l_5}/V_i	±j1 4372 ±j2.2219	-1.0546±j1.0813 −11386±j 44404

mediate functions which are listed in the rightmost column of Table III. Application of the IF synthesis equations found in [10] leads to the following A domain state-space structure:

$$\boldsymbol{A} = \begin{bmatrix} -.6717 & 0 & .7195 & 0 & 0 \\ .3345 & -.6271 & -.8878 & .5696 & .3696 \\ 0 & 0 & -.7666 & 0 & .7703 \\ -.0607 & -.821139 & .4428 & -.6844 & -.9683 \end{bmatrix}$$

$$\boldsymbol{b} = \begin{bmatrix} -.8627 \\ .4144 \\ -.4425 \\ .0963 \\ -.3442 \end{bmatrix}$$

$$\boldsymbol{c}^T = \begin{bmatrix} 0 & 0 & 0 & 0 & -.6072 \end{bmatrix} \quad d = .0169.$$

This structure has been scaled for optimum dynamic range; the intermediate functions $\{f_i\}$ are scaled for unity L_2 norms. The equations of Section II-A can be used to obtain a fifth-order SC circuit. It can then be scaled for minimum total capacitance (for our example, 488 C_u, where C_u is the minimum capacitance available in the implementation technology). It should be mentioned that a large proportion of the total capacitance (192 C_u in our example) is required for the output calculation, a direct result of the small value of ***d.***

TABLE IV
INDIVIDUAL A DOMAIN INTEGRATOR SENSITIVITIES (EXPRESSED IN DECIBELS FOR A 1-PERCENT VARIATION IN EACH INTEGRATOR GAIN)

DESIGN METHOD	TRANSFER FUNCTION CHANGE, Δt_i DUE TO THE *ith* INTEGRATOR CHANCE				
	1	2	3	4	5
delta domain	+ 113	+ 550	+ 271	+ 496	+ 027
ref [12]	+ 021	+ 214	+ 226	+ 189	+ 021

If we consider these state-space equations to be implemented in a nonmultiplexed fashion, then a useful measure of performance for the filter realization is the output noise power resulting from the noise contribution made by each integrator. In particular, if noise with a white spectral density of 1 W/Hz is applied to the input of each integrator, then this structure will have an output noise power of 1.72 W.[1] This figure can be compared to an optimum structure having an output noise power of 1.15 W [10], [11]. Comparing the two noise figures indicates that our A domain structure is 1.75 dB below the optimum. This would indicate that further improvement to the A domain state-space structure is possible and should be sought after.*

Although the multiplexing realization uses a single op-amp, integration is performed five times. Thus, the usual performance measure of evaluating the transfer function sensitivity to each integrator gain can be employed here. Table IV presents the results of a worst-case sensitivity analysis performed using the methods of [10]. Specifically, the largest transfer function variations within the filter passband resulting from a l-percent change in the gain of every integrator are given. For comparison purposes, we also list in Table IV the sensitivity results for the design proposed in [12]. Although the method of [12] produces a less sensitive structure, it does not offer the multiplexing capability of the A domain state-space structure. Therefore, depending upon the design requirements, a more sensitive structure may be preferred when the advantages of multiplexing with one or two op-amps are considered.

In order to verify the methods of this paper, we have simulated and breadboarded the design example of this section using the single op-amp circuit of Fig. 2. The SC simulation program SWITCAP [13] produced results simi-

[1] The method for performing these calculations is given in [10].

[2] Although our generalized SC filter circuit would appear to require a large number of switches, the switch count can be reduced with appropriate switch-sharing. In particular, our fifth-order design example requires a minimum of 64 switches. For comparison purposes, we note that a design based on the synthesis method of [12] requires a minimum of 56 switches. Therefore, our proposed circuit structure has almost the same number of potential noise sources as the state-of-the-art.

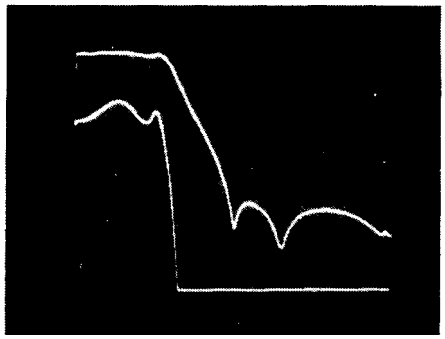


Fig. 6. Measured response of the fifth-order elliptic single op-amp Δ domain low-pass filter. horizontal 0.2 kHz/div. Vertical: 10 dB/div. (upper trace), 1 dB/div. (lower trace).

lar to those obtained by the breadborded circuit. The breadboarded circuit implemented the differential op-amp using two LF356-type op-amps; one op-amp acted as the front-end differential stage and the other as an inverter to produce the complementary output. The switches used were of the CA4066 type and an ll-phase clock of 5-kHz frequency was generated with a digital circuit having a master clock frequency of 55 kHz. The nonoverlap time of each phase lasted no longer than 50 ns.

Fig. 6 shows the measured response obtained from the SC circuit of this example. The output was measured using a sample-and-hold circuit; hence, the $\sin(x)/x$ function multiplies the response.

V. Conclusions

We have presented a fully-differential stray-insensitive multiplexing algorithm using 1 to N op-amps, realizing any Nth-order transfer function. The synthesis method is straightforward once a state-space representation of the given transfer function is obtained. Various circuit options have been introduced, increasing the versatility and practicality of the multiplexing scheme. Low-sensitivity state-space representations were obtained by applying the methods of IF synthesis. The algorithm presented was verified using both computer simulation and breadboard experimentation.

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