A 4TH-ORDER BANDPASS SIGMA-DELTA MODULATOR

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Abstract

Digital radio receivers must perform the analog-to-digital conversion of bandpass signals. For signals with small relative bandwidths, bandpass $\Sigma\Delta$ analog-to-digital converters offer high signal-to-noise ratios at significantly lower sampling rates than are required for lowpass $\Sigma\Delta$ converters, while still providing excellent linearity. A 4th-order bandpass $\Sigma\Delta$ modulator implemented in a 3 μm CMOS process has been designed to convert bandpass signals centered at 455 kHz with 10 kHz bandwidth. The converter is clocked at a mere 1.82 MHz, and realizes greater than 65 dB SNR. A single converter occupies 3.4 mm x 1.8 mm and consumes approximately 230 mW.

Introduction

Sigma-delta modulation has very recently become the method of choice for high resolution A/D conversion. The benefits of oversampled noise-shaping converters include inherent linearity, reduced anti-aliasing filter complexity, high tolerance to circuit imperfection, and a system architecture that lends itself to switched-capacitor implementation [1]. The bandpass variant of $\Sigma\Delta$ retains these advantages and offers a promising technique for use in the rapidly developing area of digital radio [2][3].

Traditional $\Sigma\Delta$ converters place noise transfer-function zeros near $\omega_0 = 0$ in order to null quantization noise in a narrow band around DC. This noise-shaping concept was extended in [4] to the bandpass case, wherein the noise transfer-function zeros are placed at a non-zero frequency, ω_0. Quantization noise is nulled in a narrow band around ω_0, such that the output bit-stream accurately represents the input signal in this narrow band.

For narrow-band signals away from DC, the band-reject noise shaping of a bandpass $\Sigma\Delta$ converter results in high signal-to-noise ratios at significantly lower sampling rates than are required for lowpass $\Sigma\Delta$ converters. The oversampling ratio is defined as one-half the sampling rate divided by the width of the band of interest. Imagine the conversion of a signal centered at 1 MHz with 10 kHz bandwidth: with a 10 MHz sampling rate, a traditional converter would provide 5 times oversampling; a bandpass $\Sigma\Delta$ converter would achieve 500 times oversampling [2][3].

Bandpass $\Sigma\Delta$ A/D converters are well suited for use in the front-end of radio receivers, allowing direct conversion to digital at either intermediate- or radio-frequency [3]. An early conversion to digital results in a more robust system with improved testability, and may result in a reduced component count and lower power consumption. Additionally, it provides opportunities for dealing with the multitude of standards present in commercial broadcasting and telecommunications.

This paper presents a 4th-order bandpass $\Sigma\Delta$ modulator that converts signals with 10 kHz bandwidth centered at 455 kHz. The circuit is implemented in a 3 μm, ± 5 V CMOS process with standard switched-C circuit techniques, and was implemented by modifying an existing lowpass $\Sigma\Delta$ integrated circuit.

The Transfer Functions

In a discrete-time system, a choice can be made in the location of the band-of-interest. Tradeoffs are possible among sampling rate, oversampling ratio, and anti-aliasing filter requirements [2]. We wish to convert a signal centered at 455 kHz with 10 kHz bandwidth, and by placing the band at $f_s/4$ *we* achieve an oversampling ratio of 91 with a sampling rate of 1.82 MHz. A summary of the design values is given in Table 1.

Parameter	Symbol	Value	Normalized Value
center frequency	f_o	455 kHz	$\pi/2$
bandwidth	fb	10 kHz	$\pi/91$
sampling **freq**uency	f_s	1.82 MHz	2π
oversampling ratio	OSR	91 ($f_s/2f_b$)	

Table 1   Design parameters for our 4th-order bandpass $\Sigma\Delta$ modulator.

In the analysis of $\Sigma\Delta$ modulators, the quantizer is often replaced by an additive noise source to yield a linear model. The input signal, u, and the noise of the quantizer, n, have different z-domain transfer functions to the output, y. Figure 1 shows the pole-zero placement for the signal transfer function (STF) and the noise transfer function (NTF) in the z-plane. The 4th-order modulator NTF has two complex-conjugate pairs of zeros, optimally located around an angular frequency of $\pi/2$ ($f_s/4$) in order to null quantization noise in a narrow band around $f_s/4$. The STF zeros are placed at

$z = -1$ ($f_s/2$), $z = 1$ (DC) and $z = 0$. Note that the transfer functions share poles, due to our choice of structure.
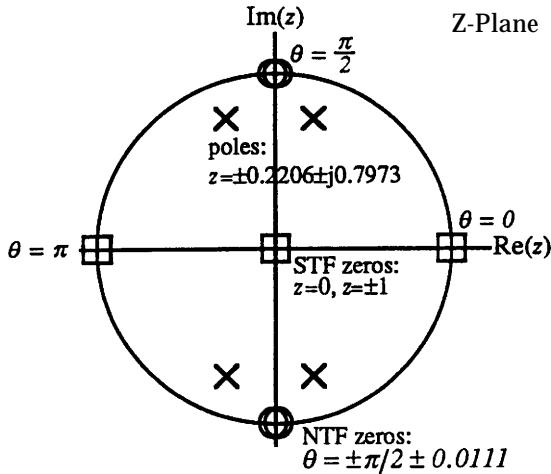

Figure **1**   Pole-zero placements for the noise and signal transfer functions of the 4th-order bandpass $\Sigma\Delta$ modulator.

The Modulator Architecture

The transfer functions above are implemented using a cascade-of-resonators structure described previously in [5] and [6]. This structure has been shown to have adequate sensitivity properties for bandpass $\Sigma\Delta$ modulators [2].
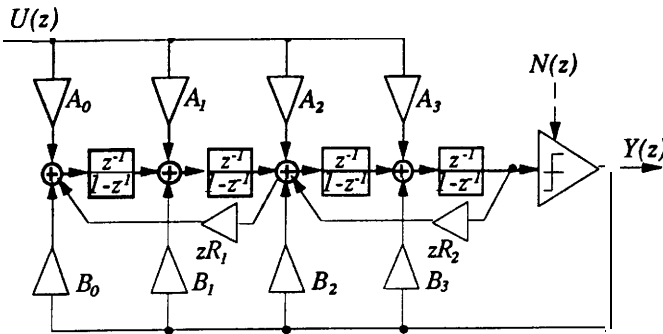

Figure 2   The Cascade-of-Resonators Structure.

The cascade-of-resonators structure is named for its two-integrator "resonator" loops. Each resonator is formed as a lossless-discrete-integrator (LDI) pair. The loop forms a biquad with its poles on the unit circle that would resonate were the modulator feedback removed. With the modulator feedback, the poles of the resonators become the zeros of the NTF. The R coefficients are set by capacitor ratios, which must accurately center the noise-shaping around 455 kHz. Mismatch in the R capacitor ratios causes the NTF zeros to move from their optimal locations, which increases the in-band noise power and lowers the SNR.

Each integrator shown in Figure 2 represents a delayed-type integrator, or rather, the clock phasing produces a delayed-type integration. The A coefficients are switched-capacitor feed-ins to these delayed-type integrators. The R coefficients are actually feed-ins to non-delaying integrators, and are thus symbolically modified by the z term to cancel the delay. The B coefficients are also feed-ins to non-delaying integrators and are modified by z terms, but the z terms are cancelled by a z^{-1} delay term associated with the latched comparator. The output of each integrator feeds the following integrator in a delayed fashion, with some gain if desired.

Modulator Implementation

The modulator was implemented by modifying an existing IC [6] at Analog Devices Semiconductor Division. While this modification process. facilitated the fast turn time of a robust test chip, it imposed several design constraints, particularly with respect to modulator order and allowable capacitor sizes, that ultimately reduced the effectiveness of the resulting IC from a "design-from-scratch" approach.

Capacitor Sizes

The bandpass $\Sigma\Delta$ modulator was designed with fully-differential switched-C circuit techniques. A single-ended representation of the modulator is shown in Figure 3. In this single-ended circuit (with positive capacitors) the A coefficients can only be positive as they are implemented with non-inverting feed-ins, whereas the B and R coefficients can only be negative as they are implemented with inverting feed-ins. Both positive and negative coefficients are typically required for bandpass modulators, and are easily accommodated in a differential design. Negative capacitor ratios are realized by making polarity-reversed connections to the differential op-amp outputs. Clock phasing was chosen for compatibility with the existing IC.

Capacitor ratios were chosen to correctly set the NTF and STF coefficients of the cascade-of-resonators structure shown in Figure 2, and were then adjusted to scale the circuit for maximum dynamic range. As the bandpass $\Sigma\Delta$ concept is new, and the effects of clipping are not yet well understood, a conservative ℓ_∞-norm was used: integrator output swings were found for a variety of inputs, and scaling was based on the worst-case integrator states plus a 10% safety margin. Absolute capacitor sizes were chosen to realize these scaled ratios, but unit capacitor sizes were constrained by the use of an existing IC, limiting capacitor precision to about 1%.

The clock-phasing used in the original IC is not optimal. In certain clock phases multiple op amps are connected in series, which results in "second-order" settling that increases the settling time and makes analysis difficult.

It is believed that a design of the bandpass $\Sigma\Delta$ circuit from scratch, with all op amps and capacitor ratios optimized for circuit speed, along with an improvement of the clock-phasing scheme, would more than double the speed of the IC. The use of a faster process would further increase the IC speed.
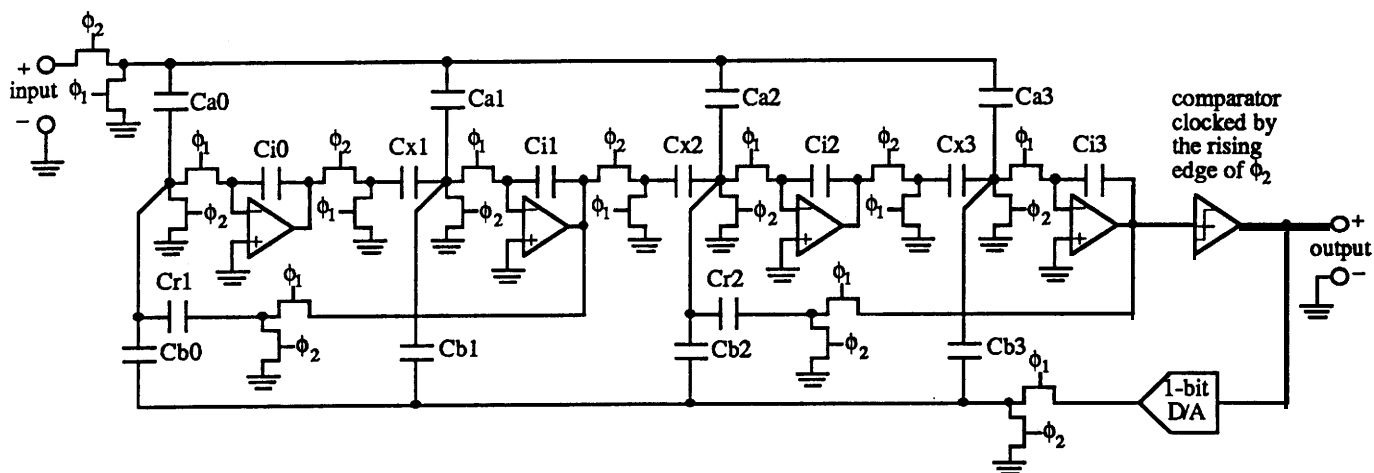
parameter	R_1	A_0	B_0	X_1	A_1	B_1	X_2	R_2	A_2	B_2	X_3	A_3	B_3
initial coefficient	-1.9778	-0.2974	-0.2755	1.0000	-0.2942	0.0183	1.0000	-20222	0.1504	0.8254	1.0000	0.1471	0.00o0
scaled coefficient	-1.3940	-0.1701	-0.1576	1.4188	-0.2388	0.0149	0.3834	-1.4394	0.0468	0.2569	1.4049	0.0643	0.0000
capacitor ratio	1.3940	-0.1701	0.1576	1.4188	-0.2388	-0.0149	0.3834	1.4394	0.0468	-0.2569	1.4049	0.0643	0.0000

Figure 3 A single-ended representation of the 4th-order modulator with the cascade-of-resonators structure. The coefficients have been scaled to maximize circuit dynamic range. The negative capacitor ratios are realized in a differential design by polarity-reversed connections to the differential op-amp outputs.

Modulator Order

A bandpass $\Sigma\Delta$ modulator typically has even order, so a modification of a fifth-order lowpass modulator could produce only a second or fourth-order modulator. As the original IC contained dual fifth-order modulators, identical fourth-order bandpass modulators were implemented on the IC, one in each of the existing channels. This required the first stage in each channel to be completely disabled.

Experimental Results

A photomicrograph of the IC appears in Figure 4. Each modulator occupies an active area of approximately 3.4 mm by 1.8 mm. Two modulators exist side-by-side on the die, giving the left-to-right symmetry. Fully differential switched-C techniques were used, resulting in the internal symmetry. The large capacitors of the disconnected first stages are clearly evident towards the top of the photo.

Output bit-stream data was gathered and analyzed to determine the shape of the modulator's output spectrum. The clock rate was the nominal 1.82 MHz, with no input signal injected into the modulator. Figure 5 shows the experimental spectrum overlaid on a simulated spectrum. Both output spectra contain lK-bins, obtained (by summing the power in 8-bin groups) from the first 8K-bins of a 16K-bin Hann-weighted FFT of the modulator output bit-stream. The band-reject noise-shaping is clearly evident in the experimental data spectrum, and the noise-shaping notch is centered at 455 kHz as expected. Similar tests were undertaken on several IC samples, and all had nearly identical output spectra.

The modulator was then tested at its nominal 1.82 MHz, with a 455 kHz sine-wave injected into the input. The noise-shaping remained, and a spike appeared at the 455 kHz mark, indicating that the modulator did indeed convert the input signal accurately in the narrow 10 kHz band centered at 455 kHz. Indeed, as the level of the input signal was adjusted in 10 dB increments, the representation of that frequency in the output bit-stream changed by the same amount.

A proper signal generator was not available at test time to inject a suitable signal: one with sufficiently low frequency jitter to confine its input signal to only a few frequency bins. Despite this, preliminary results indicate a signal-to-noise ratio of 65 dB over a 10 kHz bandwidth. This is nearly the performance expected from simulations: ideal 78 dB SNR for a half-scale input signal, with 2-3 dB degradation from finite 55 dB op-amp DC gain and 6-8 dB degradation from random 1% capacitor mismatch. Further experimentation is underway to achieve proper SNR results.

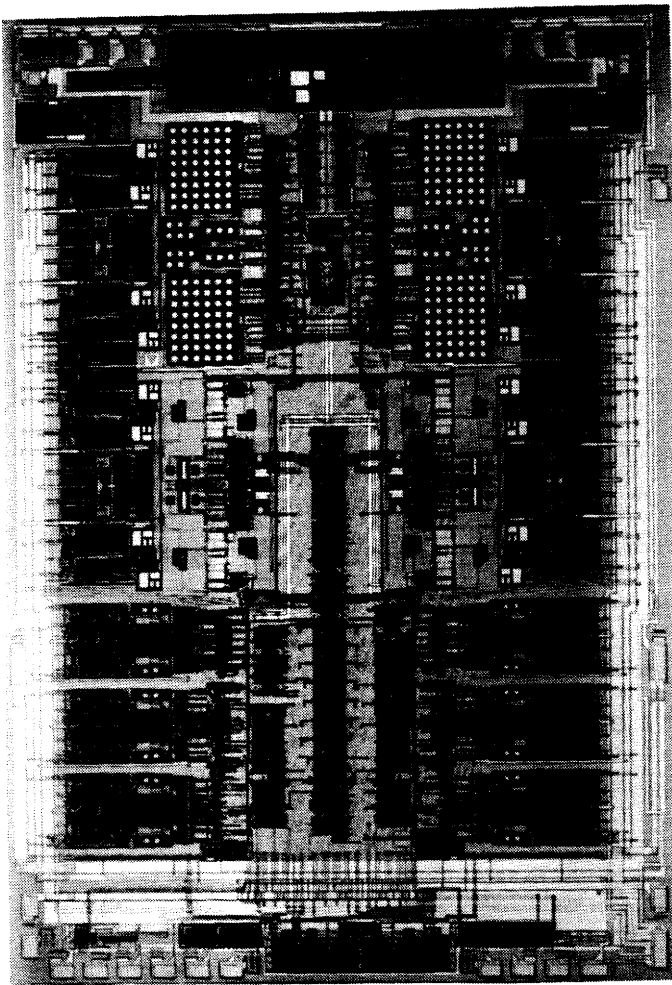Power consumption for the IC is 750 mW, with approximately 230 mW per modulator.

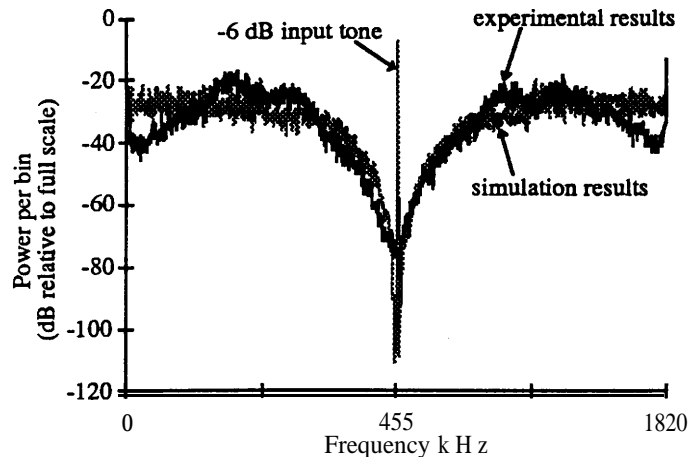**Figure 4** Photomicrograph of the bandpass ΣΔ IC.

Figure 5 Output spectra of the 4th-order bandpass IC centered at 455 kHz with 10 kHz bandwidth. Spectra are shown for both simulated and experimental data.

References

[1] J. C. Candy and G. C. Temes, "Oversampling Methods for A/D and D/A Conversion" in **Oversampling** *Delta-Sigma Converters,* (J. C. Candy and G. C. Temes, Eds.) IEEE Press, 1992.

[2] S. Jantzi, R. Schreier and M. Snelgrove, "Bandpass Sigma-Delta Analog-to-Digital Conversion," *IEEE Transactions on Circuits and Systems,* **vol. 38, no. 11,** pp. 1406-1409, Nov 1991.

[3] S. A. Jantzi, R. Schreier, and M. Snelgrove, "A Bandpass ΣΔ A/D Convertor for a Digital AM Receiver," *Proceedings of the IEE Internutionai Conference on Analogue-to-Digital and Digital-to-Analogue Conversion,* Swansea, U.K., pp. 75-80, 17-19 Sept. 1991.

[4] R. Schreier, and M. Snelgrove, "Bandpass Sigma-Delta Modulation," *Electronics Letters,* **vol. 25,** no. *23,* pp. 1560-1561, 9th November 1989.

[5] P. F. Ferguson Jr., A. Ganesan, and R. W. Adams, "One Bit Higher Order Sigma-Delta A/D Converters," *Proc. IEEE Int. Symp. on Circuits and Systems,* pp. 890-893, May 1990.

[6] P. F. Ferguson Jr., A. Ganesan, R. W. Adams, S. Vincelette, R. Libert, A. Volpe, D. Andreas, A. Charpentier and J. Dattorro, "An 18b 20kHz Dual Sigma-Delta A/D Converter," *Proc. IEEE Int. Solid-State Circuits* pp. 68-69, Feb 1991.

Conclusions

To our knowledge, the world's first bandpass ΣΔ IC has been designed and fabricated. The modulator performs the necessary operations of band-reject noise shaping the quantization noise and passing narrow-band input signals. The IC has been shown to operate at speeds exceeding the nominal design speed by 70%. Preliminary test results are very promising, and indicate a signal-to-noise ratio of 65 dB, or ll-bit performance, in the conversion of signals at 455 kHz while clocked at a mere 1.82 MHz.

Modification of an existing IC reduced the design time considerably and increased the likelihood of success, but imposed several design constraints. The modulator was limited to 4th-order, and SNR performance could be increased by nearly 24 dB by using a 6th-order modulator. A "design-from-scratch" approach using the same 3 μm process, with an improvement of the clock phasing scheme and with all op amps and capacitor sizes optimized, would likely improve the operating speed of the modulator by greater than two times and the SNR by 6dB. The use of a faster process would **give** a further increase in circuit speed.